



STFI26NM60N

N-channel 600 V, 0.135 Ω , 20 A MDmesh™ II Power MOSFET in I²PAKFP package

Datasheet — production data

Features

Type	V _{DSS}	R _{DS(on)} max	I _D
STFI26NM60N	600 V	< 0.165 Ω	20 A

- Fully insulated and low profile package with increased creepage path from pin to heatsink plate
- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET applies a new vertical structure to the company's strip layout to yield a device with one of the world's lowest on-resistance and gate charge, making it suitable for the most demanding high-efficiency converters.

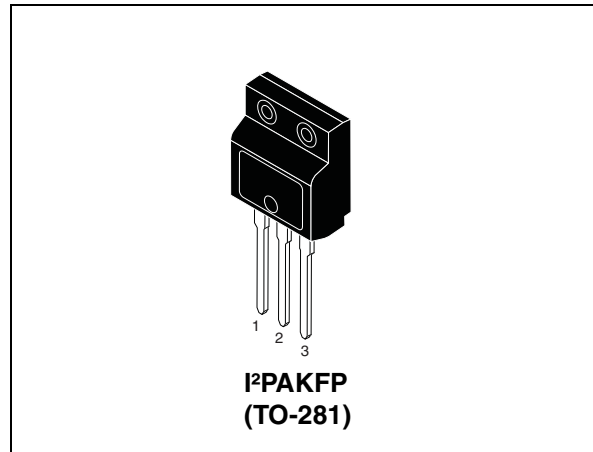


Figure 1. Internal schematic diagram

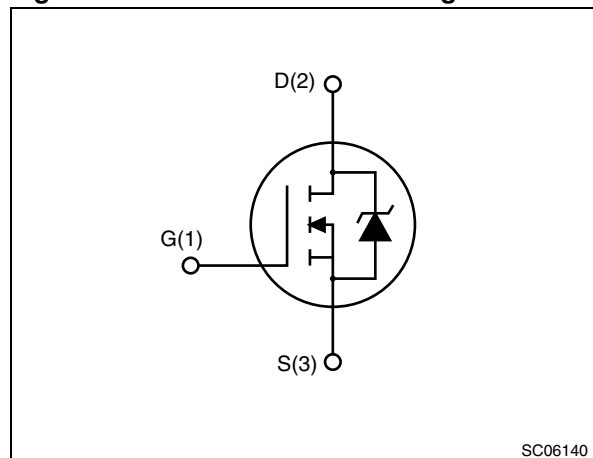


Table 1. Device summary

Order codes	Marking	Package	Packaging
STFI26NM60N	26NM60N	I ² PAKFP (TO-281)	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	600	V
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	20 ⁽¹⁾	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	12.6 ⁽¹⁾	A
$I_{DM}^{(2)}$	Drain current (pulsed)	80 ⁽¹⁾	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	35	W
	Derating factor	0.28	W/ $^\circ\text{C}$
$dv/dt^{(3)}$	Peak diode recovery voltage slope	15	V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s; $T_C=25\text{ }^\circ\text{C}$)	2500	V
T_{stg}	Storage temperature	- 55 to 150	$^\circ\text{C}$
T_j	Max. operating junction temperature	150	$^\circ\text{C}$

1. Limited by maximum junction temperature.

2. Pulse width limited by safe operating area .

3. $I_{SD} \leq 20\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DSpeak} \leq V_{(BR)DSS}$, $V_{DD} = 80\% V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	3.6	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	$^\circ\text{C}/\text{W}$

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	6	A
E_{AS}	Single pulse avalanche energy (starting $T_j=25\text{ }^\circ\text{C}$, $I_D=I_{AS}$, $V_{DD}=50\text{ V}$)	610	mJ

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	600			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 600\text{ V}$ $V_{DS} = 600\text{ V}$, $T_C = 125\text{ °C}$			1 100	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 25\text{ V}$			± 0.1	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 10\text{ A}$		0.135	0.165	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 50\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	1800	-	μF
C_{oss}	Output capacitance			115		
C_{rss}	Reverse transfer capacitance			1.1		
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0$, $V_{DS} = 0\text{ to }480\text{ V}$	-	310	-	μF
Q_g	Total gate charge	$V_{DD} = 480\text{ V}$, $I_D = 20\text{ A}$, $V_{GS} = 10\text{ V}$, <i>(see Figure 15)</i>	-	60	-	nC
Q_{gs}	Gate-source charge			8.5		
Q_{gd}	Gate-drain charge			30		
R_g	Gate input resistance	$f = 1\text{ MHz}$ gate DC Bias=0 test signal level = 20 mV open drain	-	2.8	-	Ω

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 10\text{ A}$ $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ <i>(see Figure 14)</i>	-	13	-	ns
t_r	Rise time			25		
$t_{d(off)}$	Turn-off delay time			85		
t_f	Fall time			50		

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		20	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		80	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 20\text{ A}, V_{GS} = 0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 20\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	-	370		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60\text{ V}$	-	5.8		μC
I_{RRM}	Reverse recovery current	(see Figure 16)	-	31.6		A
t_{rr}	Reverse recovery time	$I_{SD} = 20\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	-	450		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60\text{ V}, T_j = 150\text{ }^\circ\text{C}$	-	7.5		μC
I_{RRM}	Reverse recovery current	(see Figure 16)	-	32.5		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

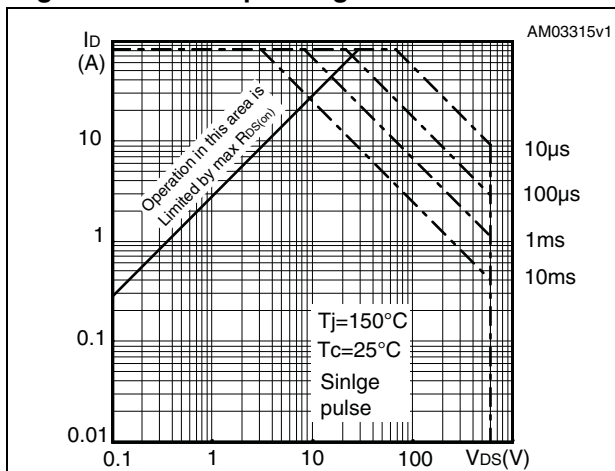


Figure 3. Thermal impedance

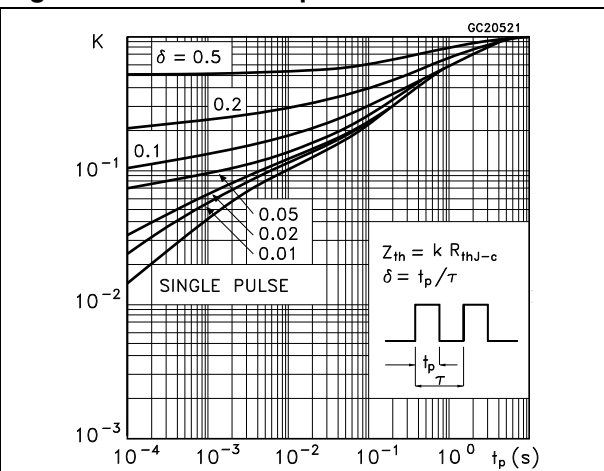


Figure 4. Output characteristics

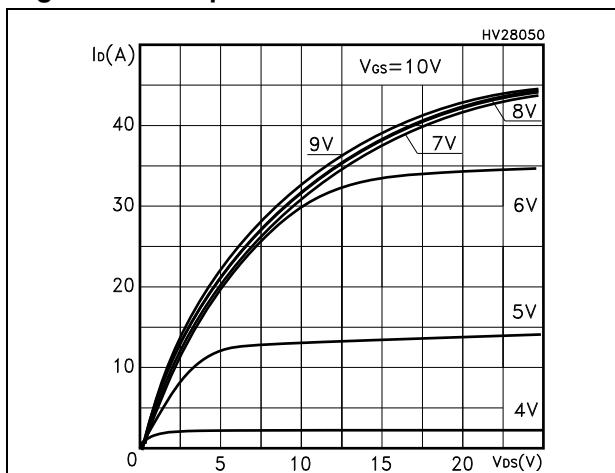


Figure 5. Transfer characteristics

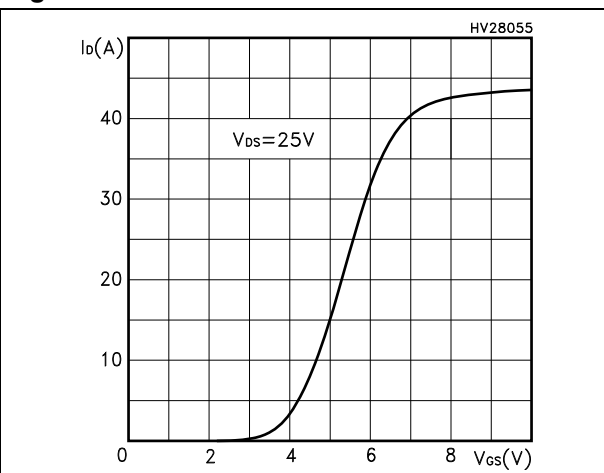


Figure 6. Transconductance

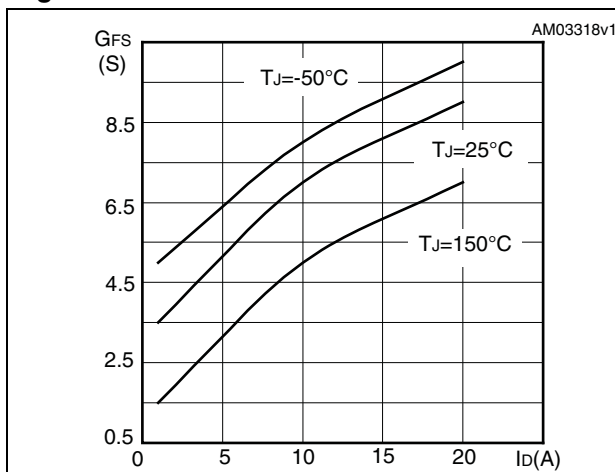


Figure 7. Static drain-source on-resistance

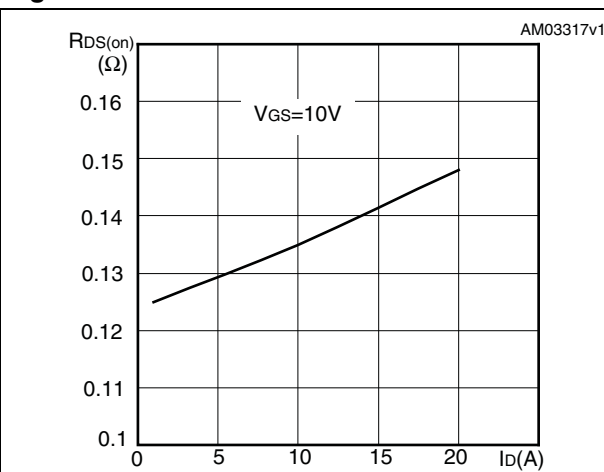


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

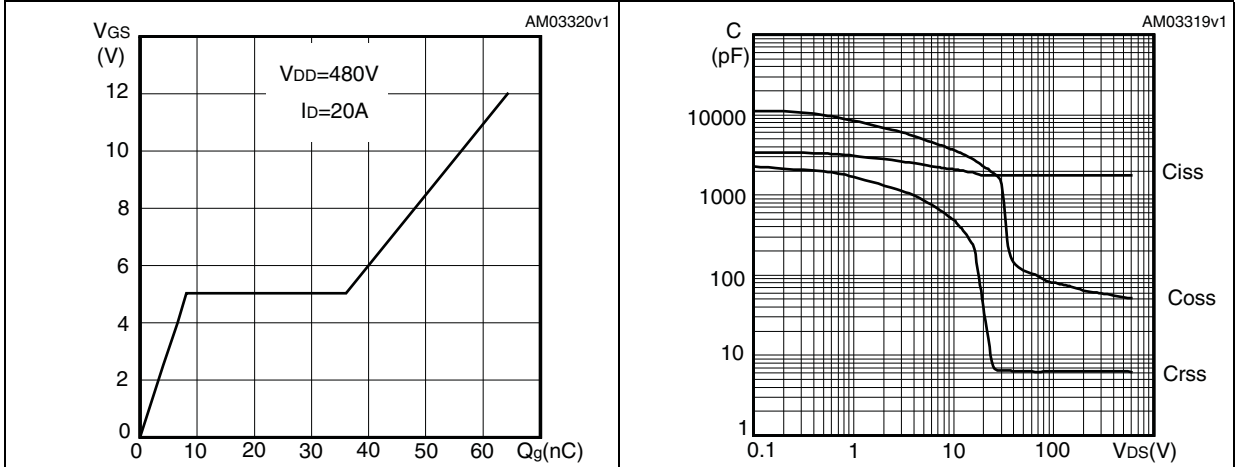


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

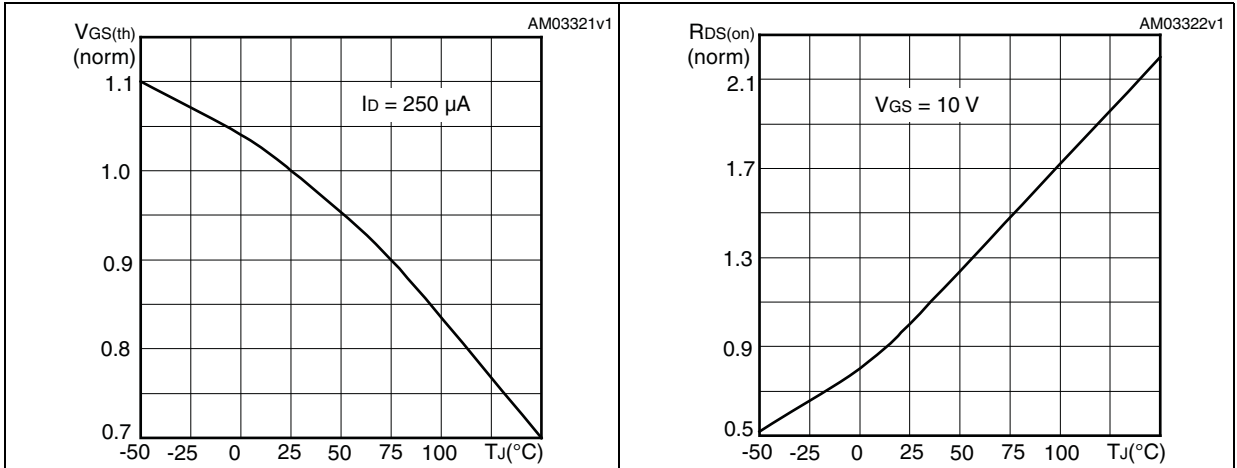
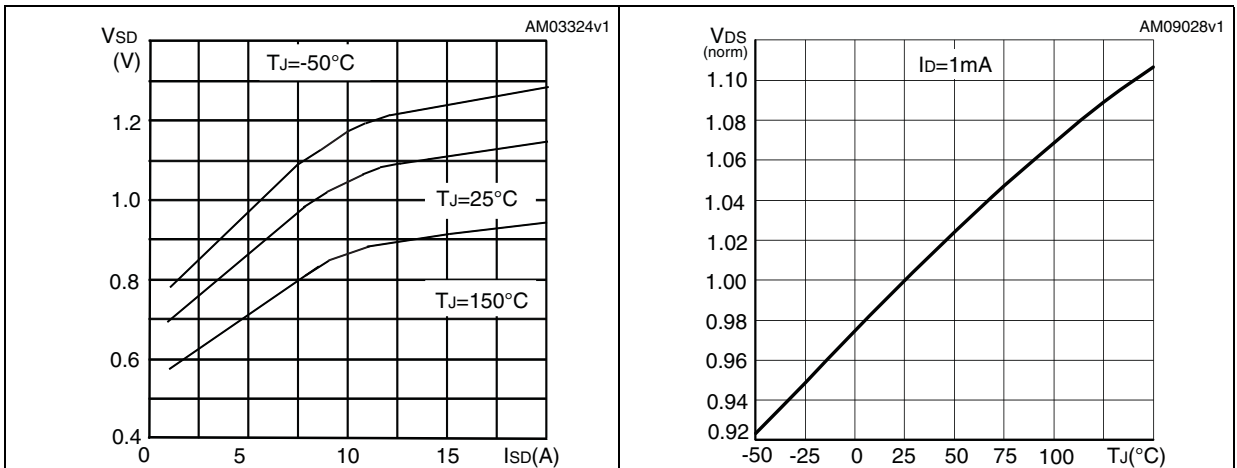
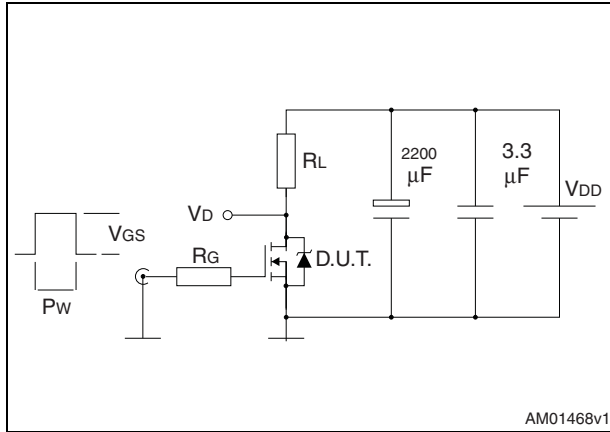


Figure 12. Source-drain diode forward characteristics Figure 13. Normalized V_{DS} vs temperature



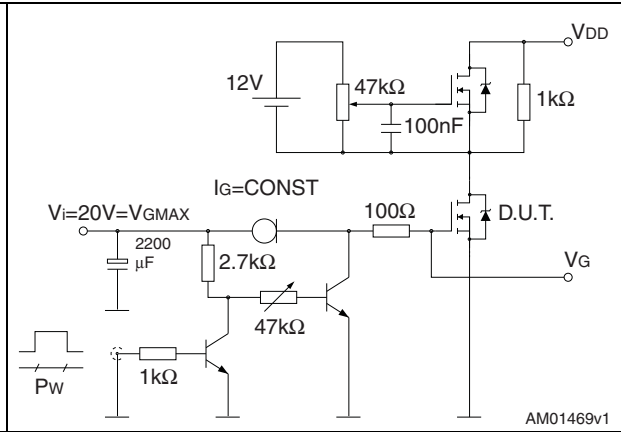
3 Test circuits

Figure 14. Switching times test circuit for resistive load



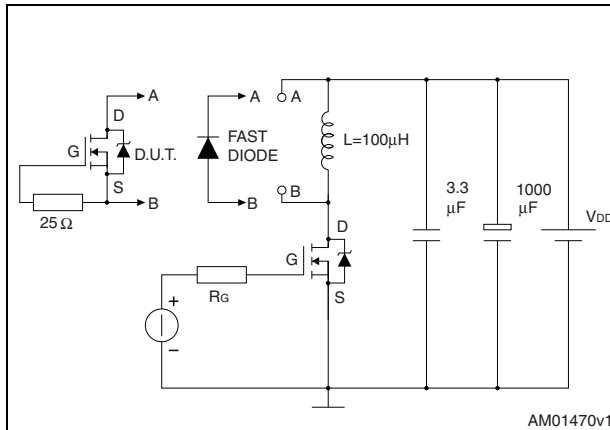
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Figure 15. Gate charge test circuit



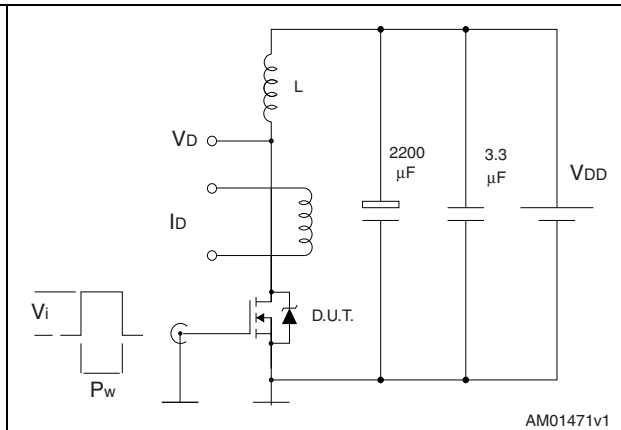
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Figure 16. Test circuit for inductive load switching and diode recovery times



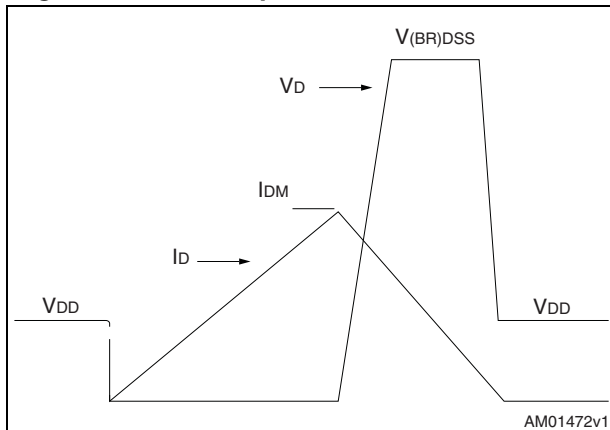
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Figure 17. Unclamped inductive load test circuit



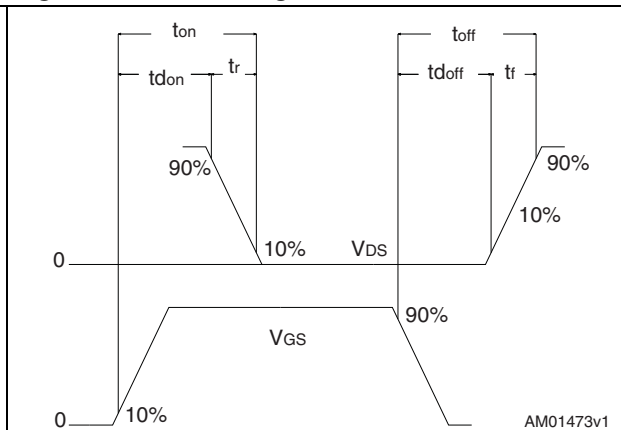
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Figure 18. Unclamped inductive waveform



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Figure 19. Switching time waveform



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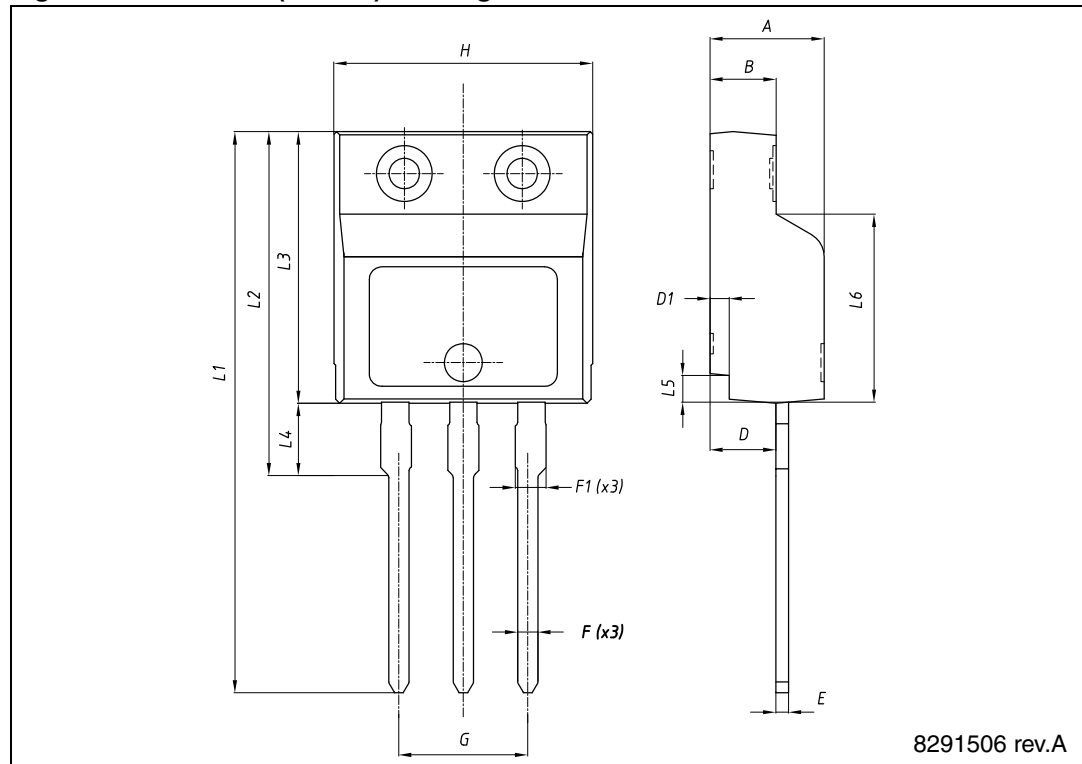
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 9. I²PAKFP (TO-281) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
D1	0.65		0.85
E	0.45		0.70
F	0.75		1.00
F1			1.20
G	4.95	-	5.20
H	10.00		10.40
L1	21.00		23.00
L2	13.20		14.10
L3	10.55		10.85
L4	2.70		3.20
L5	0.85		1.25
L6	7.30		7.50

Figure 20. I²PAKFP (TO-281) drawing



5 Revision history

Table 10. Document revision history

Date	Revision	Changes
15-Nov-2011	1	First release.
04-Jun-2012	2	Document status promoted from preliminary data to production data. Updated P_{TOT} and derating factor values in Table 2: Absolute maximum ratings ; $R_{th-case}$ value in Table 3: Thermal data Package name has been updated.

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