



STFI20NK50Z

N-channel 500 V, 0.23 Ω , 17 A Zener-protected SuperMESH™ Power MOSFET in I²PAKFP package

Datasheet — production data

Features

Type	V _{DSS}	R _{DS(on) max}	I _D	P _{TOT}
STFI20NK50Z	500 V	< 0.27 Ω	17 A	40 W

- Fully insulated and low profile package with increased creepage path from pin to heatsink plate
- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized

Applications

- Switching applications

Description

This device is an N-channel Zener-protected Power MOSFET developed using STMicroelectronics' SuperMESH™ technology, achieved through optimization of ST's well-established strip-based PowerMESH™ layout. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.

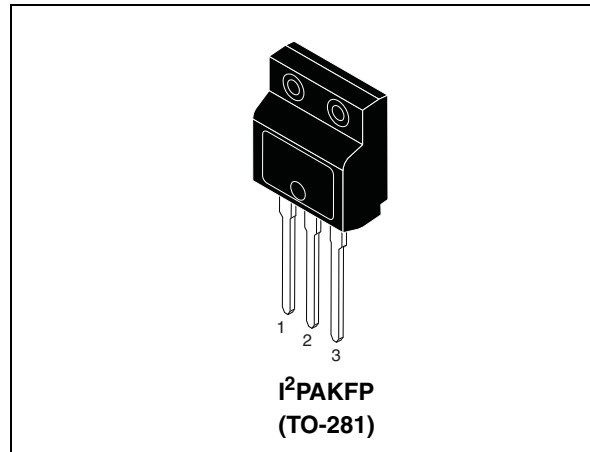


Figure 1. Internal schematic diagram

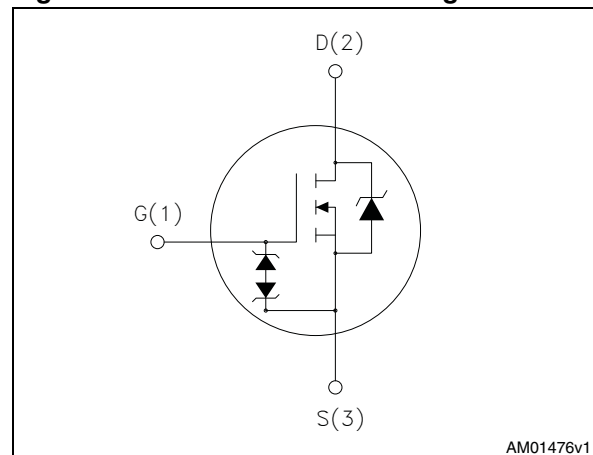


Table 1. Device summary

Order codes	Marking	Package	Packaging
STFI20NK50Z	20NK50Z	I ² PAKFP (TO-281)	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	500	V
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	17 ⁽¹⁾	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	10.71 ⁽¹⁾	A
$I_{DM}^{(2)}$	Drain current (pulsed)	68	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	40	W
ESD	Gate-source human body model ($R=1,5\text{ k}\Omega$, $C=100\text{ pF}$)	6	kV
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1\text{ s}$; $T_C = 25\text{ }^\circ\text{C}$)	2500	V
$dv/dt^{(3)}$	Peak diode recovery voltage slope	4.5	V/ns
T_{stg}	Storage temperature	-55 to 150	$^\circ\text{C}$
T_j	Max operating junction temperature	150	$^\circ\text{C}$

1. Limited by maximum junction temperature.
2. Pulse width limited by safe operating area.
3. $I_{SD} < 17\text{ A}$, $di/dt < 200\text{ A}/\mu\text{s}$, $V_{DD} = 80\% V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	3.1	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	$^\circ\text{C}/\text{W}$

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
$I_{AR}^{(1)}$	Repetitive or non repetitive avalanche current	17	A
E_{AS}	Single pulse avalanche energy (starting $T_J=25\text{ }^\circ\text{C}$, $I_D=I_{AR}$, $V_{DD}=50\text{ V}$)	850	mJ

1. Limited by maximum junction temperature.

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage ($V_{GS} = 0$)	$I_D = 1\text{ mA}$	500			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 500\text{ V}$ $V_{DS} = 500\text{ V}, T_C = 125\text{ °C}$			1 50	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 100\text{ }\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}, I_D = 8.5\text{ A}$		0.23	0.27	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15\text{ V}, I_D = 8.5\text{ A}$	-	13		S
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}, f = 1\text{ MHz},$ $V_{GS} = 0$	-	2600		pF
C_{oss}	Output capacitance			328		pF
C_{rss}	Reverse transfer capacitance			72		pF
$C_{oss\text{ eq.}}^{(2)}$	Equivalent output capacitance	$V_{DS} = 0, V_{DS} = 0\text{ to }640\text{ V}$	-	187		pF
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 250\text{ V}, I_D = 8.5\text{ A},$ $R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$ (see Figure 15)	-	28		ns
t_r	Rise time			20		ns
$t_{d(off)}$	Turn-off delay time			70		ns
t_f	Fall time			15		ns
Q_g	Total gate charge	$V_{DD} = 400\text{ V}, I_D = 17\text{ A},$ $V_{GS} = 10\text{ V}$ (see Figure 16)	-	85	119	nC
Q_{gs}	Gate-source charge			15.5		nC
Q_{gd}	Gate-drain charge			42		nC

1. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		17	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		68	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 17 \text{ A}, V_{GS} = 0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 17 \text{ A},$ $di/dt = 100 \text{ A}/\mu\text{s}$ $V_R = 100 \text{ V}$ (see Figure 17)	-	355		ns
Q_{rr}	Reverse recovery charge			3.90		μC
I_{RRM}	Reverse recovery current			22		A
t_{rr}	Reverse recovery time	$I_{SD} = 17 \text{ A},$ $di/dt = 100 \text{ A}/\mu\text{s}$ $V_R = 100 \text{ V}, T_j = 150 \text{ }^\circ\text{C}$ (see Figure 17)	-	440		ns
Q_{rr}	Reverse recovery charge			5.72		μC
I_{RRM}	Reverse recovery current			26		A

1. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2. Pulse width limited by safe operating area.

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage ($I_D = 0$)	$I_{GS} = \pm 1 \text{ mA}$	30	-		V

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

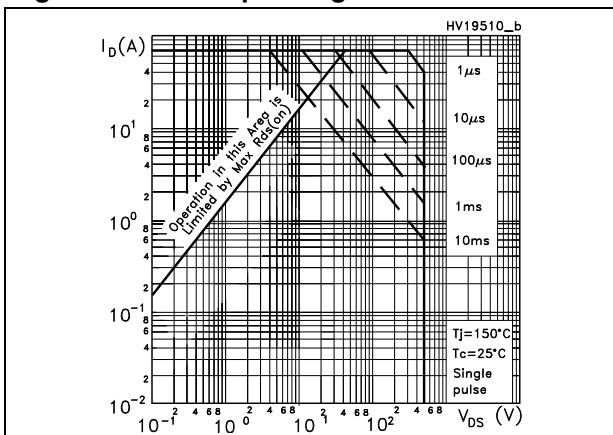


Figure 3. Thermal impedance

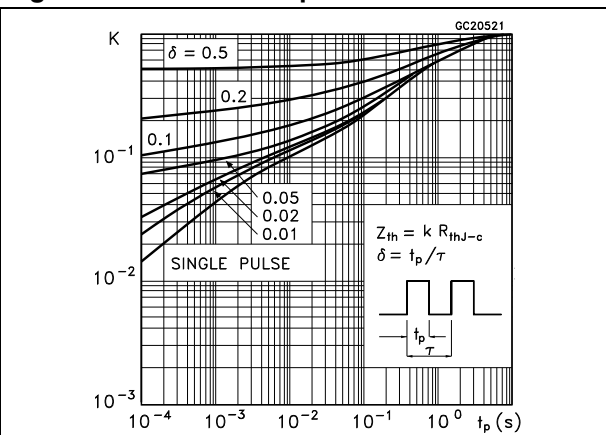


Figure 4. Output characteristics

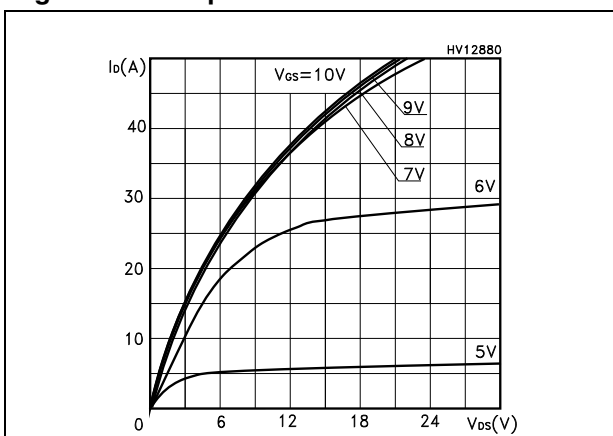


Figure 5. Transfer characteristics

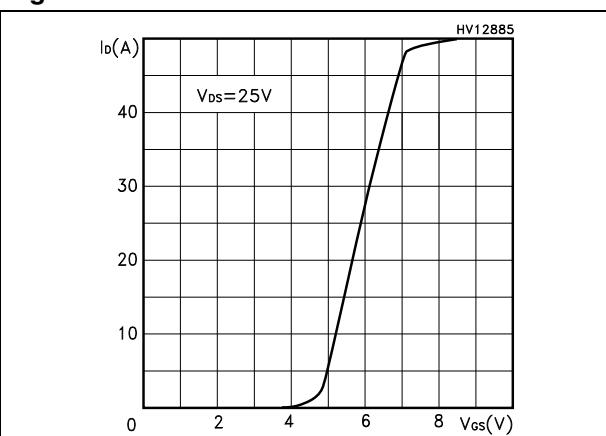


Figure 6. Transconductance

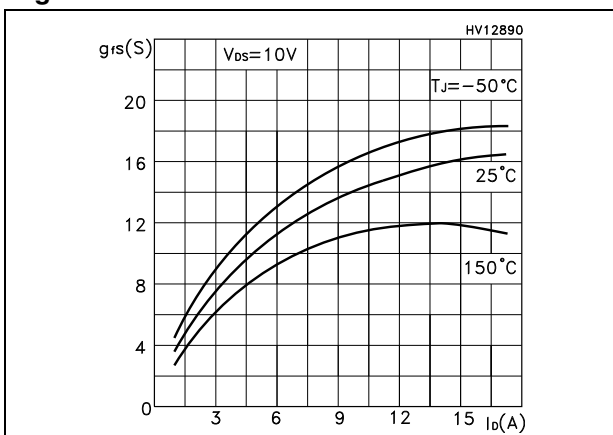


Figure 7. Static drain-source on resistance

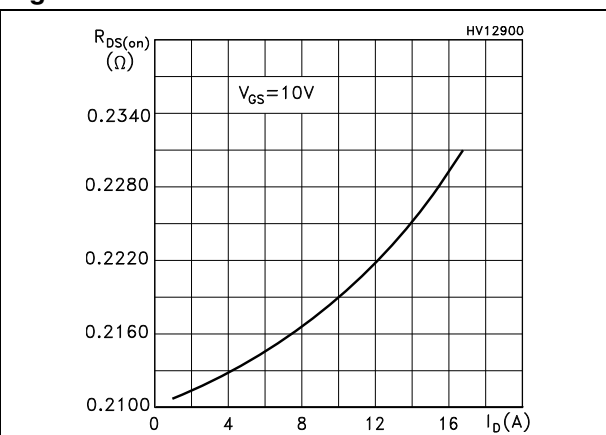


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

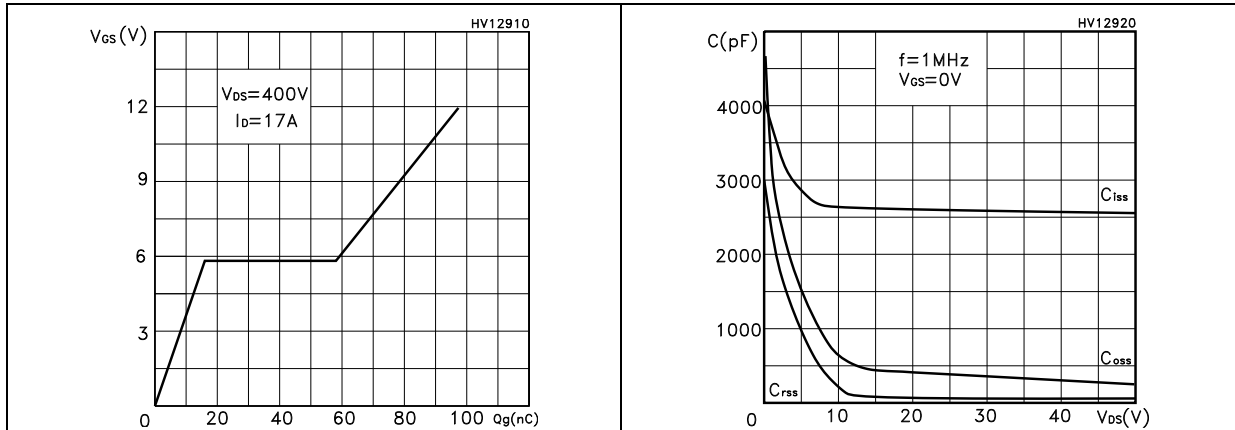


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

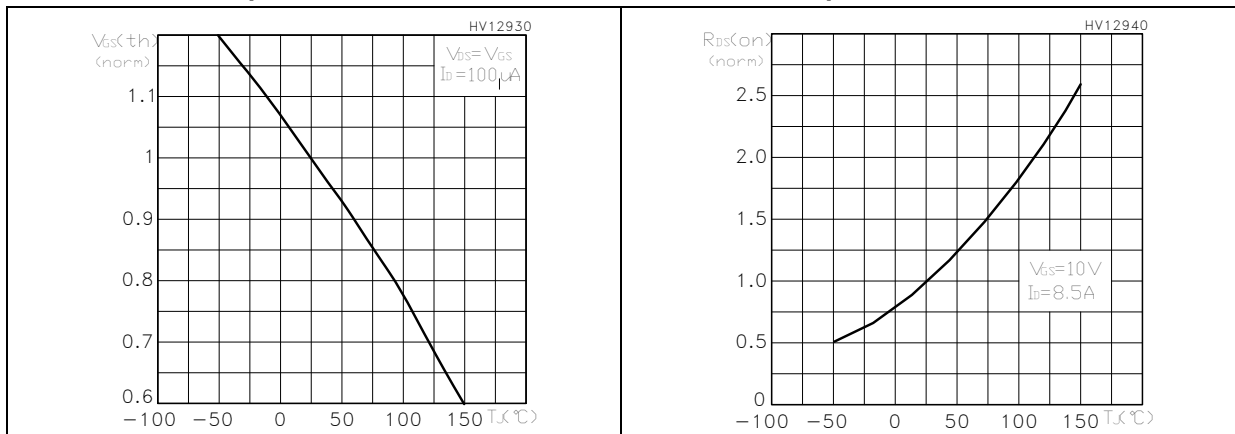


Figure 12. Maximum avalanche energy vs temperature Figure 13. Normalized B_{VDSS} vs temperature

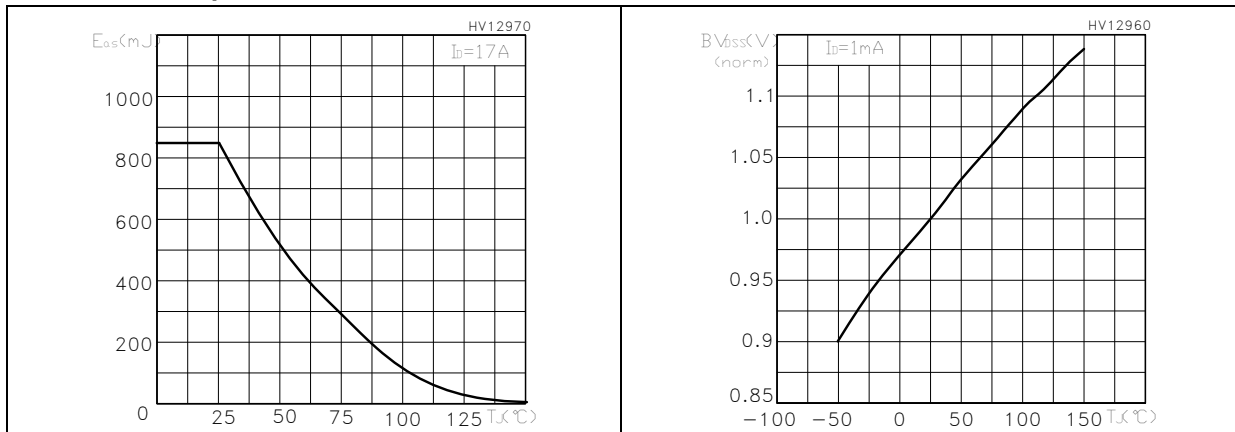
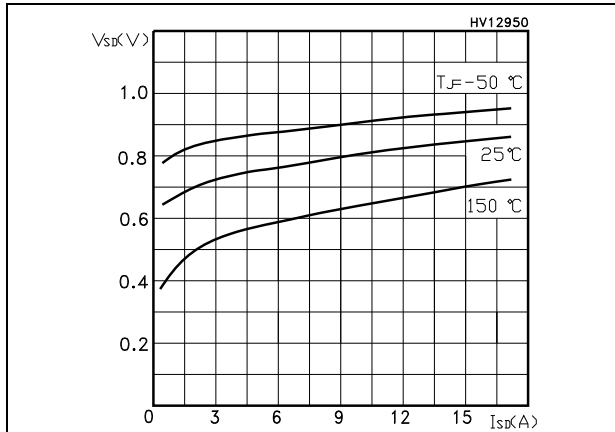


Figure 14. Source-drain diode forward characteristic



3 Test circuits

Figure 15. Switching times test circuit for resistive load

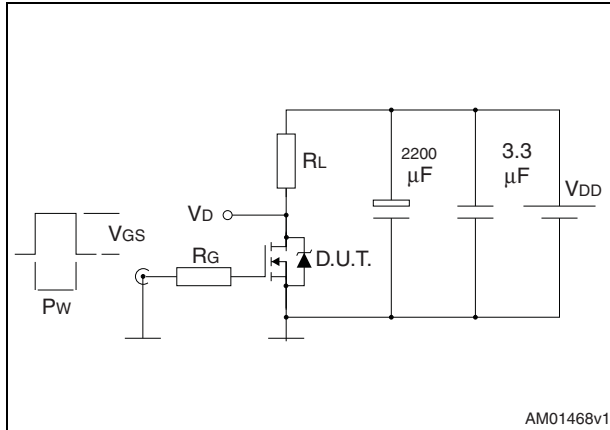


Figure 16. Gate charge test circuit

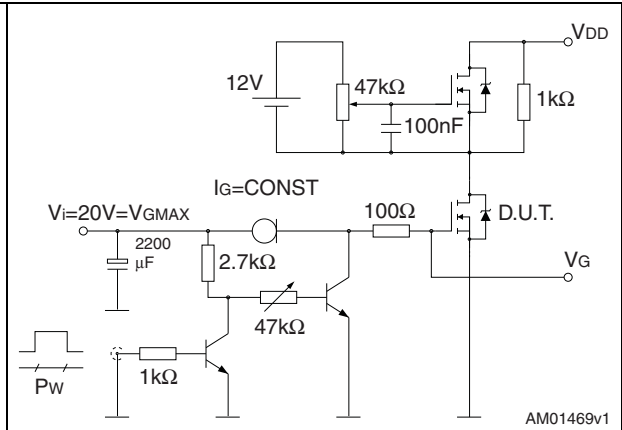


Figure 17. Test circuit for inductive load switching and diode recovery times

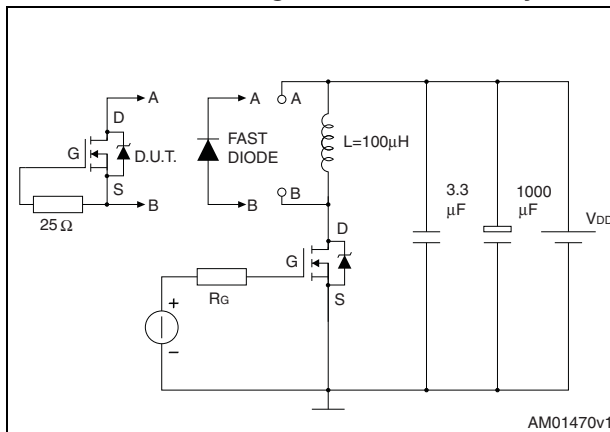


Figure 18. Unclamped inductive load test circuit

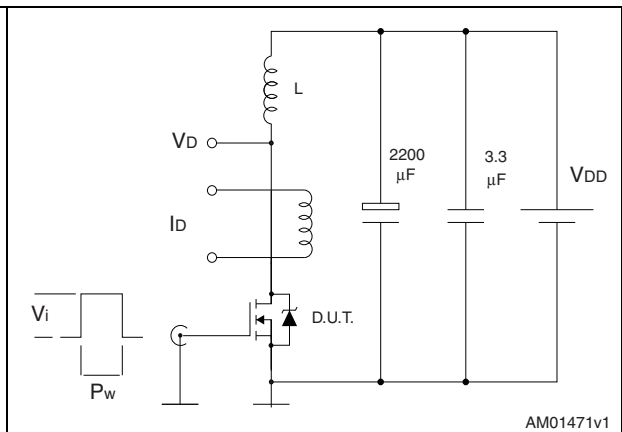


Figure 19. Unclamped inductive waveform

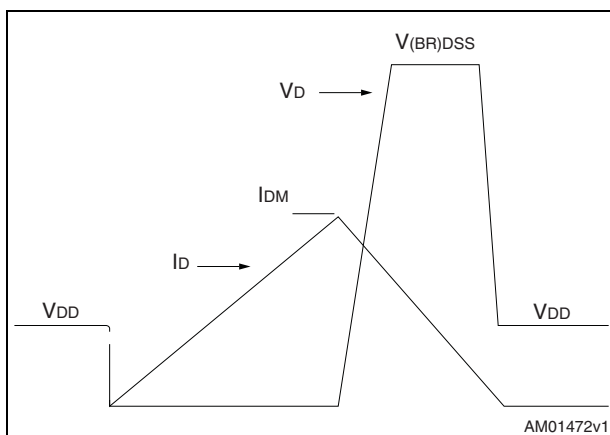
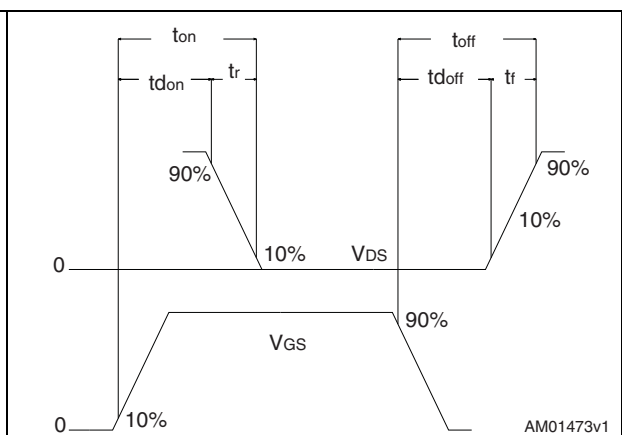


Figure 20. Switching time waveform



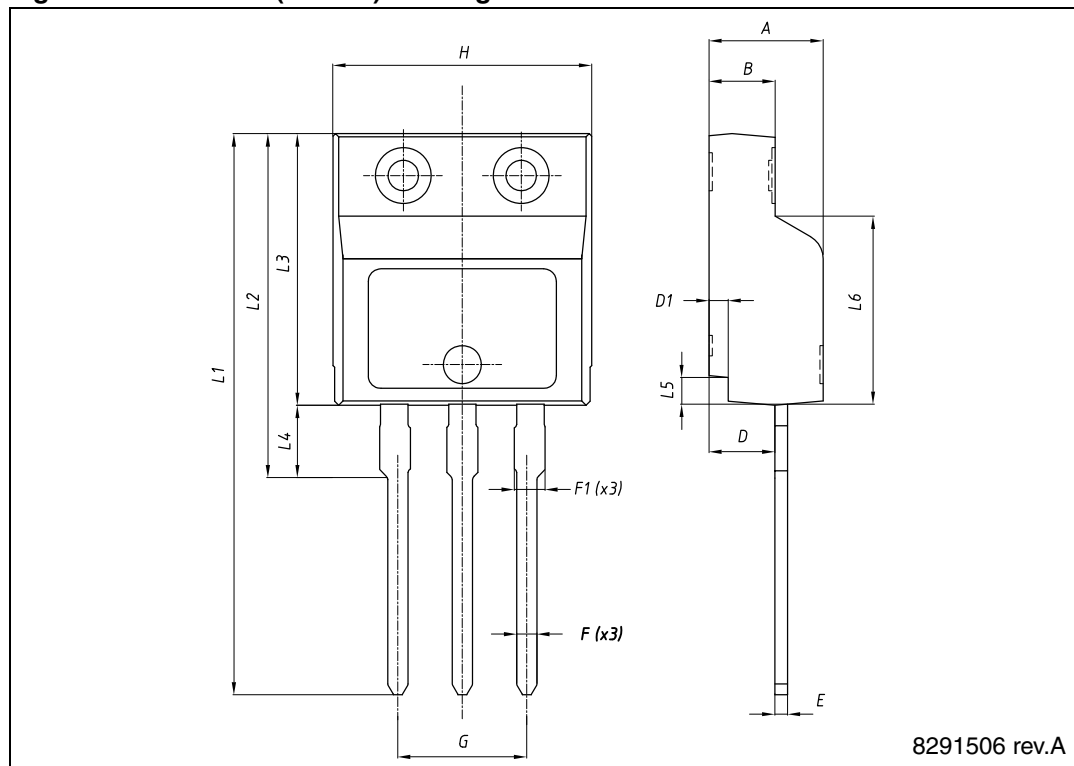
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 9. I²PAKFP (TO-281) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
D1	0.65		0.85
E	0.45		0.70
F	0.75		1.00
F1			1.20
G	4.95	-	5.20
H	10.00		10.40
L1	21.00		23.00
L2	13.20		14.10
L3	10.55		10.85
L4	2.70		3.20
L5	0.85		1.25
L6	7.30		7.50

Figure 21. I²PAKFP (TO-281) drawing



5 Revision history

Table 10. Document revision history

Date	Revision	Changes
01-Jul-2011	1	First release.
11-Nov-2011	2	<i>Figure 2: Safe operating area</i> and <i>Figure 3: Thermal impedance</i> have been added.
20-Mar-2012	3	Document status promoted from preliminary data to production data. The package name has been updated.

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