



# STP180NS04ZC

N-channel clamped 3.5 mΩ - 120 A TO-220  
fully protected SAFeFET™ Power MOSFET

## Features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STP180NS04ZC	Clamped	< 4.2 mΩ	120 A

- Low capacitance and gate charge
- 100% avalanche tested
- 175°C maximum junction temperature

## Applications

- Switching application

## Description

This fully clamped Power MOSFET is produced by using the latest advanced company's mesh OVERLAY process which is based on a novel strip layout. The inherent benefits of the new technology coupled with the extra clamping capabilities make this product particularly suitable for the harshest operation conditions such as those encountered in the automotive environment. Any other application requiring extra ruggedness is also recommended.

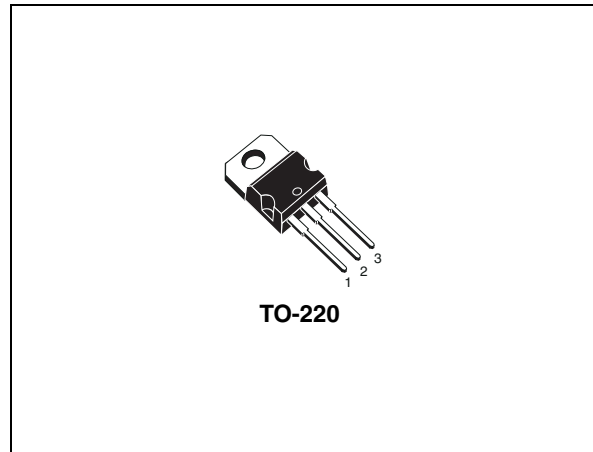


Figure 1. Internal schematic diagram

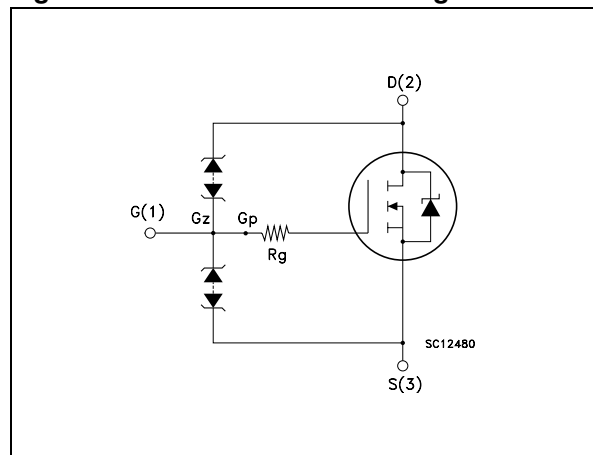


Table 1. Device summary

Order code	Marking	Package	Packaging
STP180NS04ZC	P180NS04ZC	TO-220	Tube

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	33 <sup>(1)</sup>	V
$V_{DG}$	Drain-gate voltage	33 <sup>(1)</sup>	V
$V_{GS}$	Gate-source voltage	$\pm 20$ <sup>(1)</sup>	V
$I_D$ <sup>(2)</sup>	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	120	A
$I_D$ <sup>(2)</sup>	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	120	A
$I_{DG}$	Drain gate current (continuous)	$\pm 50$	mA
$I_{GS}$	Gate-source current (continuous)	$\pm 50$	mA
$I_{DM}$ <sup>(3)</sup>	Drain current (pulsed)	480	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	300	W
	Derating factor	2	W/ $^\circ\text{C}$
$V_{ESD(G-S)}$	Gate-source ESD (HBM-C=100 pF, R=1.5 k $\Omega$ )	$\pm 8$	kV
$V_{ESD(G-D)}$	Gate-drain ESD (HBM-C=100 pF, R=1.5 k $\Omega$ )	$\pm 8$	kV
$V_{ESD(D-S)}$	Drain-source ESD (HBM-C=100 pF, R=1.5 k $\Omega$ )	$\pm 8$	kV
$T_J$	Operating junction temperature	-55 to 175	$^\circ\text{C}$
$T_{stg}$	Storage temperature		

1. Voltage is limited by zener diodes
2. Current limited by wire bonding
3. Pulse width limited by safe operating area

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.50	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	$^\circ\text{C}/\text{W}$
$T_I$	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}$

**Table 4. Avalanche data**

Symbol	Parameter	Value	Unit
$I_{AS}$	Avalanche current, repetitive or not repetitive (pulse width limited by $T_{jmax}$ $\delta < 1\%$ )	80	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$ , $I_D = I_{AS}$ , $V_{DD} = 21\text{ V}$ ) (see Figure 17, Figure 14.)	1000	mJ

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}\text{C}$  unless otherwise specified)

**Table 5. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DG}$	Clamped voltage	$I_D = 1 \text{ mA}$ , $V_{GS} = 0$ $-40 < T_j < 175^{\circ}\text{C}$	33		41	V
$V_{DSR(CL)}$	Drain-source clamping voltage (DC)	$I_{GS(CL)} = -2 \text{ mA}$ , $I_D = 1 \text{ A}$		41		V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 16 \text{ V}$ $V_{DS} = 16 \text{ V}$ , $T_j = 150^{\circ}\text{C}$ $V_{DS} = 16 \text{ V}$ , $T_j = 175^{\circ}\text{C}$			1 50 100	$\mu\text{A}$ $\mu\text{A}$ $\mu\text{A}$
$I_{GSS}^{(1)}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 10 \text{ V}$ $V_{GS} = \pm 10 \text{ V}$ , $T_j = 175^{\circ}\text{C}$ $V_{GS} = \pm 16 \text{ V}$ , $T_j = 175^{\circ}\text{C}$			2 50 150	$\mu\text{A}$ $\mu\text{A}$ $\mu\text{A}$
$V_{GSS}$	Gate-source breakdown voltage	$I_{GS} = \pm 100 \mu\text{A}$	18		25	V
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 1 \text{ mA}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10 \text{ V}$ , $I_D = 40 \text{ A}$		3.5	4.2	$\text{m}\Omega$
$R_G$	Internal gate resistor			14		$\Omega$

1. Gate Oxide, without zener diodes, tested at wafer sorting ( $I_{GSS} < \pm 100 \text{ nA}$  @  $\pm 20 \text{ V}$   $T_j=25^{\circ}$ ). [Figure 17.: Unclamped Inductive load test circuit](#) for electrical schematics

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15 \text{ V}$ , $I_D = 40 \text{ A}$		95		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25 \text{ V}$ , $f = 1 \text{ MHz}$ , $V_{GS} = 0$		4560 1700 550		pF pF pF
$t_{r(Voff)}$ $t_f$ $t_c$	Off voltage rise time Fall time Cross-over time	$V_{CLAMP} = 30 \text{ V}$ , $I_D = 80 \text{ A}$ , $V_{GS} = 10 \text{ V}$ , $R_G = 4.7 \Omega$ <a href="#">(see Figure 16)</a>		250 115 290		ns ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 20 \text{ V}$ , $I_D = 120 \text{ A}$ $V_{GS} = 10 \text{ V}$ <a href="#">(see Figure 15)</a>		110 29 40		nC nC nC

1. Pulsed: pulse duration=300 $\mu\text{s}$ , duty cycle 1.5%

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current				120	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				480	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=120\text{ A}$ , $V_{GS}=0$			1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD}=120\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,		56		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD}=32\text{ V}$ , $T_j=150\text{ }^\circ\text{C}$		70		nC
$I_{RRM}$	Reverse recovery current	(see Figure 16)		12		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

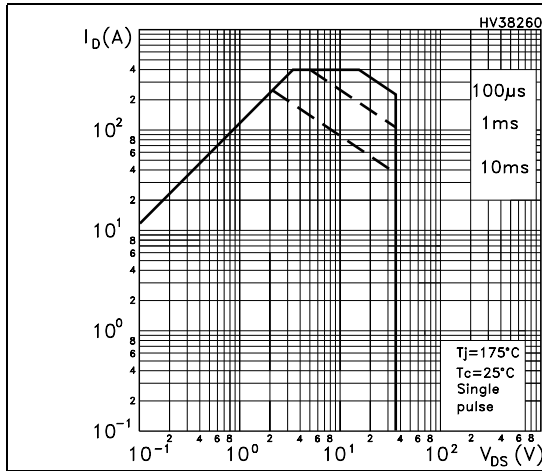


Figure 3. Thermal impedance

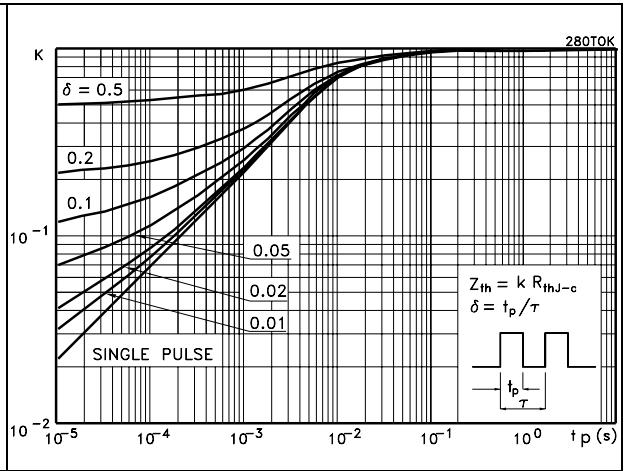


Figure 4. Output characteristics

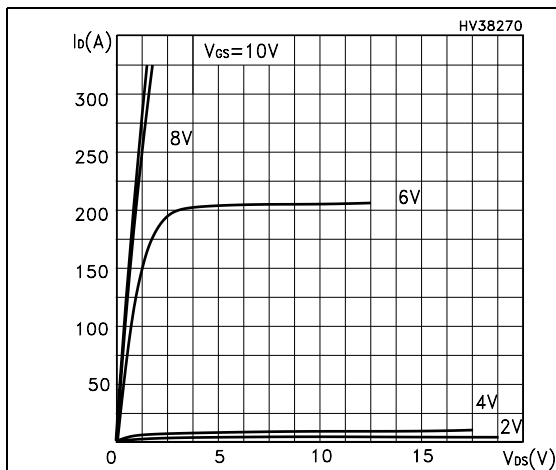


Figure 5. Transfer characteristics

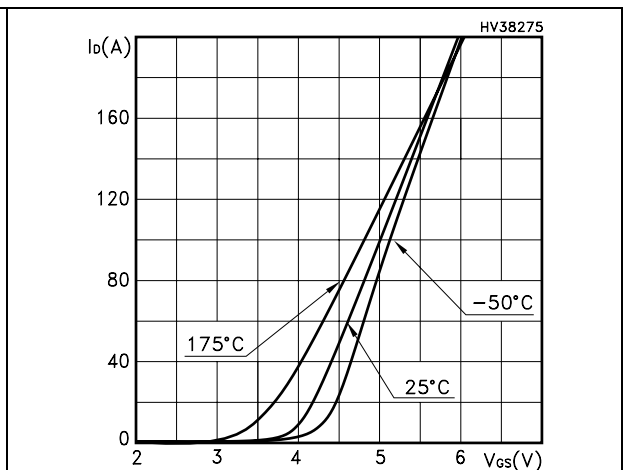


Figure 6. Transconductance

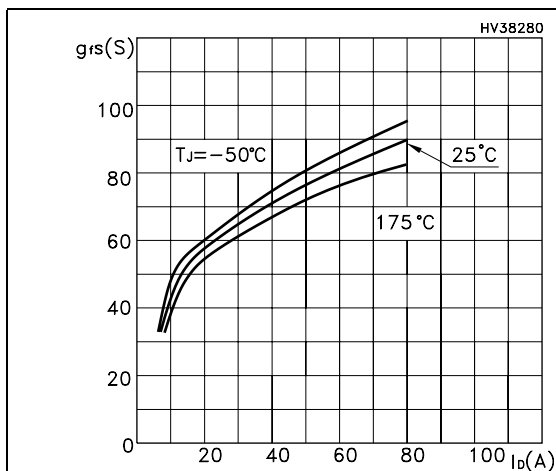


Figure 7. Static drain-source on resistance

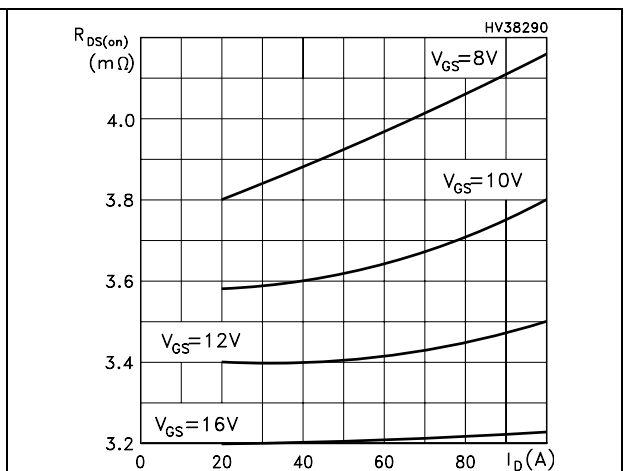


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

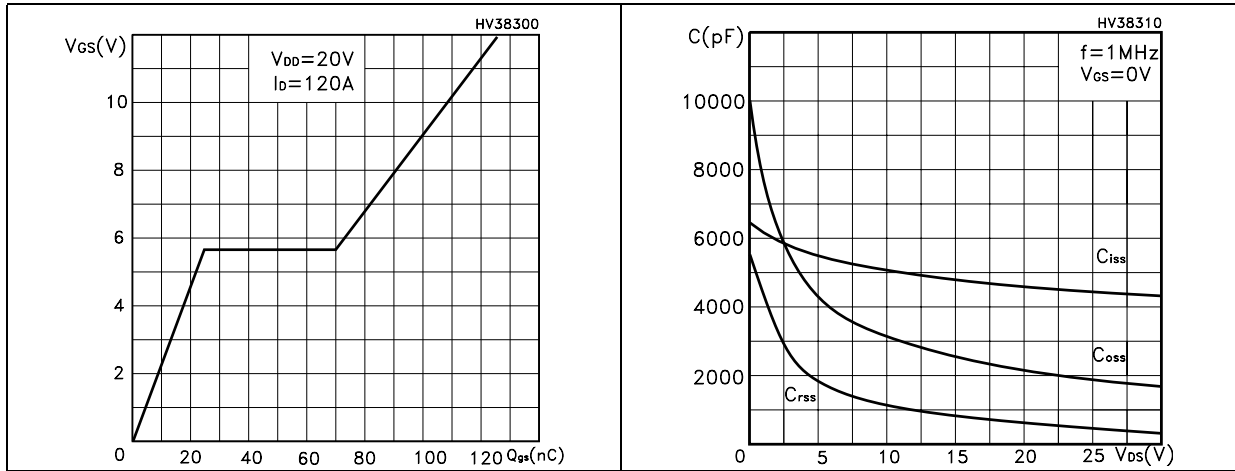


Figure 10. Normalized gate threshold voltage vs temperature

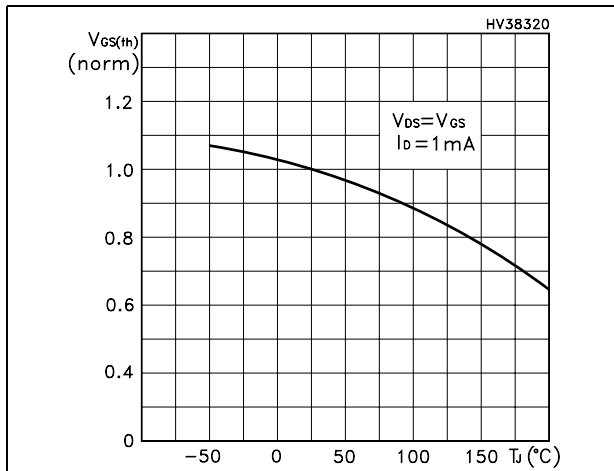


Figure 11. Normalized on resistance vs temperature

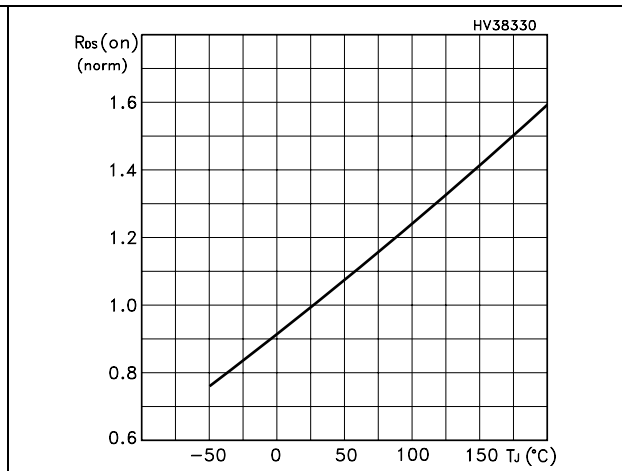


Figure 12. Source-drain diode forward characteristics

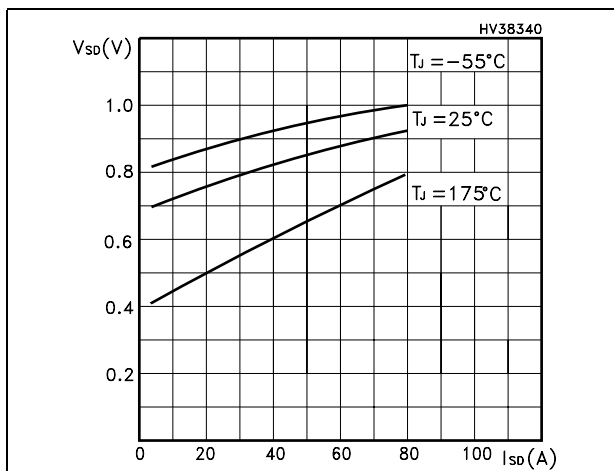
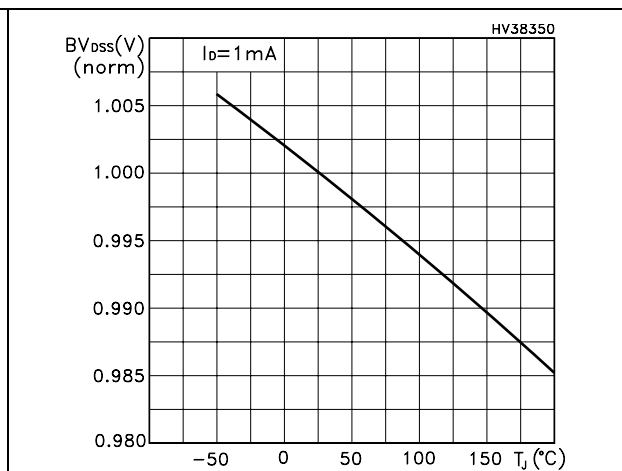


Figure 13. Normalized  $BV_{DSS}$  vs temperature



### 3 Test circuit

Figure 14. Unclamped inductive waveform

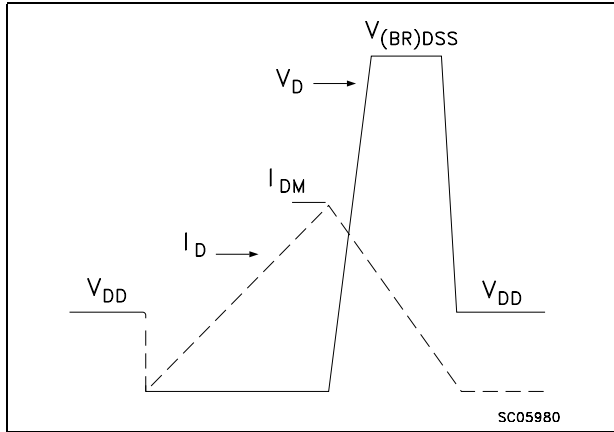


Figure 15. Gate charge test circuit

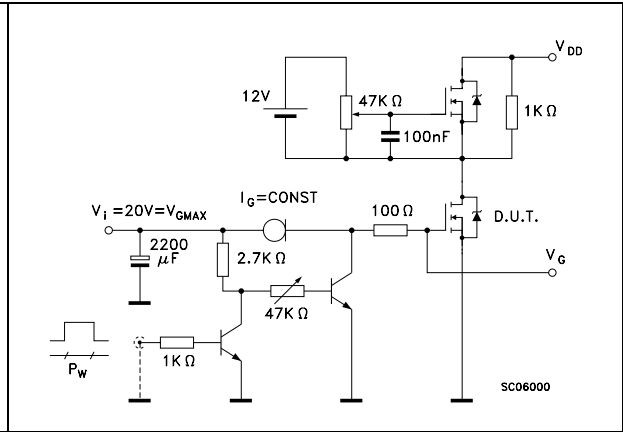


Figure 16. Test circuit for inductive load switching and diode recovery times

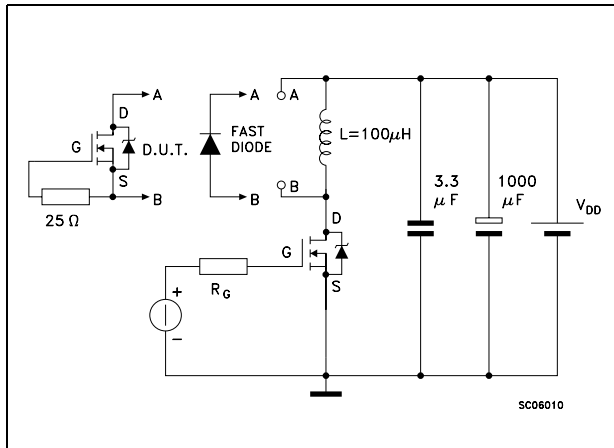
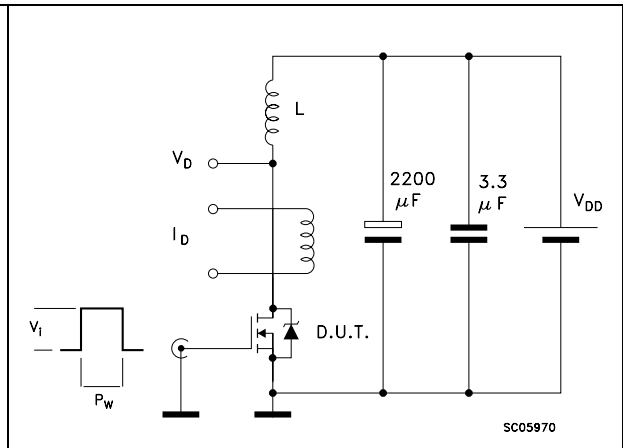


Figure 17. Unclamped Inductive load test circuit



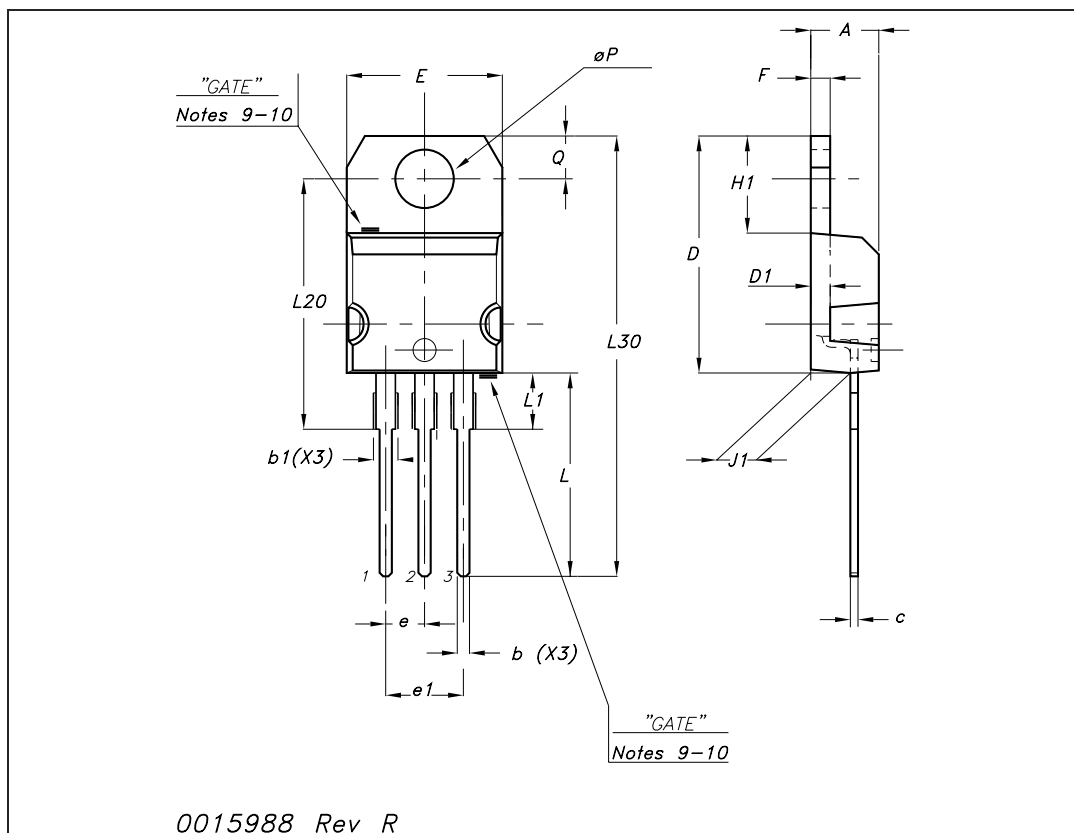


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

TO-220 mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.48		0.70	0.019		0.027
D	15.25		15.75	0.6		0.62
D1		1.27			0.050	
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.051
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
∅P	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



## 5 Revision history

**Table 8. Document revision history**

Date	Revision	Changes
03-Apr-2008	1	First release

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