



# STP30NF20 STW30NF20

N-channel 200V - 0.065Ω - 30A - TO-220/TO-247  
Low gate charge STripFET™ Power MOSFET

## General features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>	P <sub>TOT</sub>
STP30NF20	200V	0.075Ω	30A	125W
STW30NF20	200V	0.075Ω	30A	125W

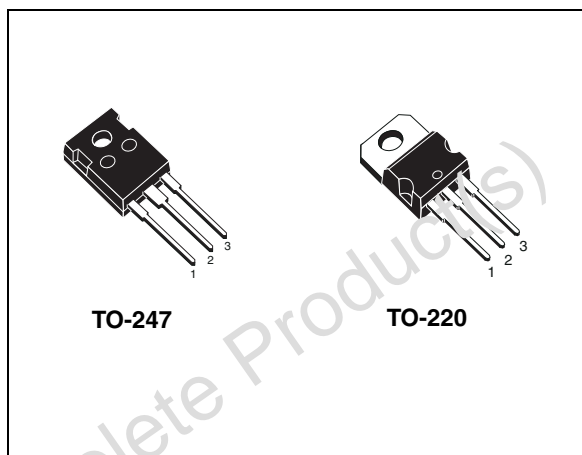
- Gate charge minimized
- 100% avalanche tested
- Excellent figure of merit (R<sub>DS</sub>\*Q<sub>g</sub>)
- Very good manufacturing repeatability
- Very low intrinsic capacitances

## Description

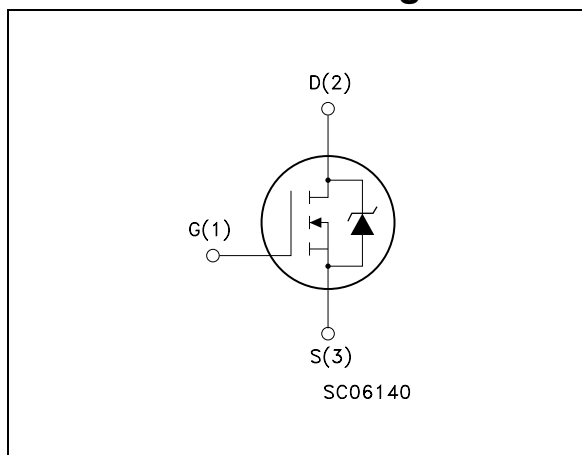
This Power MOSFET series realized with STMicroelectronics unique STripFET process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency isolated DC-DC converters.

## Applications

- Switching application



## Internal schematic diagram



## Order codes

Part number	Marking	Package	Packaging
STP30NF20	30NF20	TO-220	Tube
STW30NF20	30NF20	TO-247	Tube

# Contents

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# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	200	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	30	A
$I_D$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	19	A
$I_{DM}^{(1)}$	Drain current (pulsed)	120	A
$P_{TOT}$	Total dissipation at $T_C = 25^\circ\text{C}$	125	W
	Derating factor	1	W/ $^\circ\text{C}$
$dv/dt^{(2)}$	Peak diode recovery voltage slope	10	V/ns
$T_J$ $T_{stg}$	Operating junction temperature Storage temperature	-55 to 150	$^\circ\text{C}$
$T_l$	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}$

1. Pulse width limited by safe operating area

2.  $I_{SD} \leq 30\text{A}$ ,  $di/dt \leq 200\text{A}/\mu\text{s}$ ,  $V_{DD} = 80\%V_{(BR)DS}$

**Table 2. Thermal data**

Symbol	Parameter	TO-220	TO-247	Unit
$R_{thJC}$	Thermal resistance junction-case max	1		$^\circ\text{C}/\text{W}$
$R_{thJA}$	Thermal resistance junction-ambient max	62.5	50	$^\circ\text{C}/\text{W}$

**Table 3. Avalanche data**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not repetitive (pulse width limited by $T_{jmax}$ )	30	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{V}$ )	140	mJ

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}C$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1mA, V_{GS} = 0$	200			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating},$ $V_{DS} = \text{Max rating}, T_c = 125^{\circ}C$			1 10	$\mu A$ $\mu A$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20V$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 15A$		0.065	0.075	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15V, I_D = 15A$		20		S
$C_{iss}$	Input capacitance	$V_{DS} = 25V, f = 1\text{ MHz}, V_{GS} = 0$		1597		pF
$C_{oss}$	Output capacitance			320		pF
$C_{rss}$	Reverse transfer capacitance			43		pF
$Q_g$	Total gate charge	$V_{DD} = 160V, I_D = 30A$		38		nC
$Q_{gs}$	Gate-source charge	$V_{GS} = 10V$		8		nC
$Q_{gd}$	Gate-drain charge	(see Figure 16)		18		nC

1. Pulsed: pulse duration=300 $\mu s$ , duty cycle 1.5%

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on delay time Rise time	$V_{DD}=100V$ , $I_D=15A$ , $R_G=4.7\Omega$ , $V_{GS}=10V$ (see Figure 15)		35 15.7		ns ns
$t_{d(off)}$ $t_f$	Turn-off delay time Fall time	$V_{DD}=100V$ , $I_D=15A$ , $R_G=4.7\Omega$ , $V_{GS}=10V$ (see Figure 15)		38 8.8		ns ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM}^{(1)}$	Source-drain current Source-drain current (pulsed)				30 120	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=30A$ , $V_{GS}=0$			1.5	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=30A$ , $di/dt = 100A/\mu s$ , $V_{Dn}=100V$ , $T_j=25^\circ C$		155 0.96 12.4		ns $\mu C$ A
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=30A$ , $di/dt = 100A/\mu s$ , $V_{DD}=100V$ , $T_j=150^\circ C$		194 1.42 14.6		ns $\mu C$ A

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration=300 $\mu s$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for TO-247

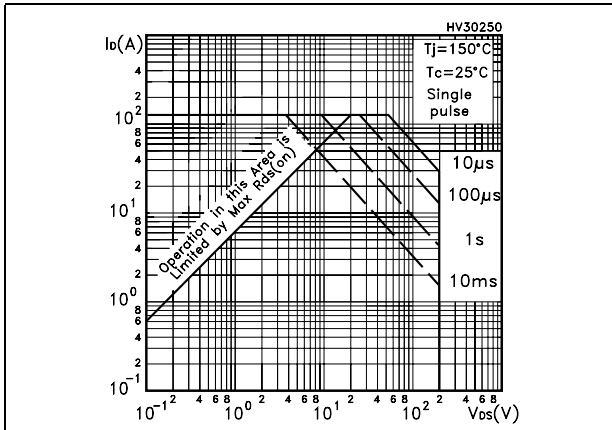


Figure 2. Thermal impedance for TO-247

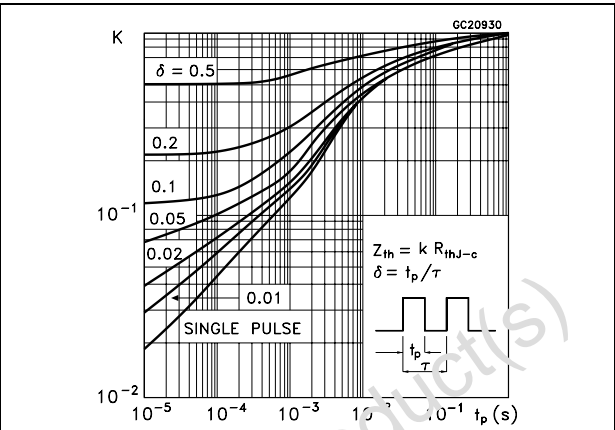


Figure 3. Safe operating area for TO-220

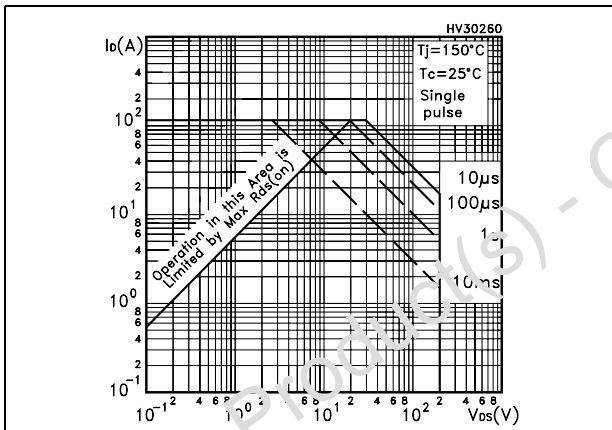


Figure 4. Thermal impedance for TO-220

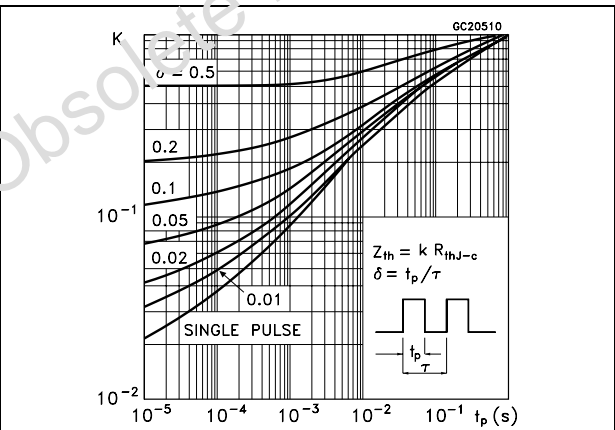


Figure 5. Output characteristics

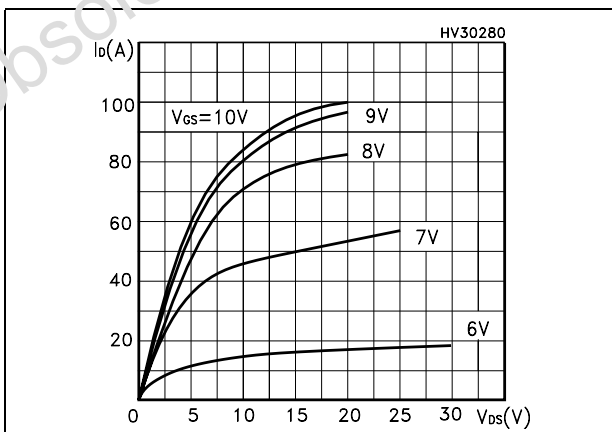


Figure 6. Transfer characteristics

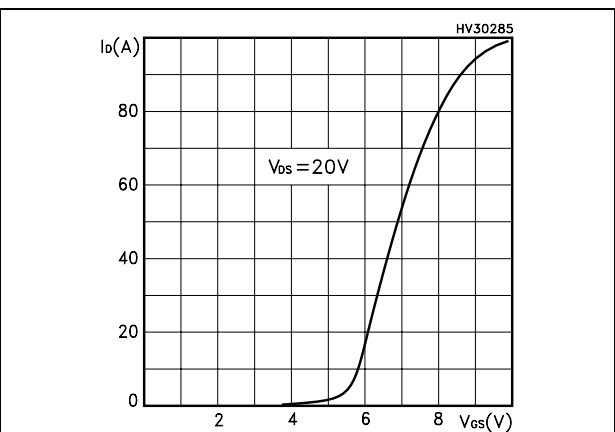


Figure 7. Normalized  $B_{V_{DS}}$  vs temperature

Figure 8. Static drain-source on resistance

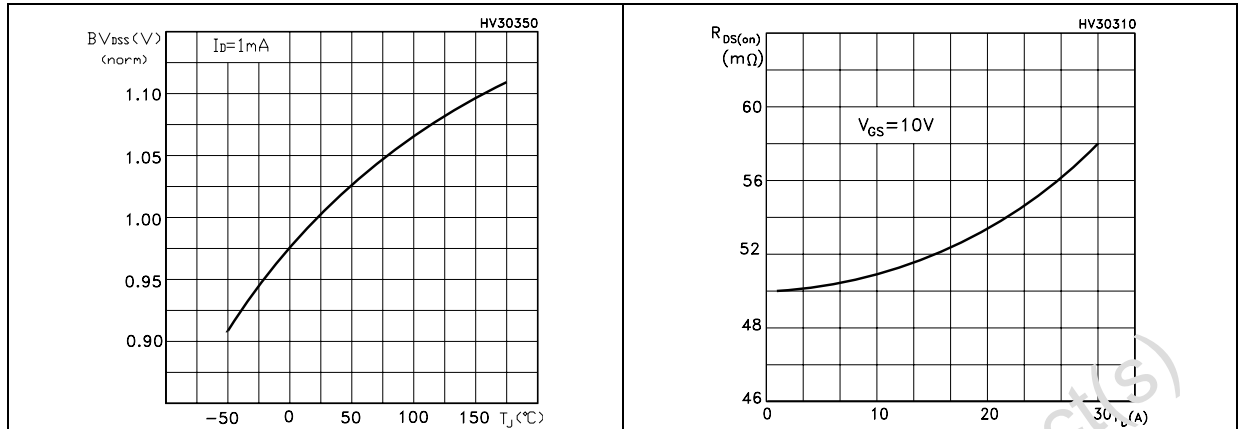


Figure 9. Gate charge vs gate-source voltage

Figure 10. Capacitance variations

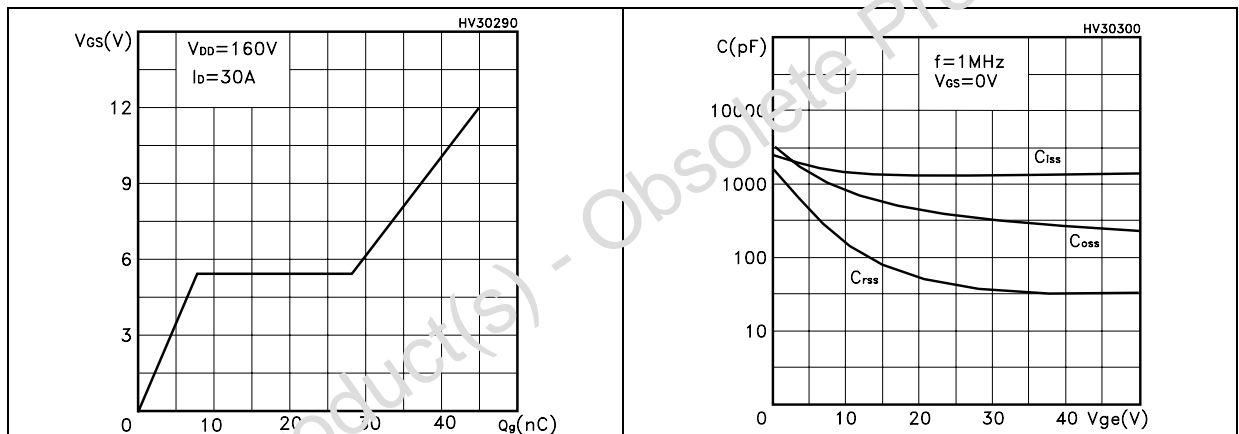


Figure 11. Normalized gate threshold voltage vs temperature

Figure 12. Normalized on resistance vs temperature

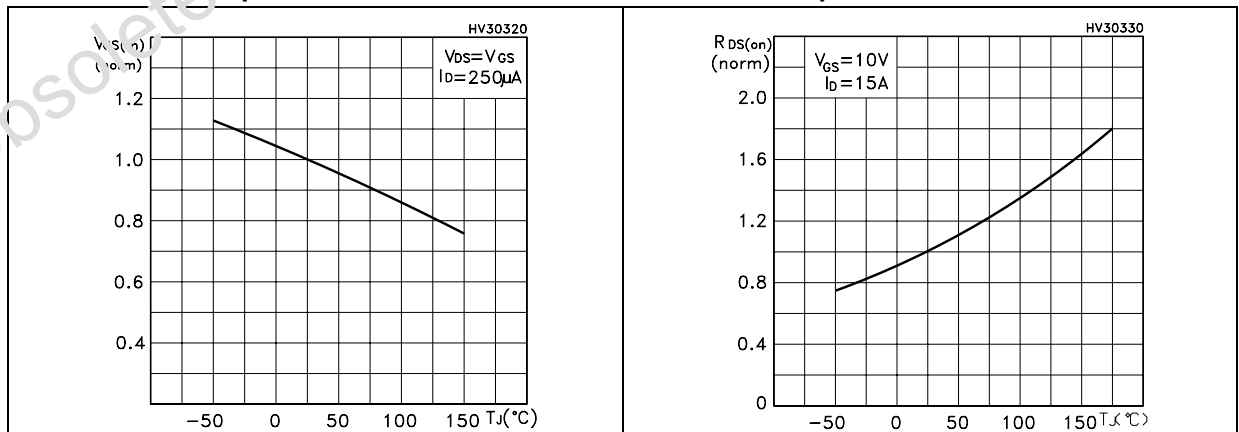


Figure 13. Source-drain diode forward characteristics

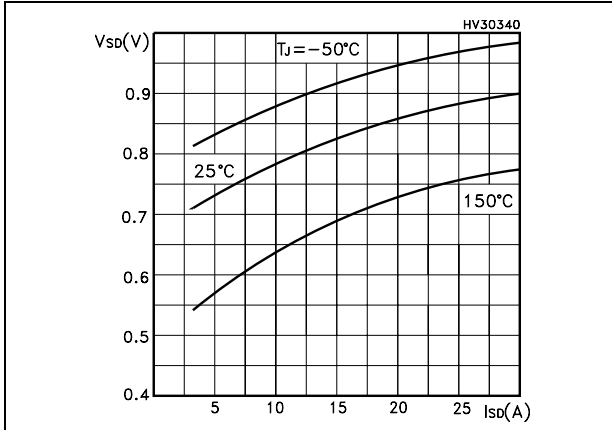
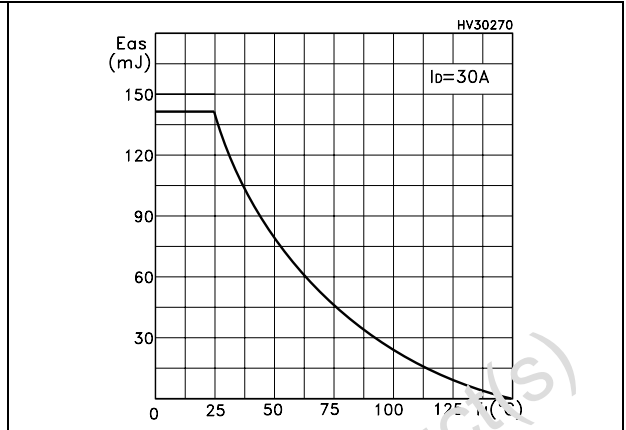


Figure 14. Maximum avalanche energy vs temperature



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### 3 Test circuit

Figure 15. Switching times test circuit for resistive load

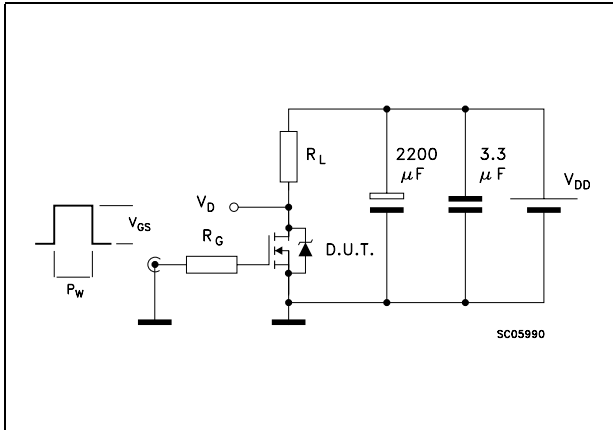


Figure 16. Gate charge test circuit

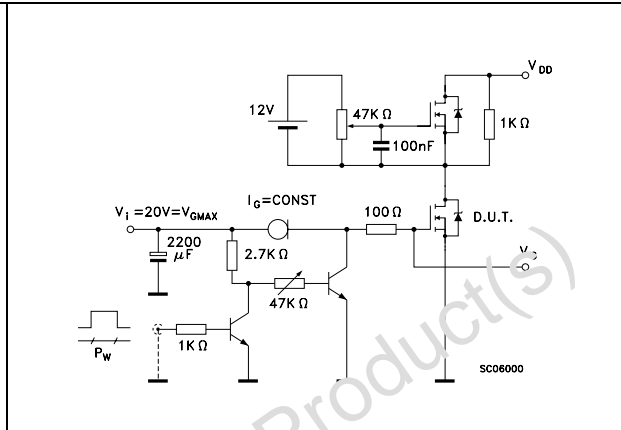


Figure 17. Test circuit for inductive load switching and diode recovery times

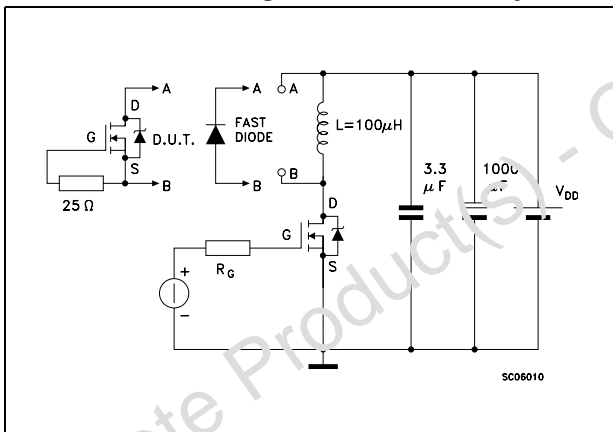


Figure 18. Unclamped inductive load test circuit

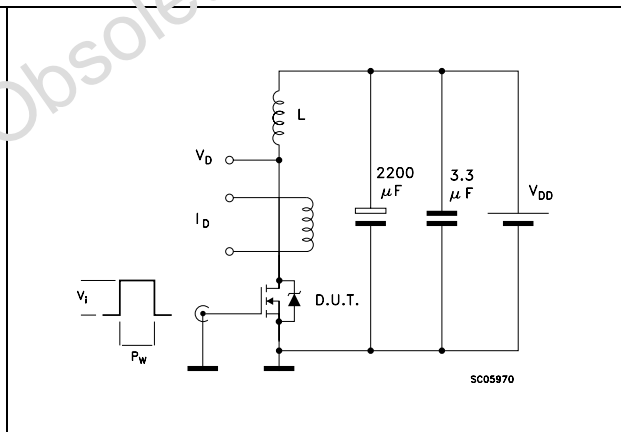


Figure 19. Unclamped inductive waveform

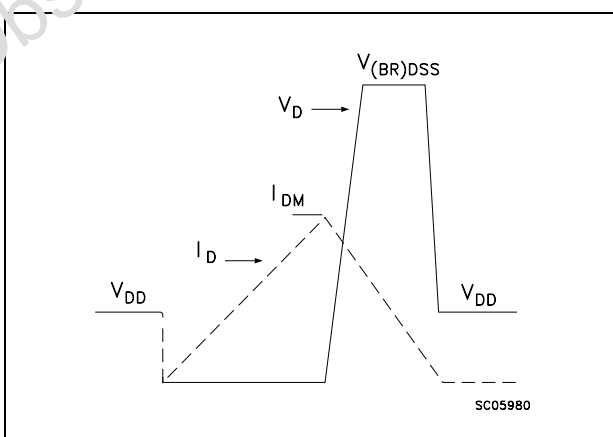
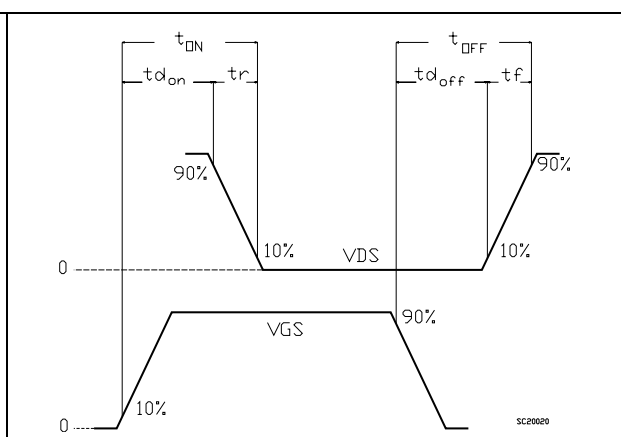


Figure 20. Switching time waveform



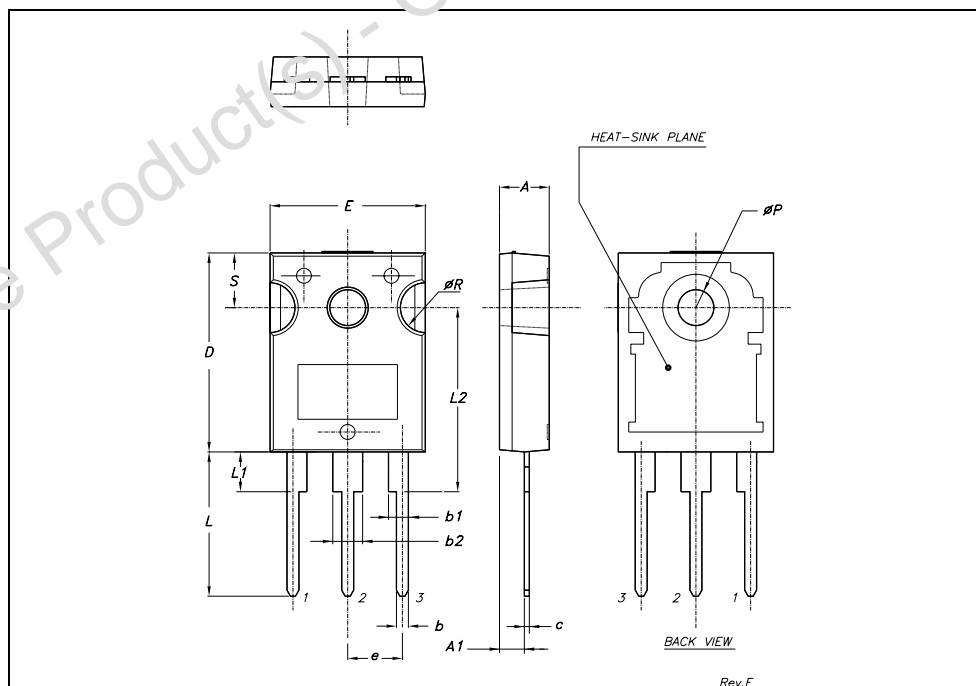
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

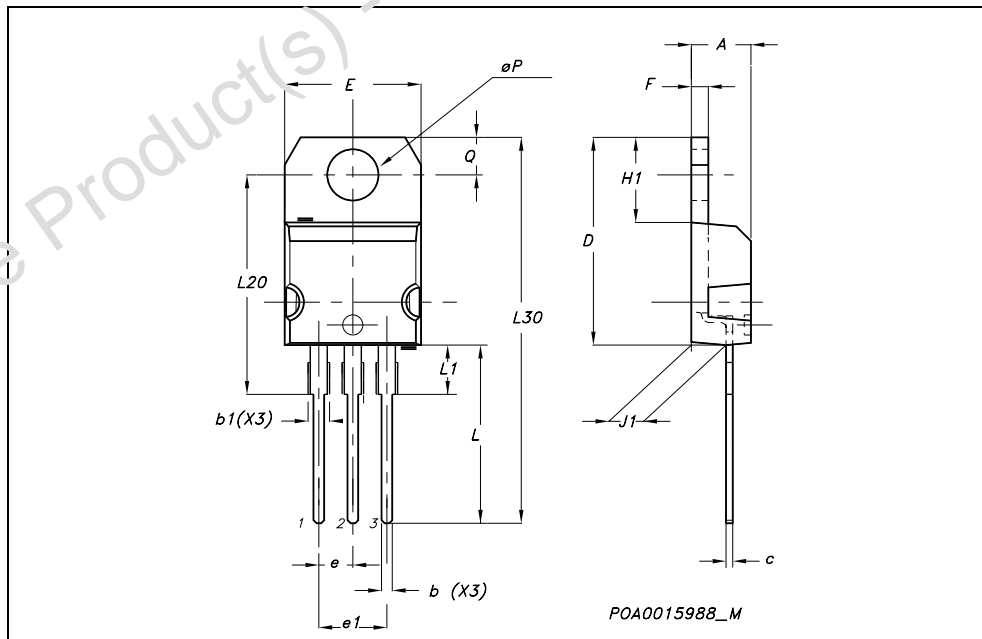
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**TO-247 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.85		5.15	0.19		0.20
A1	2.20		2.60	0.086		0.102
b	1.0		1.40	0.039		0.055
b1	2.0		2.40	0.079		0.094
b2	3.0		3.40	0.118		0.134
c	0.40		0.80	0.015		0.03
D	19.85		20.15	0.781		0.793
E	15.45		15.75	0.608		0.620
e		5.45			0.214	
L	14.20		14.80	0.560		0.582
L1	3.70		4.30	0.146		0.17
L2		18.50			0.728	
øP	3.55		3.65	0.140		0.143
øR	4.50		5.50	0.177		0.216
S		5.50			0.216	



TO-220 MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



## 5 Revision history

Table 8. Revision history

Date	Revision	Changes
06-Mar-2006	1	First Release
17-Nov-2006	2	Part number has been updated

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