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April 1st, 2010 Renesas Electronics Corporation

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DATA SHEET

MOS FIELD EFFECT TRANSISTOR

SWITCHING N-CHANNEL POWER MOS FET

DESCRIPTION

The NP110N04PUJ is N-channel MOS Field Effect Transistor designed for high current switching applications.

ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE		
NP110N04PUJ-E1B-AY Note					
NP110N04PUJ-E2B-AY Note	Pure Sn (Tin)	Tape 1000 p/reel	TO-263 (MP-25ZP) typ. 1.5 g		

Note Pb-free (This product does not contain Pb in external electrode.)

FEATURES

Super low on-state resistance

 $R_{DS(on)}$ = 1.8 m Ω MAX. (V_{GS} = 10 V, I_D = 55 A)

- Low input capacitance
- C_{iss} = 9500 pF TYP.
- Designed for automotive application and AEC-Q101 qualified

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^{\circ}C$)

Drain to Source Voltage (VGs = 0 V)	VDSS	40	V
Gate to Source Voltage (VDS = 0 V)	Vgss	±20	V
Drain Current (DC) (Tc = 25°C)	D(DC)	±110	А
Drain Current (pulse) Note1	D(pulse)	±440	А
Total Power Dissipation (Tc = 25° C)	Pt1	288	W
Total Power Dissipation (T _A = 25°C)	Pt2	1.8	W
Channel Temperature	Tch	175	°C
Storage Temperature	Tstg	-55 to +175	°C
Single Avalanche Energy Note2	Eas	518	mJ
Repetitive Avalanche Current Note3	IAR	72	А
Repetitive Avalanche Energy Note3	Ear	518	mJ

(TO-263)

Notes 1. PW \leq 10 μ s, Duty Cycle \leq 1%

2. Starting T_{ch} = 25°C, V_{DD} = 20 V, R_G = 25 Ω , V_{GS} = 20 \rightarrow 0 V, L = 100 μ H

3. $T_{ch} \le 150^{\circ}C$, RG = 25 Ω

THERMAL RESISTANCE				
Channel to Case Thermal Resistance	Rth(ch-C)	0.52		
Channel to Ambient Thermal Resistance	Rth(ch-A)	83.3		

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°C/W °C/W

Document No. D19730EJ1V0DS00 (1st edition) Date Published April 2009 NS Printed in Japan

ELECTRICAL CHARACTERISTICS (TA = 25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V _{DS} = 40 V, V _{GS} = 0 V			1	μA
Gate Leakage Current	Igss	V _{GS} = ±20 V, V _{DS} = 0 V			±100	nA
Gate to Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2.0	3.0	4.0	V
Forward Transfer Admittance Note	y _{fs}	Vds = 5 V, Id = 55 A	55	118		S
Drain to Source On-state Resistance ^{Note}	RDS(on)	Vgs = 10 V, Id = 55 A		1.4	1.8	mΩ
Input Capacitance	Ciss	V _{DS} = 25 V,		9500	14250	pF
Output Capacitance	Coss	V _{GS} = 0 V,		1250	1880	pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		410	740	pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 20 V, I _D = 55 A,		45	100	ns
Rise Time	tr	V _{GS} = 10 V,		22	60	ns
Turn-off Delay Time	t _{d(off)}	R _G = 0 Ω		100	200	ns
Fall Time	tr			15	40	ns
Total Gate Charge	QG	V _{DD} = 32 V,		150	230	nC
Gate to Source Charge	QGS	V _{GS} = 10 V,		35		nC
Gate to Drain Charge	Qgd	I _D = 110 A		45		nC
Body Diode Forward Voltage Note	VF(S-D)	IF = 110 A, VGS = 0 V		0.9	1.5	V
Reverse Recovery Time	trr	I⊧ = 110 A, V _{GS} = 0 V,		68		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/ <i>µ</i> s		135		nC

PG.

τ

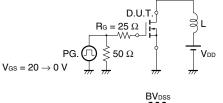
 $\tau = 1 \, \mu s$

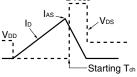
Vgs

0.

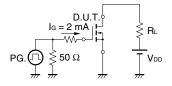
Note Pulsed test

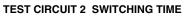
TEST CIRCUIT 1 AVALANCHE CAPABILITY

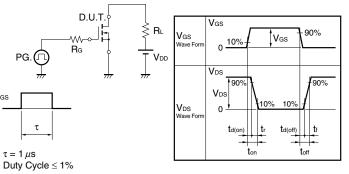




TEST CIRCUIT 3 GATE CHARGE

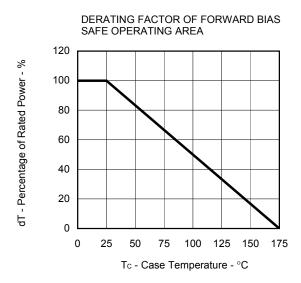




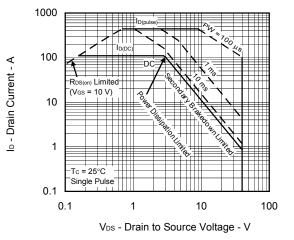


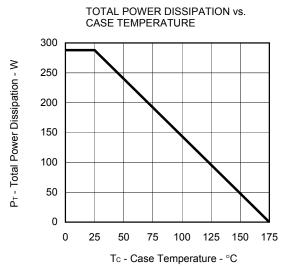
Data Sheet D19730EJ1V0DS

TYPICAL CHARACTERISTICS (T_A = 25°C)

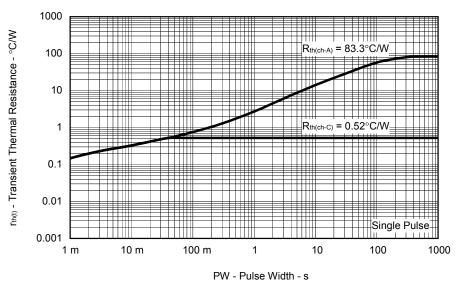






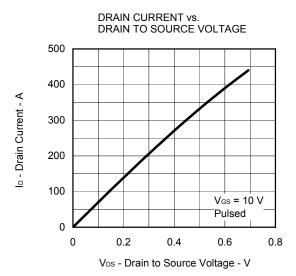


TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

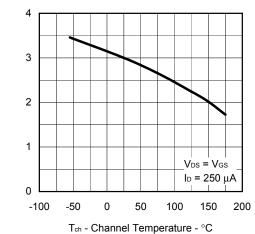


Data Sheet D19730EJ1V0DS

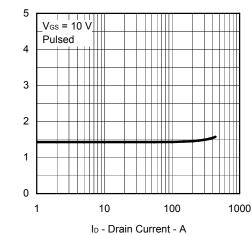
V_{GS(th)} - Gate to Source Threshold Voltage - V



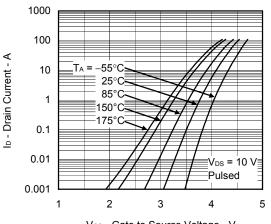




DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

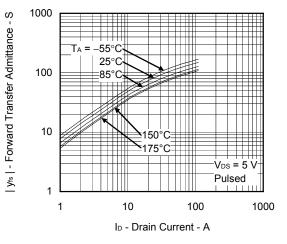


FORWARD TRANSFER CHARACTERISTICS

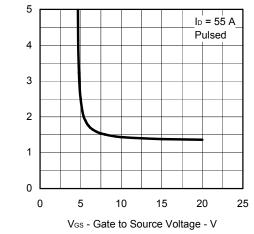


VGS - Gate to Source Voltage - V

FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



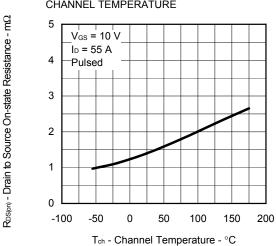
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



 $R_{DS(m)}$ - Drain to Source On-state Resistance - $m\Omega$

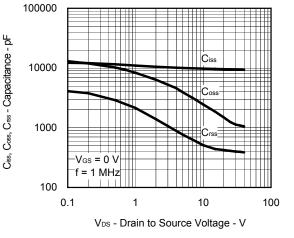
 $R_{DS(m)}$ - Drain to Source On-state Resistance - m Ω

ta(on), tr, ta(off), tr - Switching Time - ns

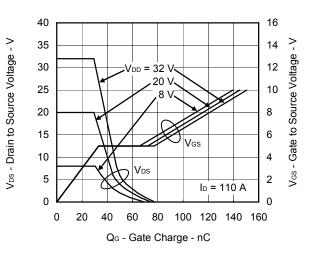




CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



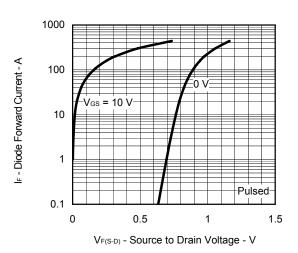
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



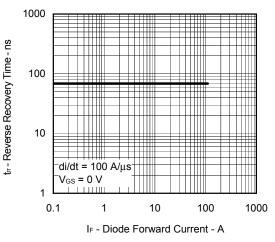
1000 100 td(off) td(on) tf 10 $V_{DD} = 20 V_{c}$ V_{GS} = 10 V $R_G = 0 \Omega$ 1 0.1 1 10 100 1000 ID - Drain Current - A

SWITCHING CHARACTERISTICS

SOURCE TO DRAIN DIODE FORWARD VOLTAGE

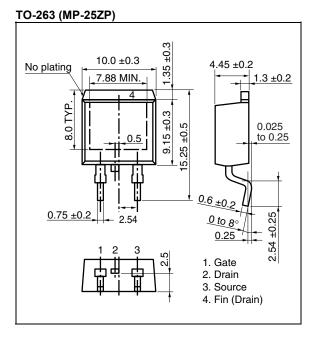




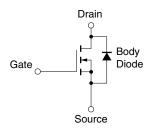


Data Sheet D19730EJ1V0DS

PACKAGE DRAWING (Unit: mm)



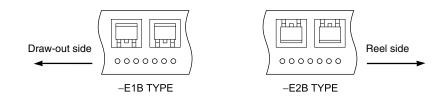
EQUIVALENT CIRCUIT



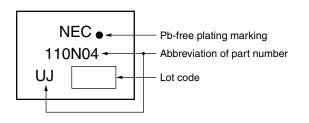
Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

TAPE INFORMATION

There are two types (-E1B, -E2B) of taping depending on the direction of the device.



MARKING INFORMATION



RECOMMENDED SOLDERING CONDITIONS

The NP110N04PUJ should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, please contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Maximum temperature (Package's surface temperature): 260°C or below	IR60-00-3
	Time at maximum temperature: 10 seconds or less	
	Time of temperature higher than 220°C: 60 seconds or less	
	Preheating time at 160 to 180°C: 60 to 120 seconds	
	Maximum number of reflow processes: 3 times	
	Maximum chlorine content of rosin flux (percentage mass): 0.2% or less	
Partial heating	Maximum temperature (Pin temperature): 350°C or below	P350
	Time (per side of the device): 3 seconds or less	
	Maximum chlorine content of rosin flux: 0.2% (wt.) or less	

Caution Do not use different soldering methods together (except for partial heating).

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