STL8N65M5

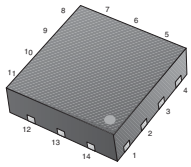
N-channel 650 V, 0.56 Ω, 7 A MDmesh™ V Power MOSFET in PowerFLAT™ 5x5

Features

Order code	V_{DSS} @ T_{Jmax}	$R_{DS(on)}$ max	I_D
STL8N65M5	710 V	< 0.6 Ω	7 A (1)

1. The value is rated according to $R_{thj\text{-}case}$

- Worldwide best $R_{DS(on)}$ * area
- Higher V_{DSS} rating
- High dv/dt capability
- Excellent switching performance
- Easy to drive
- 100% avalanche tested



PowerFLAT™ 5x5

Applications

- Switching applications

Description

This device is an N-channel MDmesh™ V Power MOSFET based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

Figure 1. Internal schematic diagram

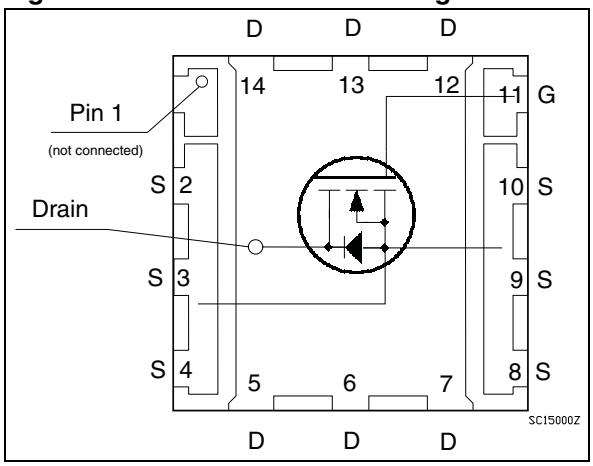


Table 1. Device summary

Order code	Marking	Package	Packaging
STL8N65M5	8N65M5	PowerFLAT™ 5x5	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	650	V
V_{GS}	Gate-source voltage	± 25	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	7	A
I_D (1)	Drain current (continuous) at T_C = 100 °C	4.4	A
I_D(2)	Drain current (continuous) at T_{amb} = 25 °C	1.4	A
I_D(2)	Drain current (continuous) at T_{amb} = 100 °C	0.6	A
I_{DM}(2),(3)	Drain current (pulsed)	5.6	A
P_{TOT} (2)	Total dissipation at T_{amb} = 25 °C	2.5	W
P_{TOT}(1)	Total dissipation at T_C = 25 °C	70	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	2	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	120	mJ
dv/dt (4)	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature	- 55 to 150	°C
T_j	Max. operating junction temperature	150	°C

1. The value is rated according to $R_{thj\text{-}case}$
2. When mounted on FR-4 board of inch², 2oz Cu
3. Pulse with limited by safe operating area.
4. $I_{SD} \leq 7$ A, di/dt $\leq$ 400 A/µs, $V_{Peak} < V_{(BR)DSS}$, V_{DD} = 400 V.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	1.78	°C/W
$R_{thj\text{-}pcb}$(1)	Thermal resistance junction-pcb max	60	°C/W

1. When mounted on 1inch² FR-4 board, 2 oz Cu

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage (V_{GS} = 0)	I_D = 1 mA	650			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 650 V V_{DS} = 650 V, T_C=125 °C			1 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 25 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 3.5 A		0.56	0.6	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0	-	690 18 2	-	pF pF pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{DS} = 0 to 520 V, V_{GS} = 0	-	17	-	pF
$C_{o(er)}$(2)	Equivalent capacitance energy related		-	52	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	2.4	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 520 V, I_D = 3.5 A, V_{GS} = 10 V (see *Figure 15*)	-	15 3.6 6	-	nC nC nC

1. $C_{oss\ eq.}$ time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. $C_{oss\ eq.}$ energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(off)}$ $t_{r\ (V)}$ $t_{c(off)}$ $t_{f\ (i)}$	Turn-off delay time Rise time Cross time Fall time	V_{DD} = 400 V, I_D = 4 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 16*), (see *Figure 19*)	-	50 14 20 11	-	ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)		-		7 28	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 7 A, V_{GS} = 0	-		1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 7A, di/dt = 100 A/µs V_{DD} = 100 V (see *Figure 16*)	-	200 1.6 16		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 7 A, di/dt = 100 A/µs V_{DD} = 100 V, T_j = 150 °C (see *Figure 16*)	-	263 1.9 15		ns µC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

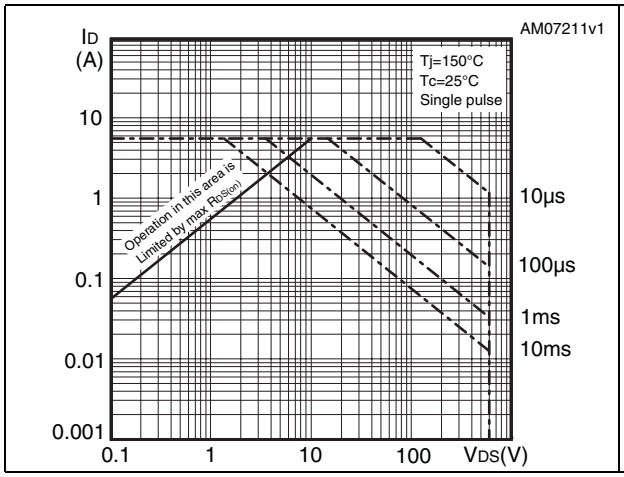


Figure 3. Thermal impedance

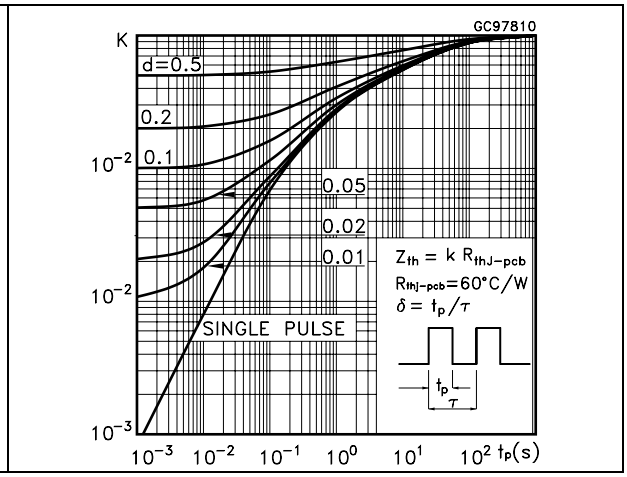


Figure 4. Output characteristics

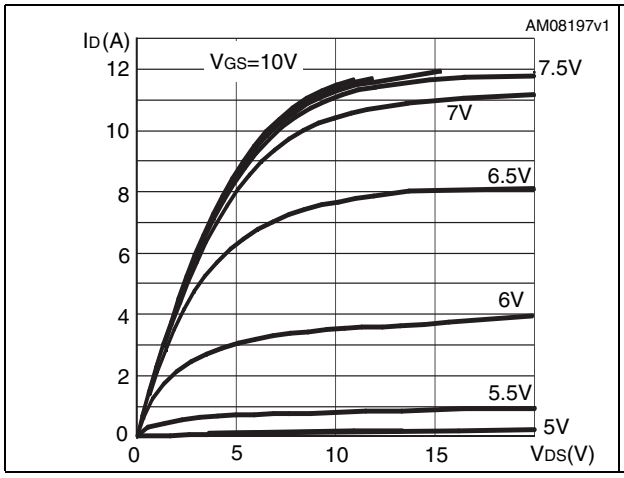


Figure 5. Transfer characteristics

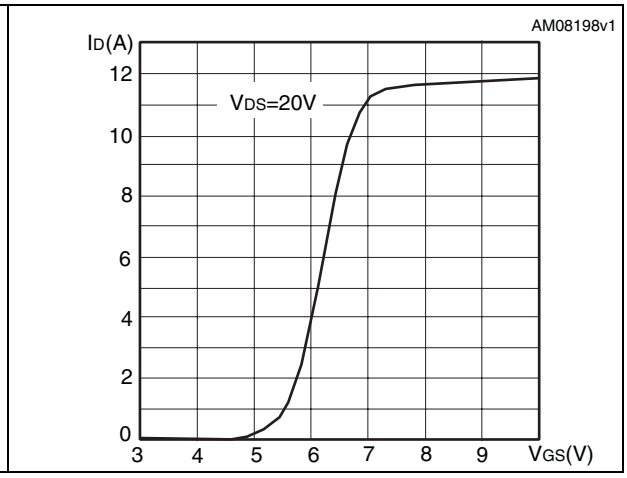


Figure 6. Gate charge vs gate-source voltage

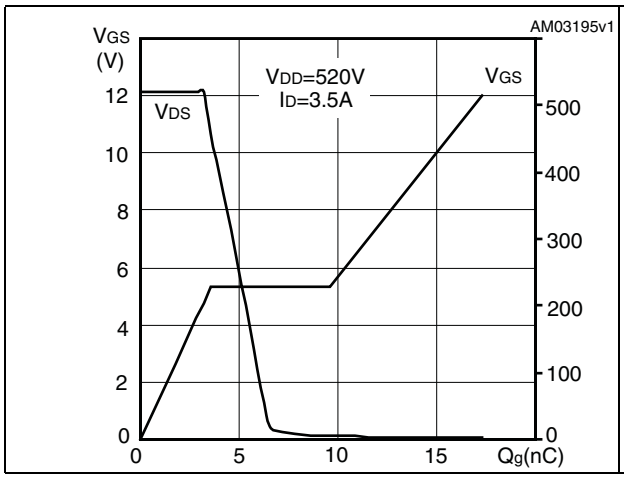


Figure 7. Static drain-source on resistance

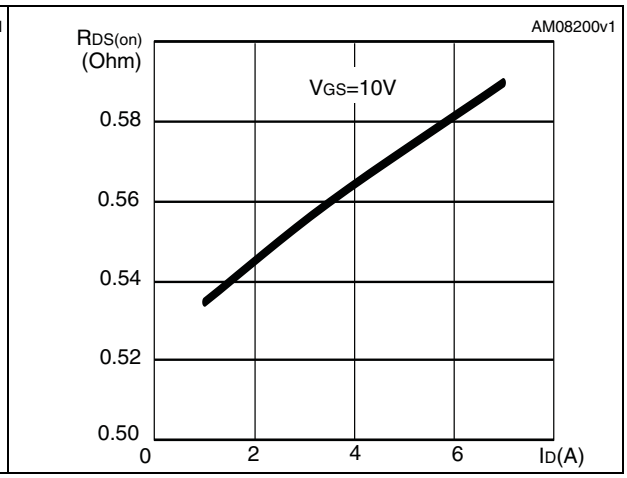


Figure 8. Capacitance variations

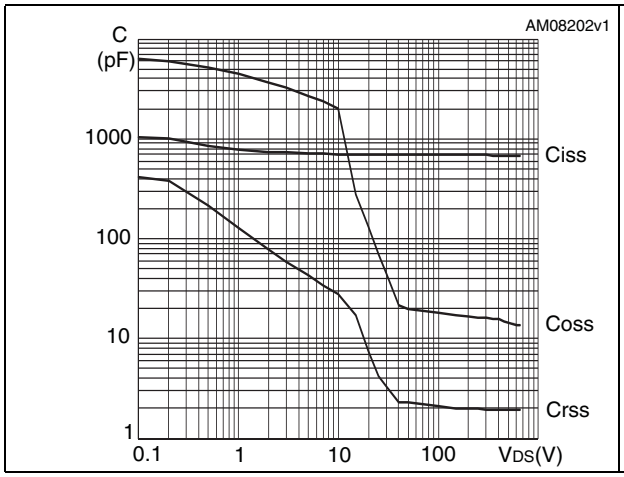


Figure 9. Output capacitance stored energy

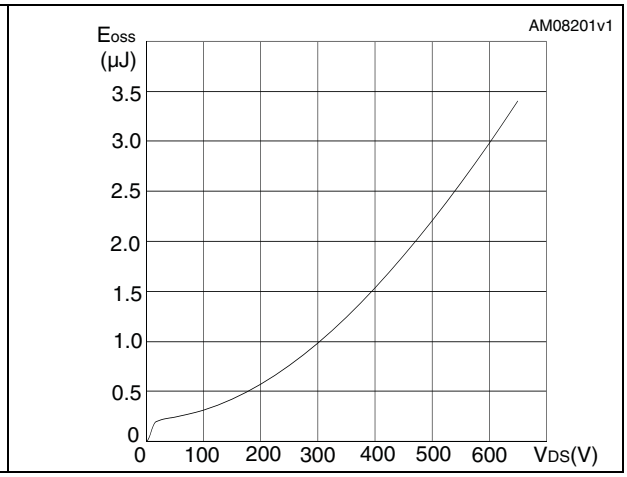


Figure 10. Normalized gate threshold voltage vs temperature

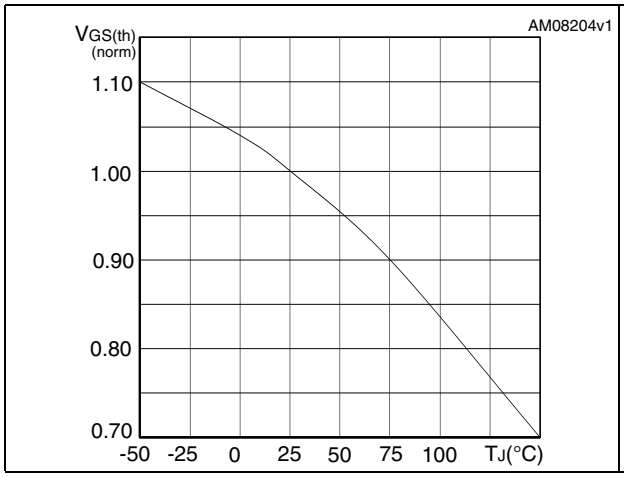


Figure 11. Normalized on resistance vs temperature

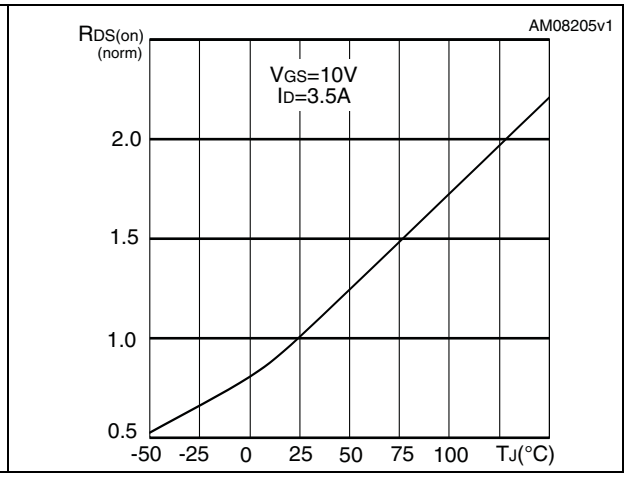


Figure 12. Switching losses vs gate resistance (1)

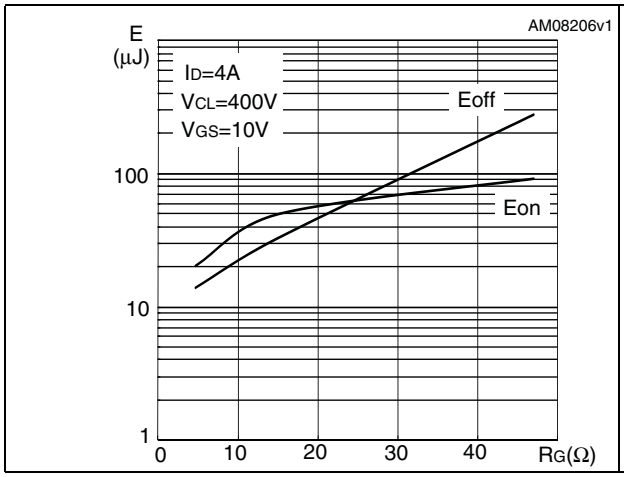
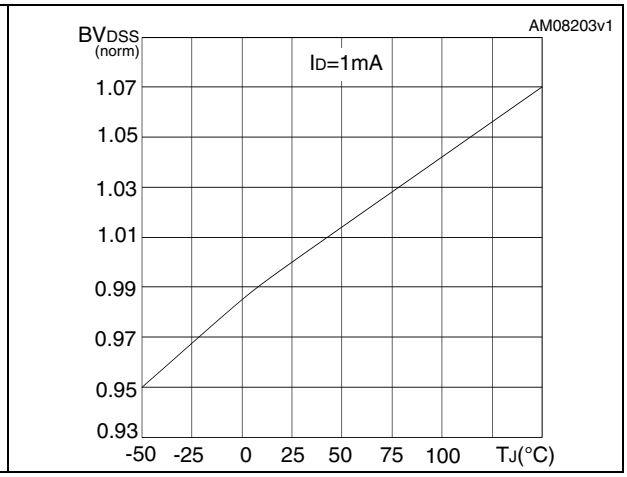


Figure 13. Normalized B_{VDSS} vs temperature



1. Eon including reverse recovery of a SiC diode

3 Test circuits

Figure 14. Switching times test circuit for resistive load

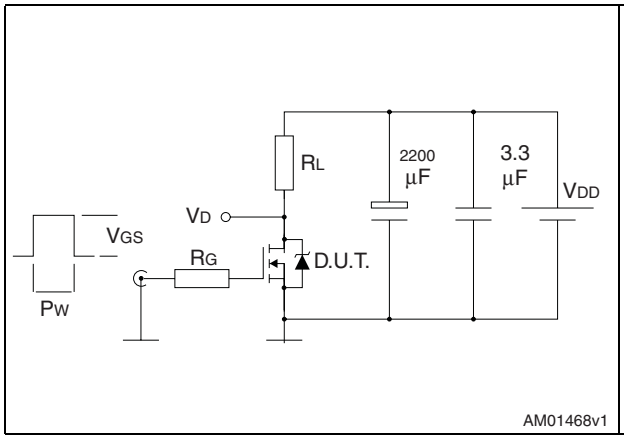


Figure 15. Gate charge test circuit

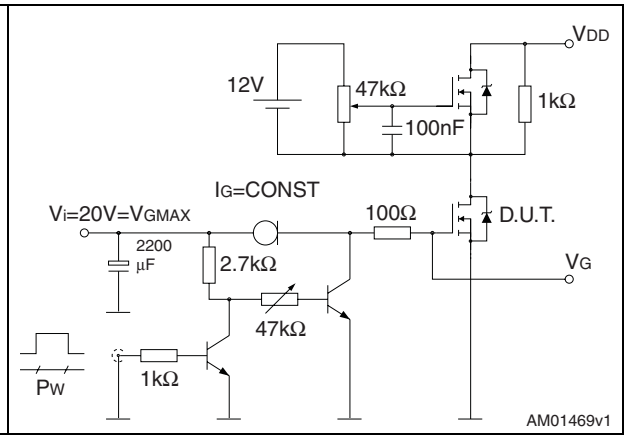


Figure 16. Test circuit for inductive load switching and diode recovery times

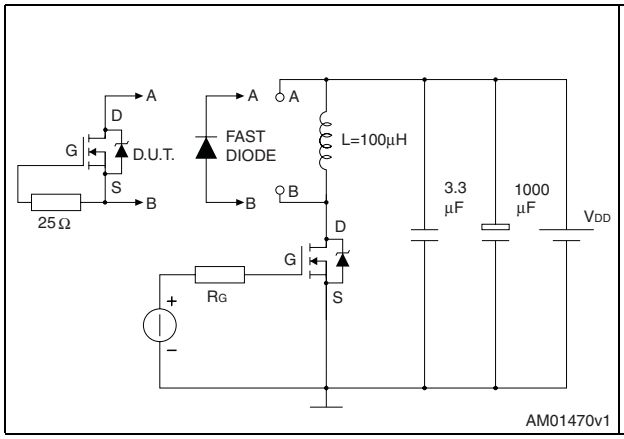


Figure 17. Unclamped inductive load test circuit

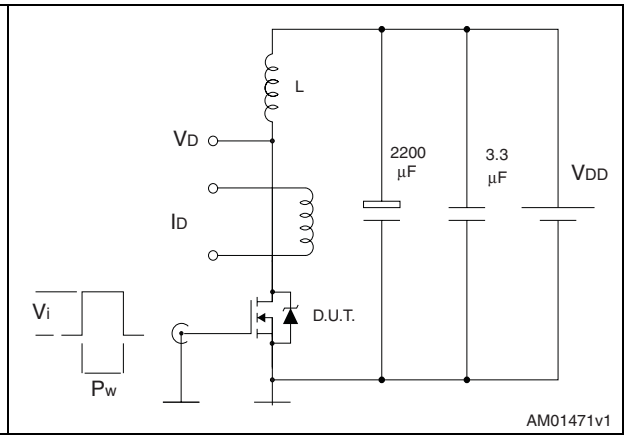


Figure 18. Unclamped inductive waveform

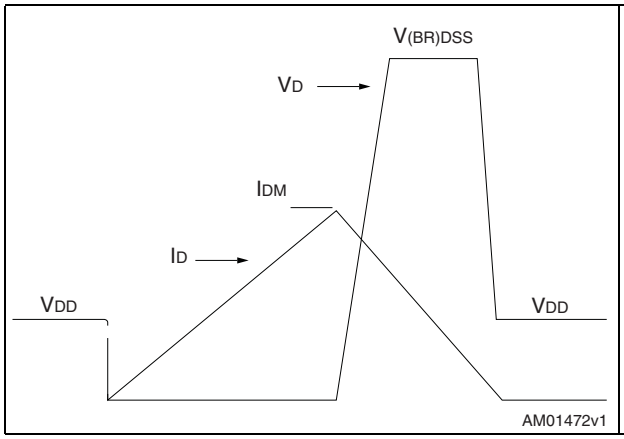
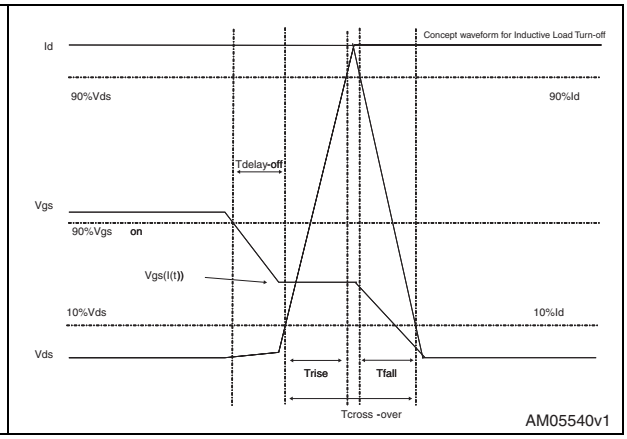


Figure 19. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. PowerFLAT™ 5x5 mechanical dimensions

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.0
A1	0	0.02	0.05
A3		0.24	
D	4.90	5.0	5.10
E	4.90	5.0	5.10
E2	2.49	2.57	2.64
e	1.22	1.27	1.32
b	0.43	0.51	0.58
c	0.64	0.71	0.79

Figure 20. PowerFLAT™ 5x5 mechanical drawing

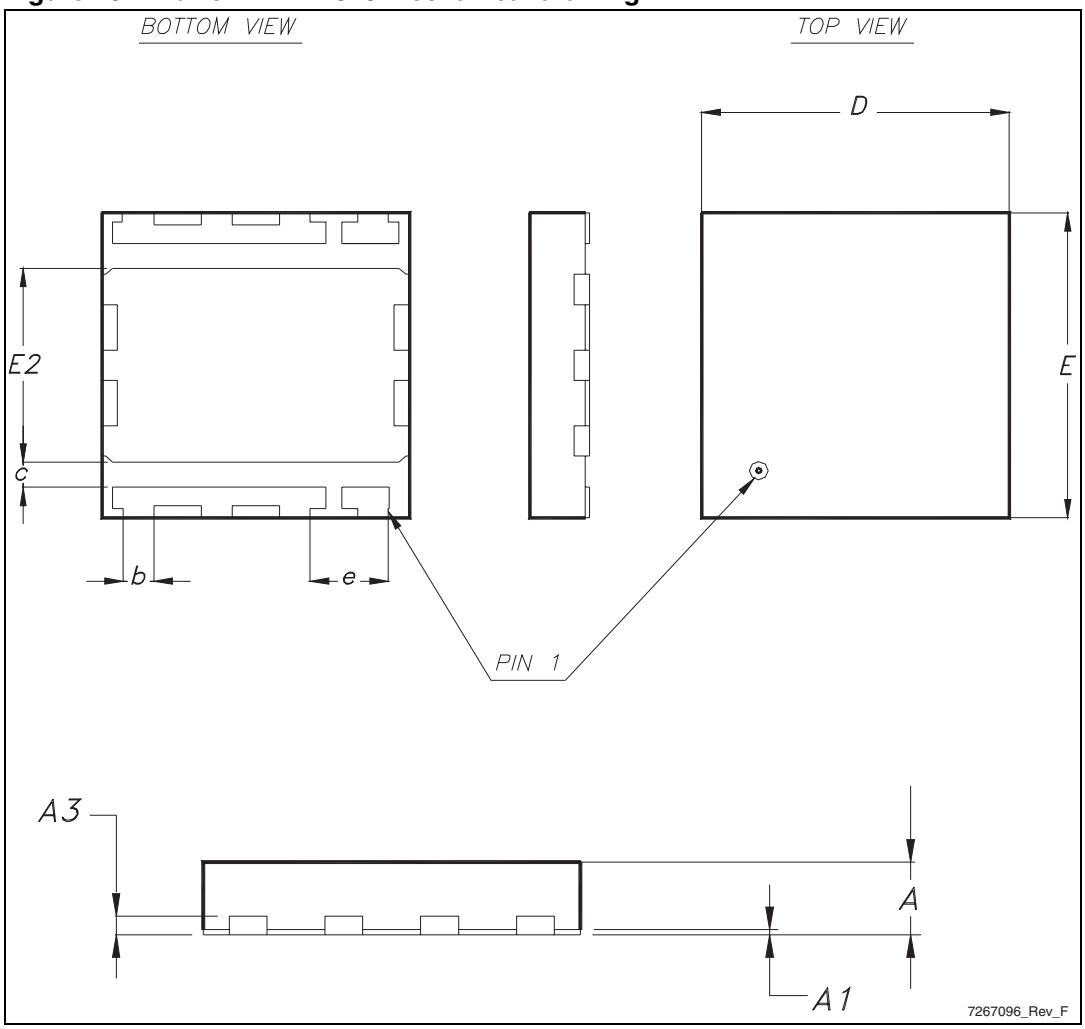
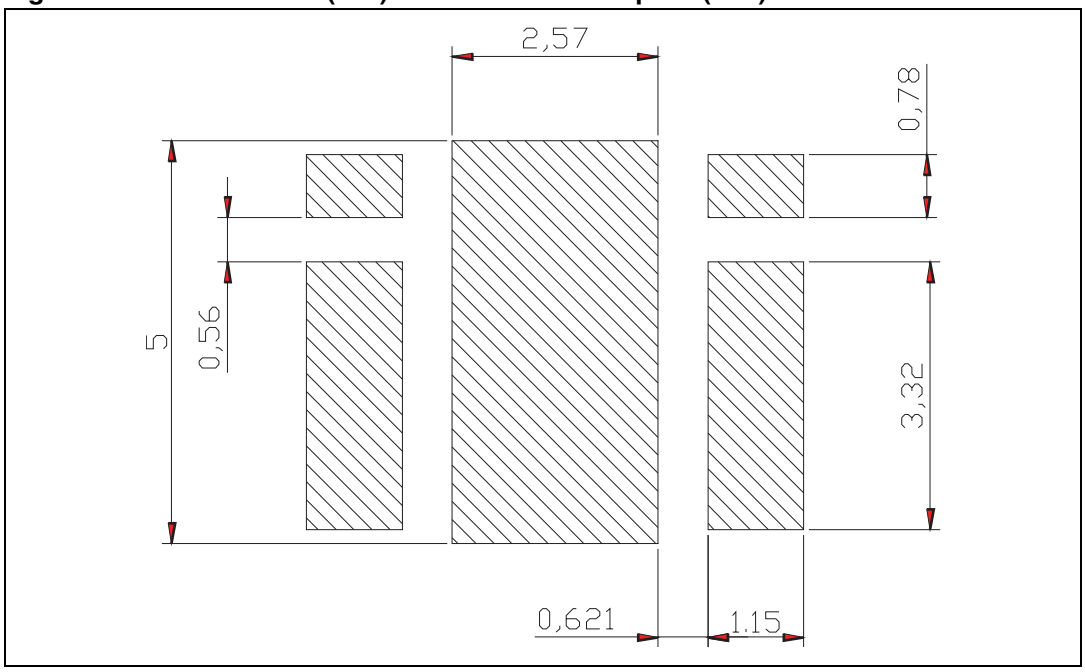


Figure 21. PowerFLAT™(5x5) recommended footprint (mm)



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
05-Jul-2011	1	First release
07-Jul-2011	2	Updated *Figure 1*.
08-Aug-2011	3	Updated *Figure 3: Thermal impedance*. and $R_{thj\text{-}pcb}$ value in *Table 3: Thermal data*. Minor text changes.

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