

# NTMFS4837NH

## Power MOSFET

30 V, 75 A, Single N-Channel, SO-8FL

### Features

- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- Low  $R_G$
- These are Pb-Free Devices

### Applications

- Refer to Application Note AND8195/D
- CPU Power Delivery
- DC-DC Converters and Low Side Switching

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	30	V
Gate-to-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current $R_{\theta JA}$ (Note 1)	$I_D$	$T_A = 25^\circ\text{C}$	16
		$T_A = 85^\circ\text{C}$	11.5
Power Dissipation $R_{\theta JA}$ (Note 1)	$P_D$	$T_A = 25^\circ\text{C}$	2.2
		$T_A = 85^\circ\text{C}$	1.15
Continuous Drain Current $R_{\theta JA} \leq 10$ s	$I_D$	$T_A = 25^\circ\text{C}$	26
		$T_A = 85^\circ\text{C}$	18.8
Power Dissipation $R_{\theta JA} \leq 10$ s	$P_D$	$T_A = 25^\circ\text{C}$	5.8
		$T_A = 85^\circ\text{C}$	3
Continuous Drain Current $R_{\theta JA}$ (Note 2)	$I_D$	$T_A = 25^\circ\text{C}$	10.2
		$T_A = 85^\circ\text{C}$	7.3
Power Dissipation $R_{\theta JA}$ (Note 2)	$P_D$	$T_A = 25^\circ\text{C}$	0.88
		$T_A = 85^\circ\text{C}$	0.46
Continuous Drain Current $R_{\theta JC}$ (Note 1)	$I_D$	$T_C = 25^\circ\text{C}$	75
		$T_C = 85^\circ\text{C}$	54
Power Dissipation $R_{\theta JC}$ (Note 1)	$P_D$	$T_C = 25^\circ\text{C}$	48
		$T_C = 85^\circ\text{C}$	25
Pulsed Drain Current	$I_{DM}$	225	A
Operating Junction and Storage Temperature	$T_J, T_{STG}$	-55 to	$^\circ\text{C}$
		+150	
Source Current (Body Diode)	$I_S$	40	A
Drain to Source $dV/dt$	$dV/dt$	6	V/ns
Single Pulse Drain-to-Source Avalanche Energy ( $V_{DD} = 30$ V, $V_{GS} = 10$ V, $I_L = 31$ A, $L = 0.3$ mH, $R_G = 25$ $\Omega$ )	EAS	144	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

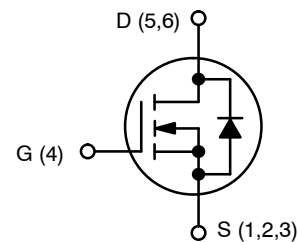
1. Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.
2. Surface-mounted on FR4 board using the minimum recommended pad size.



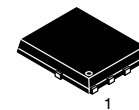
ON Semiconductor®

<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	$I_D$ MAX
30 V	5.0 m $\Omega$ @ 10 V	75 A
	8.0 m $\Omega$ @ 4.5 V	



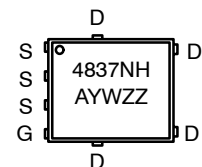
N-CHANNEL MOSFET



SO-8 FLAT LEAD  
CASE 488AA  
STYLE 1

- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

### MARKING DIAGRAM



### ORDERING INFORMATION

Device	Package	Shipping†
NTMFS4837NHT1G	SO-8FL (Pb-Free)	1500 / Tape & Reel
NTMFS4837NHT3G	SO-8FL (Pb-Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NTMFS4837NH

## THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	2.6	°C/W
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	56.6	
Junction-to-Ambient – Steady State (Note 4)	$R_{\theta JA}$	142	
Junction-to-Ambient ( $t \leq 10$ s)	$R_{\theta JA}$	21.6	

3. Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.
4. Surface-mounted on FR4 board using the minimum recommended pad size.

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0$ V, $I_D = 250$ $\mu$ A	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			27.5		mV/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0$ V, $V_{DS} = 24$ V	$T_J = 25$ °C		1	$\mu$ A
			$T_J = 125$ °C		10	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0$ V, $V_{GS} = \pm 20$ V			$\pm 100$	nA

### ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$ , $I_D = 250$ $\mu$ A	1.5	2.1	2.5	V	
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			5.7		mV/°C	
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10$ V to 11.5 V	$I_D = 30$ A		3.7	5.0	m $\Omega$
			$I_D = 15$ A		3.7		
		$V_{GS} = 4.5$ V	$I_D = 30$ A		6.5	8.0	
			$I_D = 15$ A		6.4		
Forward Transconductance	$g_{FS}$	$V_{DS} = 1.5$ V, $I_D = 50$ A		67		S	

### CHARGES AND CAPACITANCES

Input Capacitance	$C_{ISS}$	$V_{GS} = 0$ V, $f = 1$ MHz, $V_{DS} = 12$ V		2234	3016	pF
Output Capacitance	$C_{OSS}$			450	608	
Reverse Transfer Capacitance	$C_{RSS}$			243	375	
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5$ V, $V_{DS} = 15$ V; $I_D = 30$ A		15.9	23.8	nC
Threshold Gate Charge	$Q_{G(TH)}$			2.8	4.3	
Gate-to-Source Charge	$Q_{GS}$			6.4	9.5	
Gate-to-Drain Charge	$Q_{GD}$			6.6	9.8	
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 11.5$ V, $V_{DS} = 15$ V; $I_D = 15$ A		34.4	53	nC

### SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5$ V, $V_{DS} = 15$ V, $I_D = 15$ A, $R_G = 3.0$ $\Omega$		15.2	22.8	ns
Rise Time	$t_r$			27.5	41.3	
Turn-Off Delay Time	$t_{d(OFF)}$			18.3	27.5	
Fall Time	$t_f$			7.1	10.6	

5. Pulse Test: pulse width  $\leq 300$   $\mu$ s, duty cycle  $\leq 2\%$ .
6. Switching characteristics are independent of operating junction temperatures.

# NTMFS4837NH

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>SWITCHING CHARACTERISTICS</b> (Note 6)						
Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 11.5\text{ V}, V_{DS} = 15\text{ V},$ $I_D = 15\text{ A}, R_G = 3.0\ \Omega$		9.0	14	ns
Rise Time	$t_r$			19.6	29.3	
Turn-Off Delay Time	$t_{d(OFF)}$			28	38.7	
Fall Time	$t_f$			4.7	7	

## DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V},$ $I_S = 30\text{ A}$	$T_J = 25^\circ\text{C}$		0.83	1.2	V
			$T_J = 125^\circ\text{C}$		0.71		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s},$ $I_S = 30\text{ A}$			23.5		ns
Charge Time	$t_a$				11.3		
Discharge Time	$t_b$				12.2		
Reverse Recovery Charge	$Q_{RR}$				8		

## PACKAGE PARASITIC VALUES

Source Inductance	$L_S$	$T_A = 25^\circ\text{C}$		0.93		nH
Drain Inductance	$L_D$			0.005		
Gate Inductance	$L_G$			1.84		
Gate Resistance	$R_G$			0.9		

5. Pulse Test: pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .
6. Switching characteristics are independent of operating junction temperatures.

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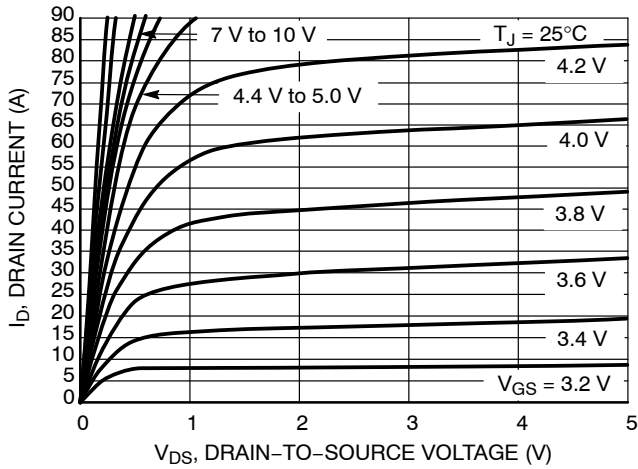


Figure 1. On-Region Characteristics

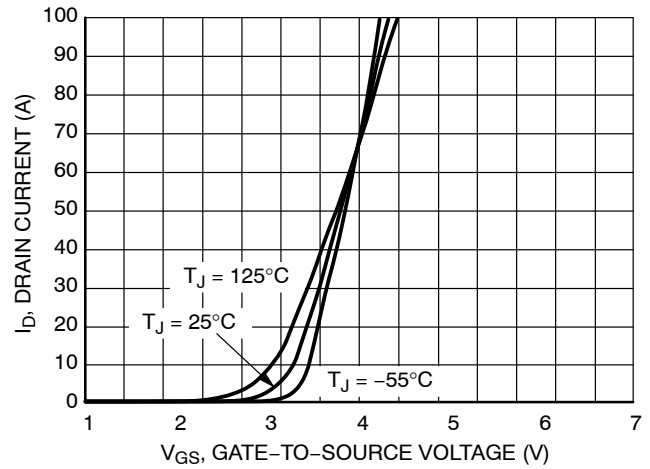


Figure 2. Transfer Characteristics

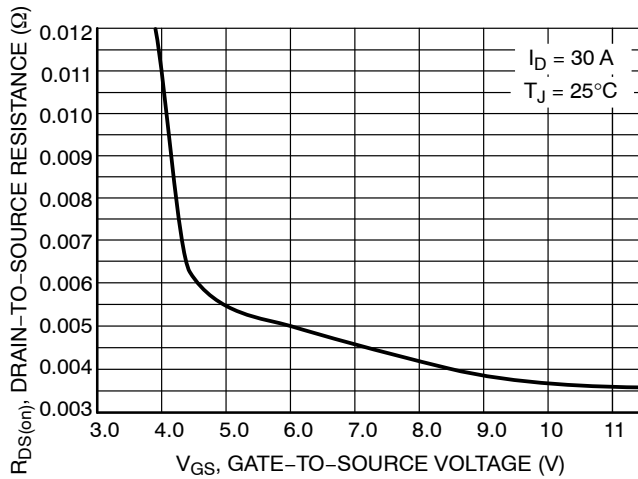


Figure 3. On-Resistance versus Gate-to-Source Voltage

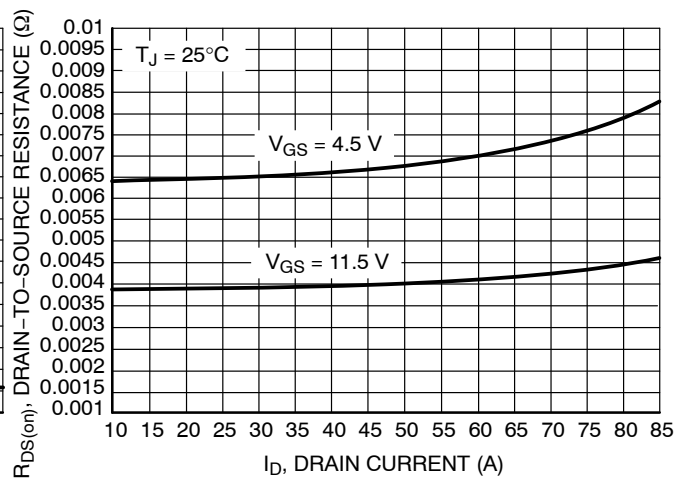


Figure 4. On-Resistance versus Drain Current and Gate Voltage

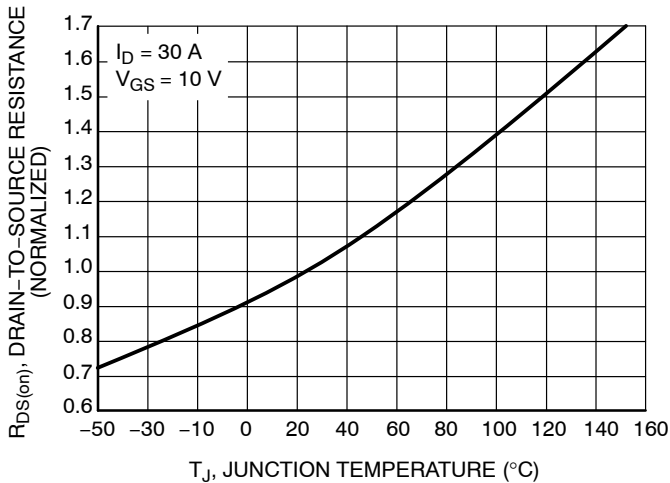


Figure 5. On-Resistance Variation with Temperature

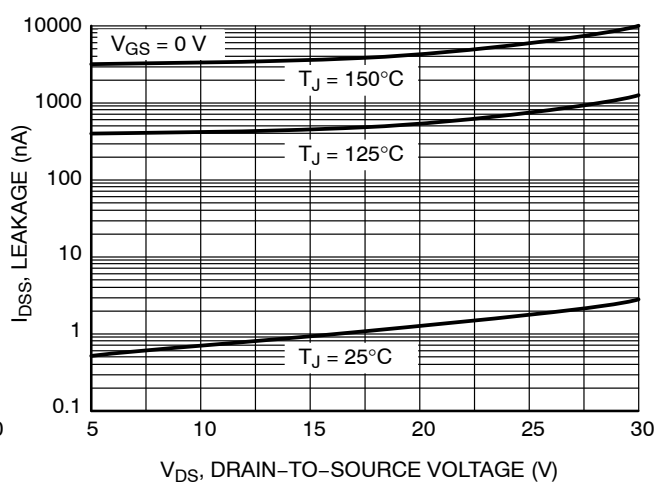
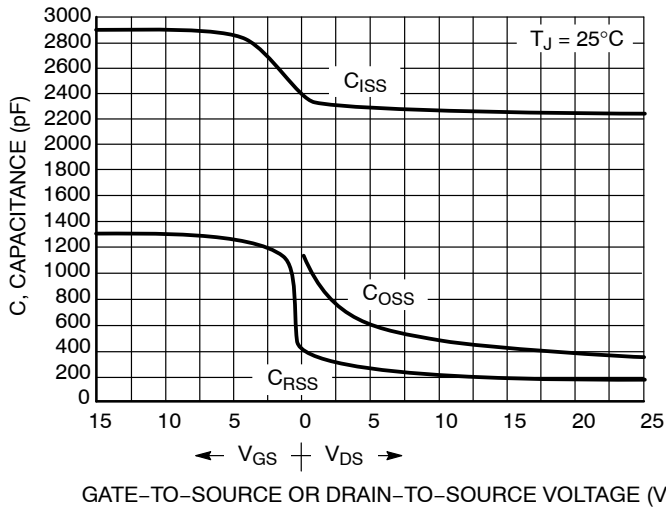
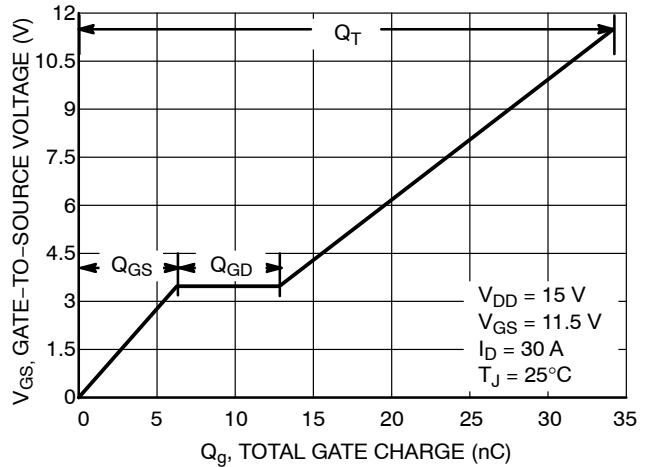


Figure 6. Drain-to-Source Leakage Current versus Voltage

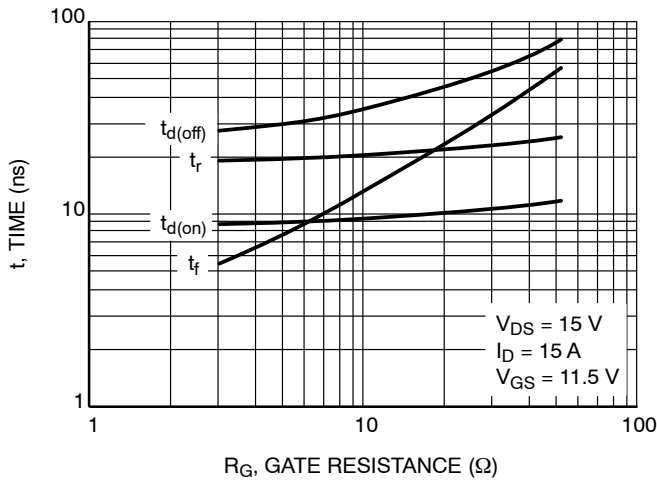
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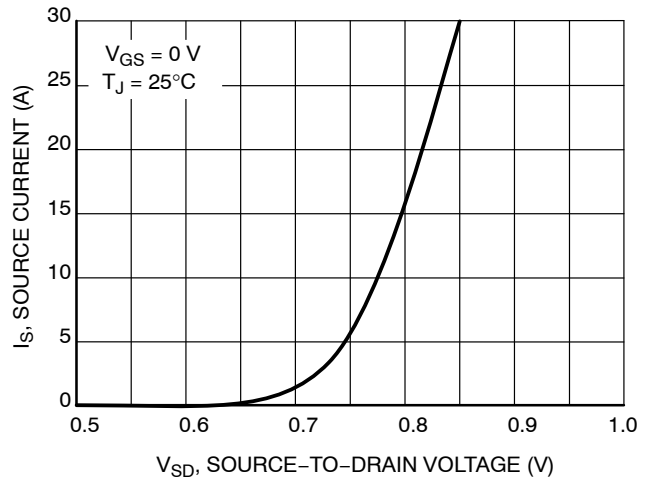
**Figure 7. Capacitance Variation**



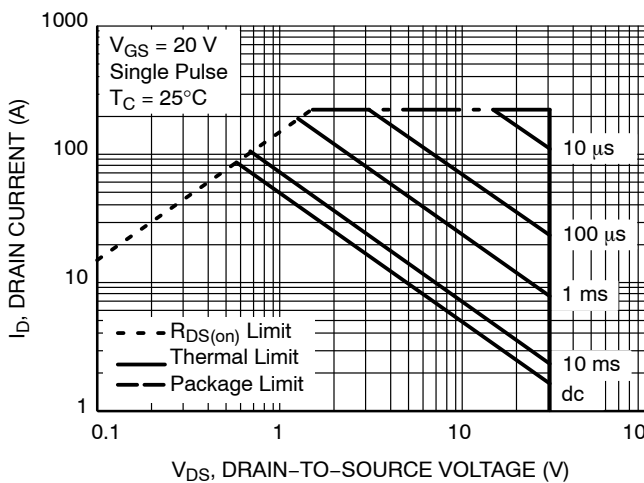
**Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Gate Charge**



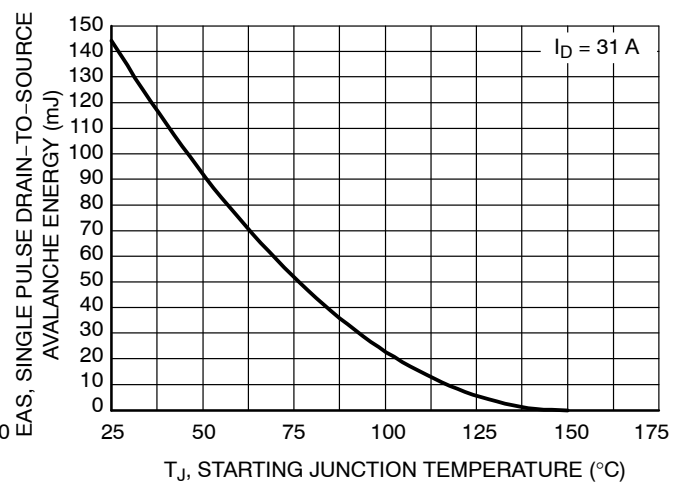
**Figure 9. Resistive Switching Time Variation versus Gate Resistance**



**Figure 10. Diode Forward Voltage versus Current**



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

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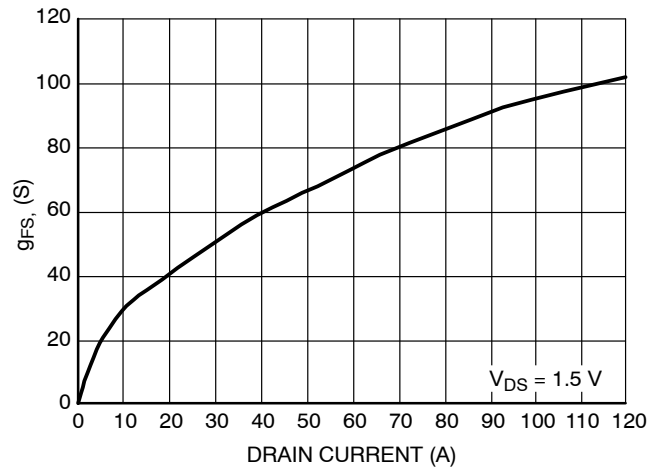
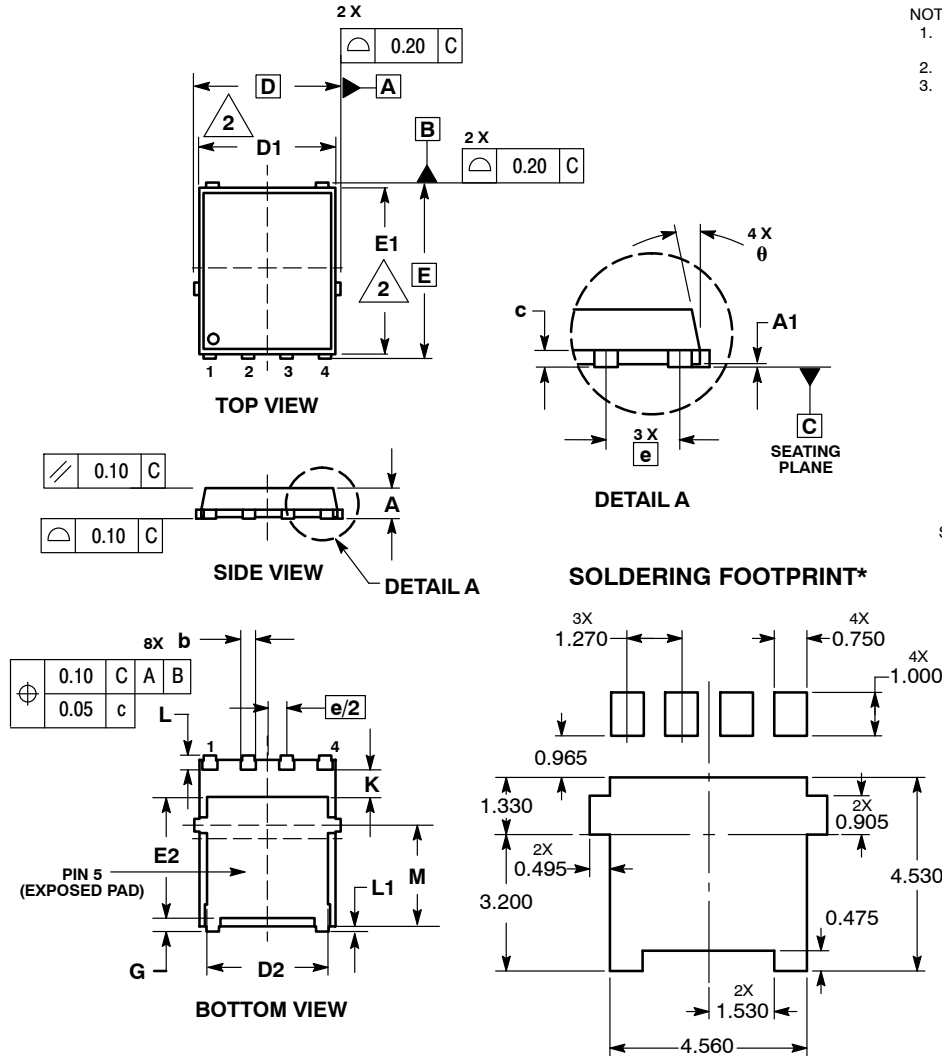


Figure 13.  $g_{FS}$  versus Drain Current

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## PACKAGE DIMENSIONS

DFN5 5x6, 1.27P  
(SO-8FL)  
CASE 488AA  
ISSUE G



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.15 BSC		
D1	4.50	4.90	5.10
D2	3.50	---	4.22
E	6.15 BSC		
E1	5.50	5.80	6.10
E2	3.45	---	4.30
e	1.27 BSC		
G	0.51	0.61	0.71
K	1.20	1.35	1.50
L	0.51	0.61	0.71
L1	0.05	0.17	0.20
M	3.00	3.40	3.80
θ	0°	---	12°

- STYLE 1:  
PIN 1. SOURCE  
2. SOURCE  
3. SOURCE  
4. GATE  
5. DRAIN

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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