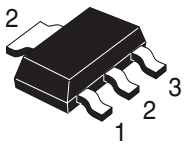
STN1NF10

N-channel 100V - 0.7Ω -1A SOT-223
STripFET™ II Power MOSFET

General features

Type	V_{DSS}	$R_{DS(on)}$	I_D
STN1NF10	100V	<0.8Ω	1A

- Exceptional dv/dt capability

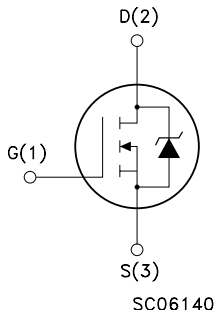


SOT-223

Description

This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

Internal schematic diagram



Applications

- Switching application

Order codes

Part number	Marking	Package	Packaging
STN1NF10	N1NF10	SOT-223	Tape & reel

Contents

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	100	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at T_C = 25°C	1	A
I_D	Drain current (continuous) at T_C=100°C	0.6	A
I_{DM} (1)	Drain current (pulsed)	4	A
P_{TOT}	Total dissipation at T_C = 25°C	2.5	W
	Derating factor	0.02	W/°C
dv/dt (2)	Peak diode recovery voltage slope	20	V/ns
E_{AS} (3)	Single pulse avalanche energy	35	mJ
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150	°C

1. Pulse width limited by safe operating area
2. $I_{SD} \leq 1A$, di/dt ≤350A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$
3. Starting T_j = 25 °C, I_D = 1A, V_{DD} = 70V

Table 2. Thermal data

Rthj-pcb	Thermal Resistance Junction-PCB (1 inch^2 copper board)	50	°C/W
Rthj-pcb	Thermal Resistance Junction-PCB (min. footprint)	90	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose	260	°C

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS}= 0	100			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating, V_{DS} = Max rating @125°C			1 10	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±20V			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10V, I_D= 0.5A		0.7	0.8	Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 15A, I_D = 1A		1		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =25V, f=1 MHz, V_{GS}=0		105 20 9		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}=50V, I_D = 1A V_{GS} =10V		4 1 1.5	6	nC nC nC

1. Pulsed: pulse duration=300µs, duty cycle 1.5%

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	V_{DD} = 50V, I_D = 0.5A, R_G = 4.7Ω, V_{GS} = 10V (see Figure 13)		4 5.5		ns ns
$t_{d(off)}$ t_f	Turn-off-delay time Fall time	V_{DD} = 50V, I_D = 0.5A, R_G = 4.7Ω, V_{GS} = 10V (see Figure 13)		13 6.5		ns ns

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current				1	A
I_{SDM} (1)	Source-drain current (pulsed)				4	A
V_{SD} (2)	Forward on voltage	I_{SD}=1A, V_{GS}=0			1.2	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}=1A, di/dt = 100A/µs, V_{DD}=20V, Tj=150°C (see Figure 15)		45 60 2.7		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration=300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

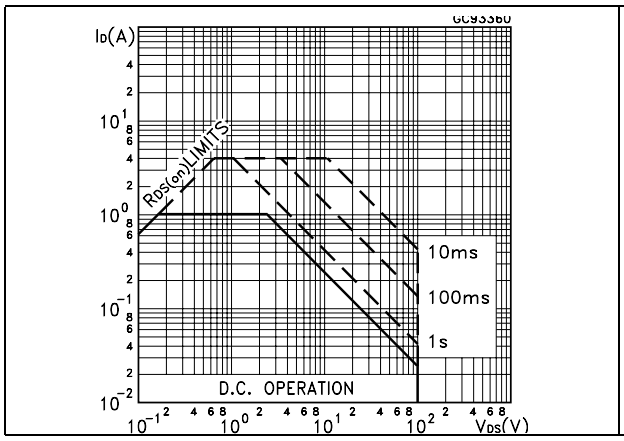


Figure 2. Thermal impedance

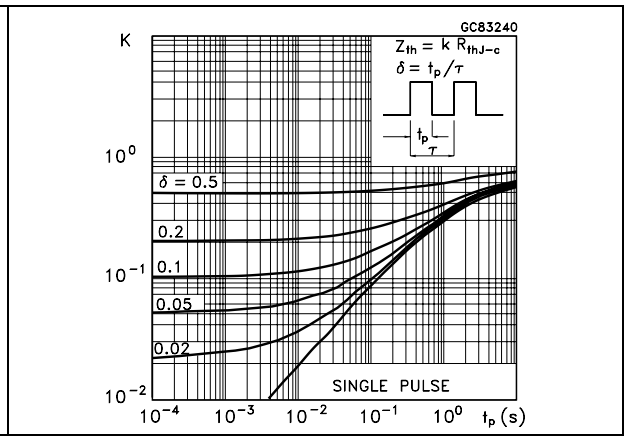


Figure 3. Output characteristics

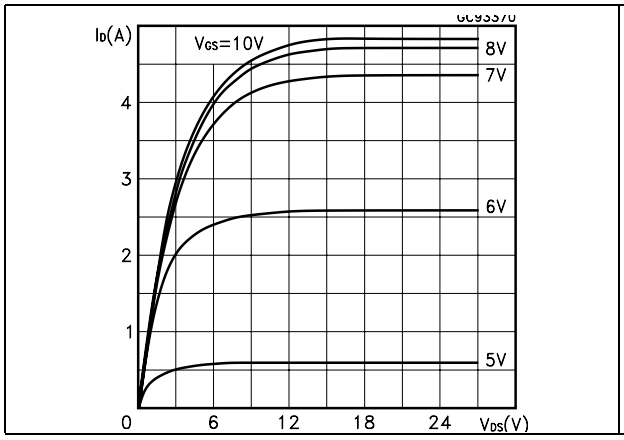


Figure 4. Transfer characteristics

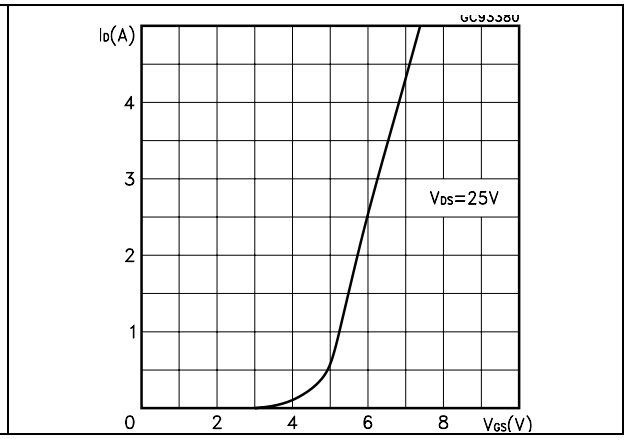


Figure 5. Transconductance

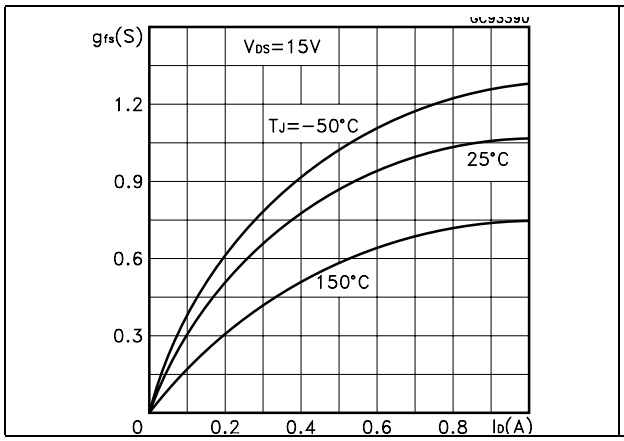


Figure 6. Static drain-source on resistance

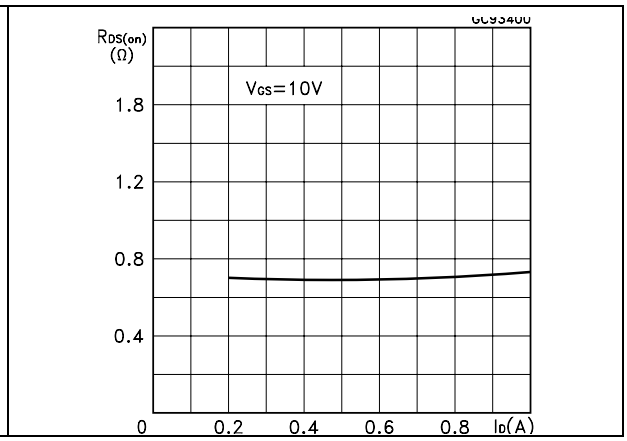


Figure 7. Gate charge vs. gate-source voltage

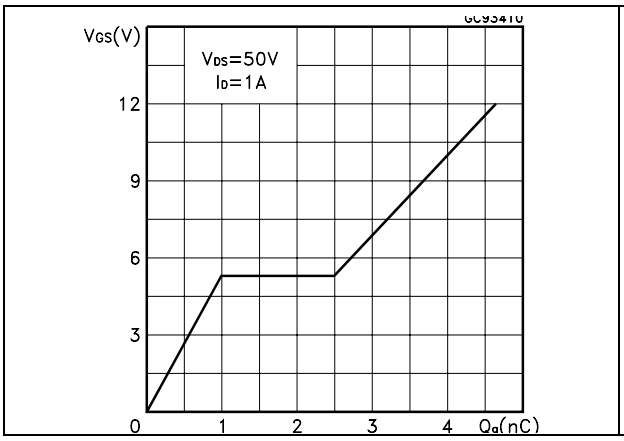


Figure 8. Capacitance variations

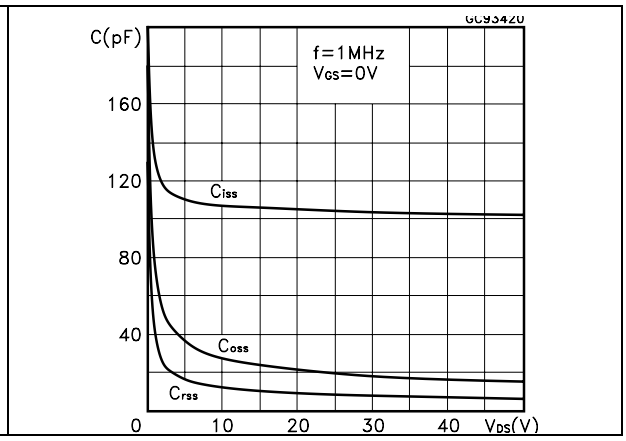


Figure 9. Normalized gate threshold voltage vs. temperature

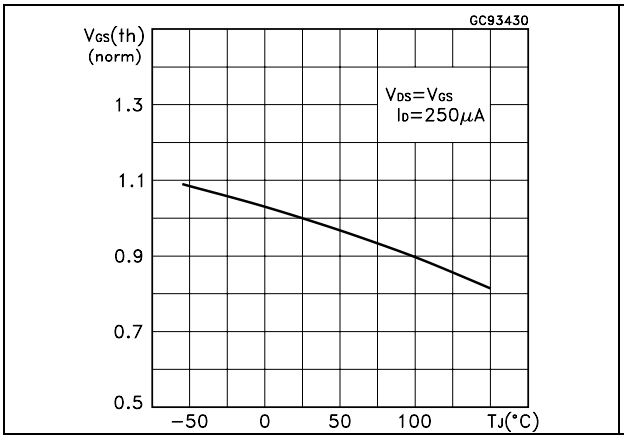


Figure 10. Normalized on resistance vs. temperature

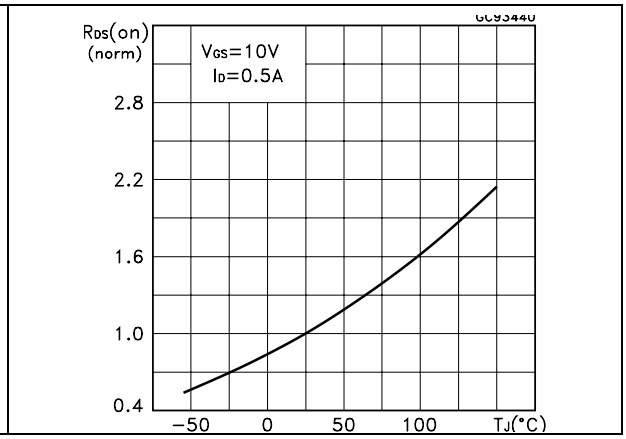


Figure 11. Source-drain diode forward characteristics

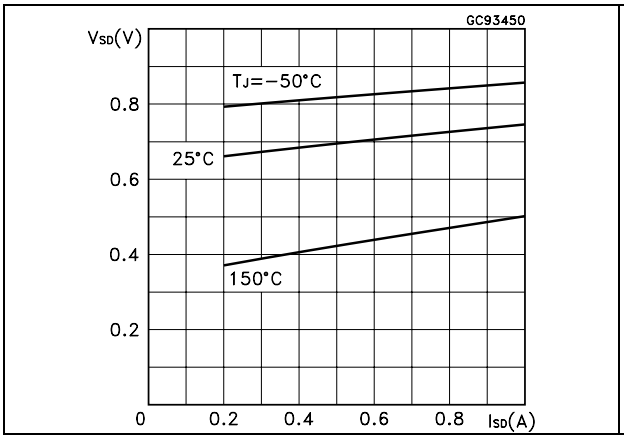
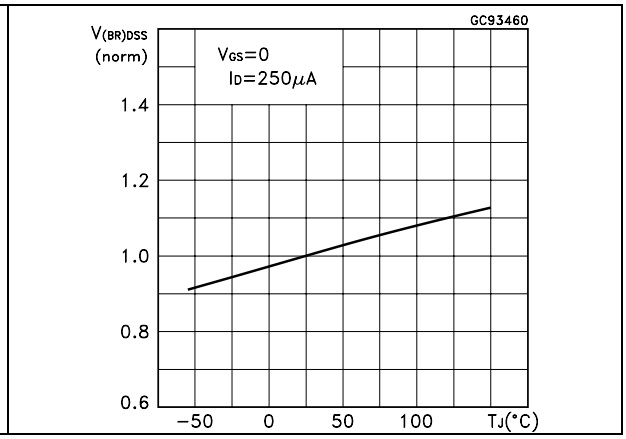


Figure 12. Normalized breakdown voltage temperature



3 Test circuit

Figure 13. Switching times test circuit for resistive load

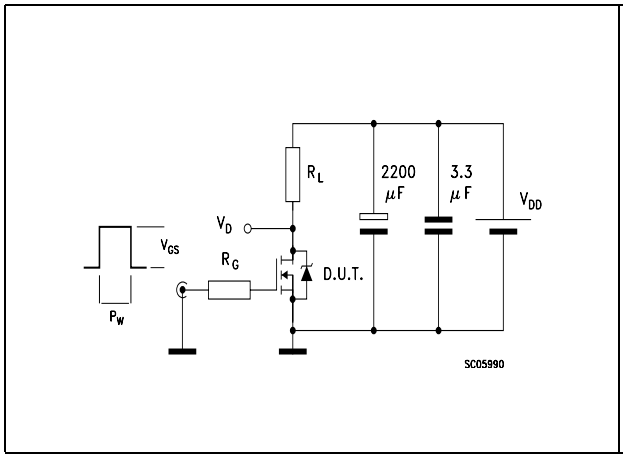


Figure 14. Gate charge test circuit

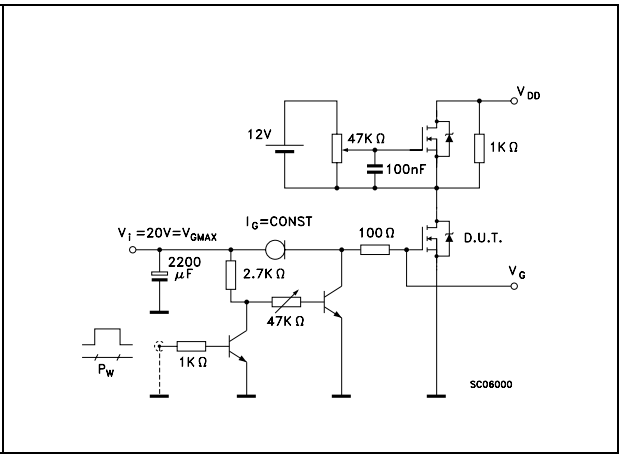


Figure 15. Test circuit for inductive load switching and diode recovery times

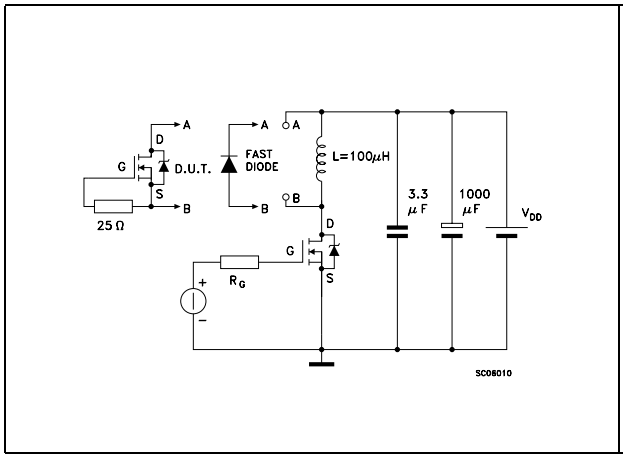


Figure 16. Unclamped Inductive load test circuit

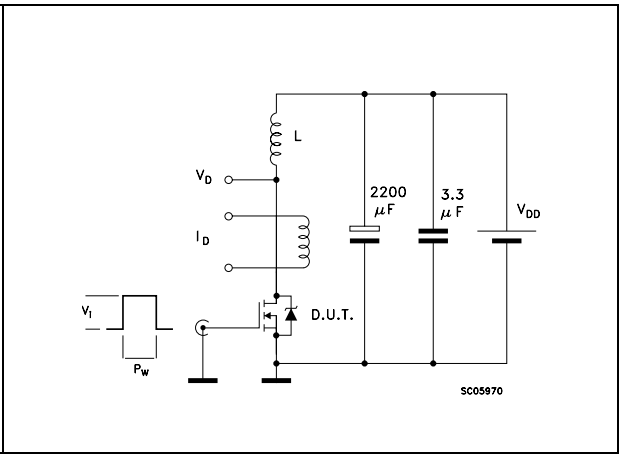


Figure 17. Unclamped inductive waveform

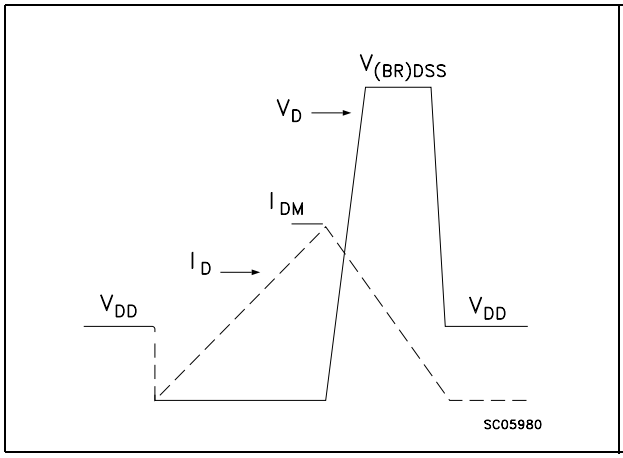
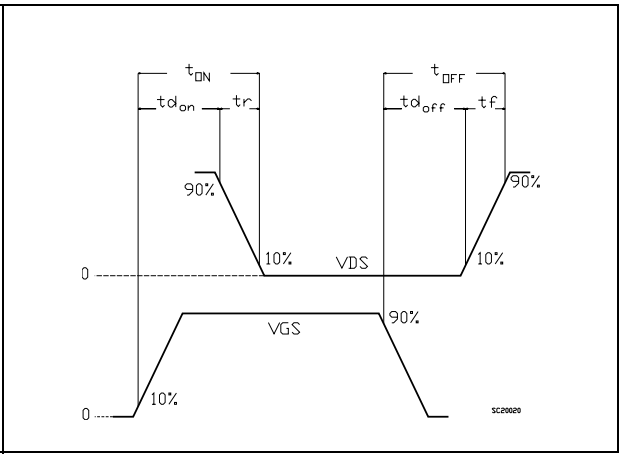


Figure 18. Switching time waveform

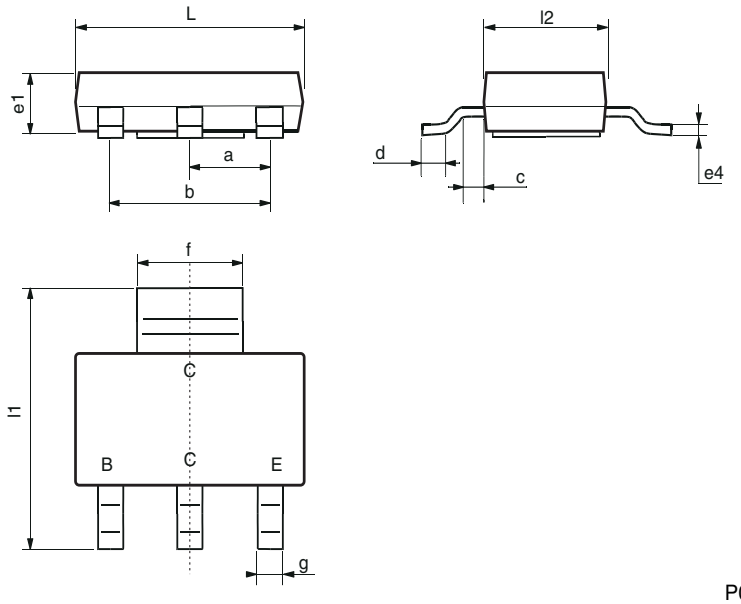


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

SOT-223 MECHANICAL DATA

DIM.	mm			mils		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a	2.27	2.3	2.33	89.4	90.6	91.7
b	4.57	4.6	4.63	179.9	181.1	182.3
c	0.2	0.4	0.6	7.9	15.7	23.6
d	0.63	0.65	0.67	24.8	25.6	26.4
e1	1.5	1.6	1.7	59.1	63	66.9
e4			0.32			12.6
f	2.9	3	3.1	114.2	118.1	122.1
g	0.67	0.7	0.73	26.4	27.6	28.7
l1	6.7	7	7.3	263.8	275.6	287.4
l2	3.5	3.5	3.7	137.8	137.8	145.7
L	6.3	6.5	6.7	248	255.9	263.8



P008B

5 Revision history

Table 7. Revision history

Date	Revision	Changes
21-Jun-2004	1	New document
19-Sep-2006	2	New template, no content change
01-Feb-2007	3	Typo mistake on *Table 1*.

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