

# FCH25N60N

## N-Channel MOSFET

### 600V, 25A, 0.126Ω

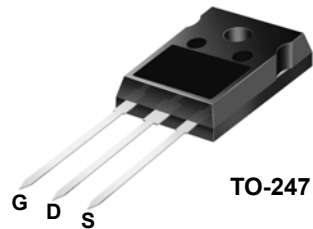
#### Features

- $R_{DS(on)} = 0.108\Omega$  (Typ.) at  $V_{GS} = 10V$ ,  $I_D = 12.5A$
- Ultra Low Gate Charge (Typ.  $Q_g = 57nC$ )
- Low Effective Output Capacitance
- 100% Avalanche Tested
- RoHS Compliant

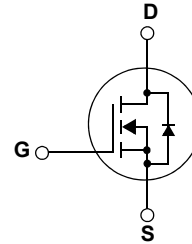
#### Description

The SupreMOS MOSFET, Fairchild's next generation of high voltage super-junction MOSFETs, employs a deep trench filling process that differentiates it from preceding multi-epi based technologies. By utilizing this advanced technology and precise process control, SupreMOS provides world class  $R_{sp}$ , superior switching performance and ruggedness.

This SupreMOS MOSFET fits the industry's AC-DC SMPS requirements for PFC, server/telecom power, FPD TV power, ATX power, and industrial power applications.



TO-247



#### MOSFET Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted\*

Symbol	Parameter	FCH25N60N	Units
$V_{DSS}$	Drain to Source Voltage	600	V
$V_{GSS}$	Gate to Source Voltage	$\pm 30$	V
$I_D$	Drain Current	Continuous ( $T_C = 25^\circ C$ )	25
		Continuous ( $T_C = 100^\circ C$ )	16
$I_{DM}$	Drain Current	Pulsed (Note 1)	75
$E_{AS}$	Single Pulsed Avalanche Energy	(Note 2)	861
$I_{AR}$	Avalanche Current		8.3
$E_{AR}$	Repetitive Avalanche Energy		2.2
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	20
	MOSFET dv/dt		100
$P_D$	Power Dissipation	( $T_C = 25^\circ C$ )	216
		Derate above $25^\circ C$	1.72
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ C$
$T_L$	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ C$

\*Drain current limited by maximum junction temperature

#### Thermal Characteristics

Symbol	Parameter	FCH25N60N	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.58	$^\circ C/W$
$R_{\theta CS}$	Thermal Resistance, Case to Heat Sink (Typical)	0.24	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	40	

## Package Marking and Ordering Information $T_C = 25^\circ\text{C}$ unless otherwise noted

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FCH25N60N	FCH25N60N	TO247	-	-	30

## Electrical Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 1\text{mA}, V_{GS} = 0\text{V}, T_J = 25^\circ\text{C}$	600	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 1\text{mA}$ , Referenced to $25^\circ\text{C}$	-	0.74	-	V/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 480\text{V}, V_{GS} = 0\text{V}$	-	-	10	$\mu\text{A}$
		$V_{DS} = 480\text{V}, T_J = 125^\circ\text{C}$	-	-	100	
$I_{GSS}$	Gate to Body Leakage Current	$V_{GS} = \pm 30\text{V}, V_{DS} = 0\text{V}$	-	-	$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	2.0	-	4.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 12.5\text{A}$	-	0.108	0.126	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 20\text{V}, I_D = 12.5\text{A}$	-	-	-	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 100\text{V}, V_{GS} = 0\text{V}$ $f = 1\text{MHz}$	-	2520	3352	pF
$C_{oss}$	Output Capacitance		-	103	137	pF
$C_{rss}$	Reverse Transfer Capacitance		-	3.2	5	pF
$C_{oss}$	Output Capacitance	$V_{DS} = 380\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	-	55	-	pF
$C_{oss\text{eff}}$	Effective Output Capacitance	$V_{DS} = 0\text{V to } 480\text{V}, V_{GS} = 0\text{V}$	-	262	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 380\text{V}, I_D = 12.5\text{A},$ $V_{GS} = 10\text{V}$ (Note 4)	-	57	74	nC
$Q_{gs}$	Gate to Source Gate Charge		-	10	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		-	18	-	nC
ESR	Equivalent Series Resistance (G-S)	Drain Open, $f = 1\text{MHz}$	-	1	-	$\Omega$

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 380\text{V}, I_D = 12.5\text{A}$ $R_G = 4.7\Omega$ (Note 4)	-	21	52	ns
$t_r$	Turn-On Rise Time		-	22	54	ns
$t_{d(off)}$	Turn-Off Delay Time		-	68	146	ns
$t_f$	Turn-Off Fall Time		-	5	20	ns

### Drain-Source Diode Characteristics

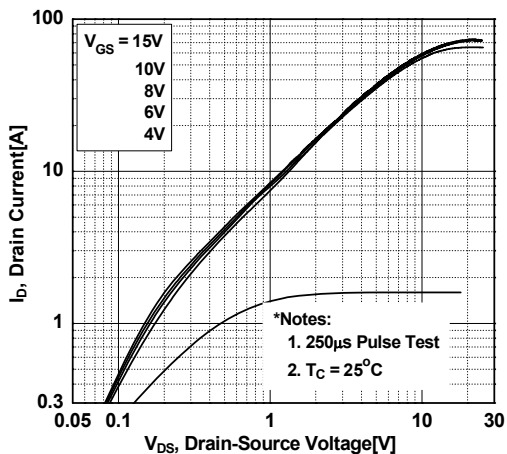
$I_S$	Maximum Continuous Drain to Source Diode Forward Current	-	-	25	A	
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current	-	-	75	A	
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_{SD} = 12.5\text{A}$	-	-	1.2	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{V}, I_{SD} = 12.5\text{A}$ $di_F/dt = 100\text{A}/\mu\text{s}$	-	370	-	ns
$Q_{rr}$	Reverse Recovery Charge		-	7	-	$\mu\text{C}$

#### Notes:

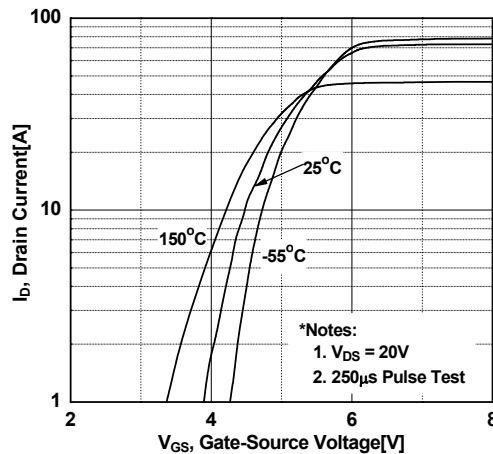
- Repetitive Rating: Pulse width limited by maximum junction temperature
- $I_{AS} = 8.3\text{A}, R_G = 25\Omega$ , Starting  $T_J = 25^\circ\text{C}$
- $I_{SD} \leq 25\text{A}, di/dt \leq 200\text{A}/\mu\text{s}, V_{DD} \leq 380\text{V}$ , Starting  $T_J = 25^\circ\text{C}$
- Essentially Independent of Operating Temperature Typical Characteristics

## Typical Performance Characteristics

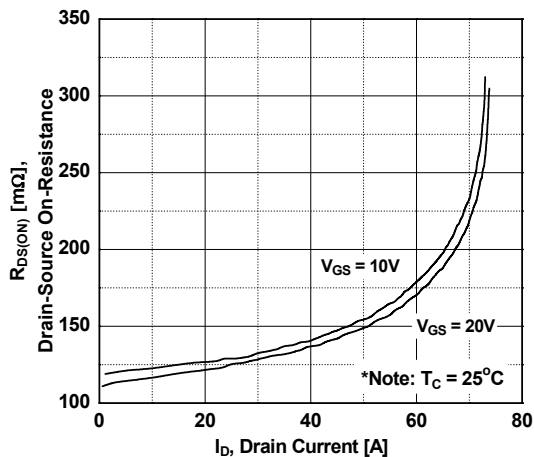
**Figure 1. On-Region Characteristics**



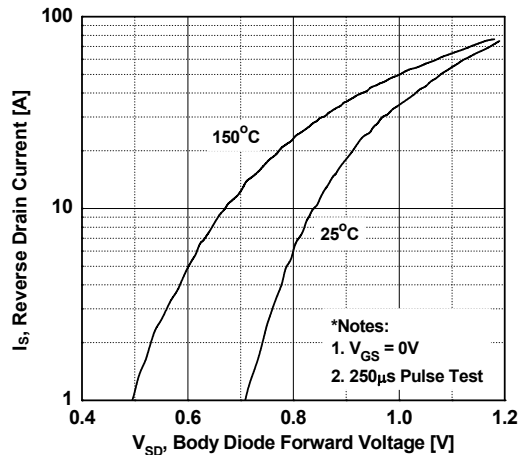
**Figure 2. Transfer Characteristics**



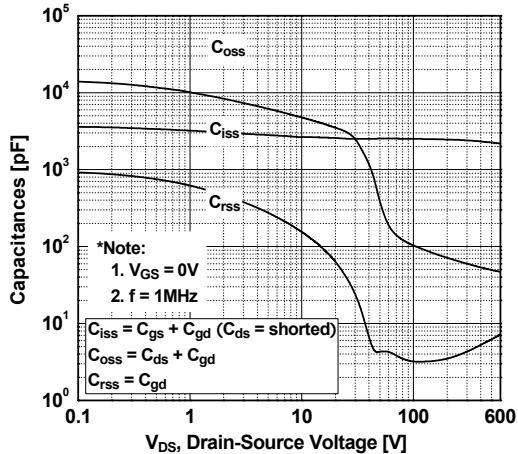
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



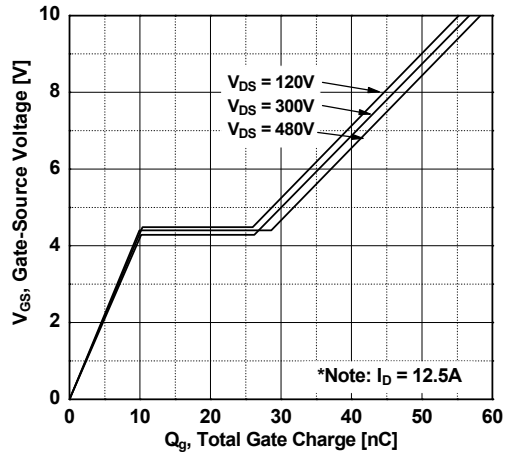
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**

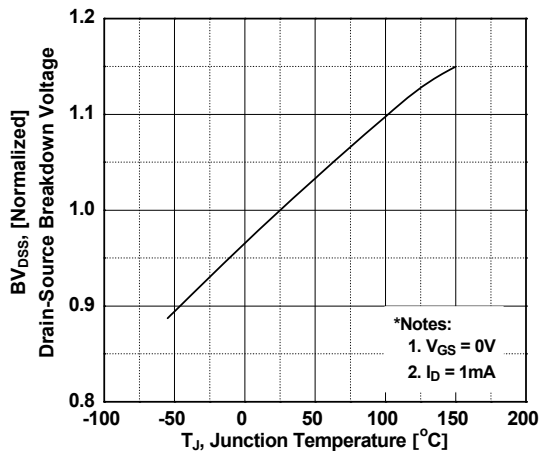


**Figure 6. Gate Charge Characteristics**

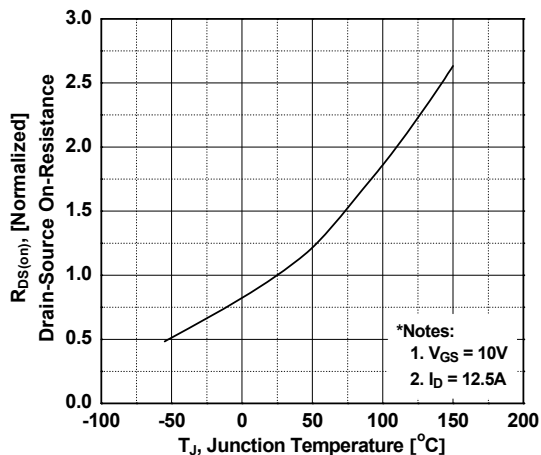


**Typical Performance Characteristics** (Continued)

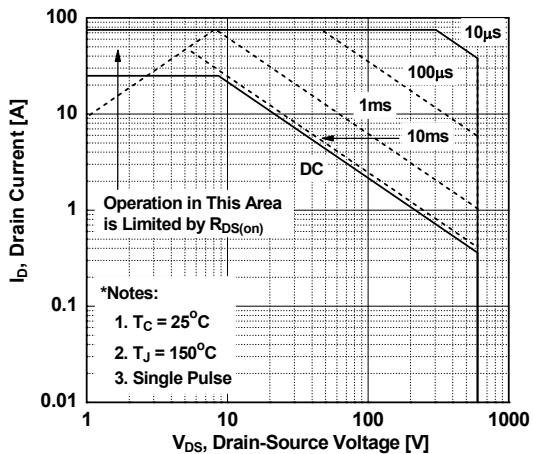
**Figure 7. Breakdown Voltage Variation vs. Temperature**



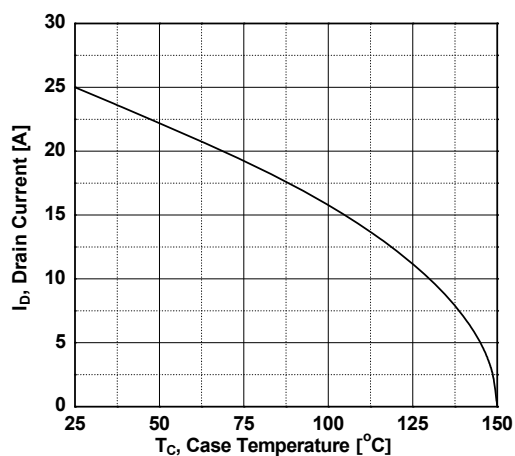
**Figure 8. On-Resistance Variation vs. Temperature**



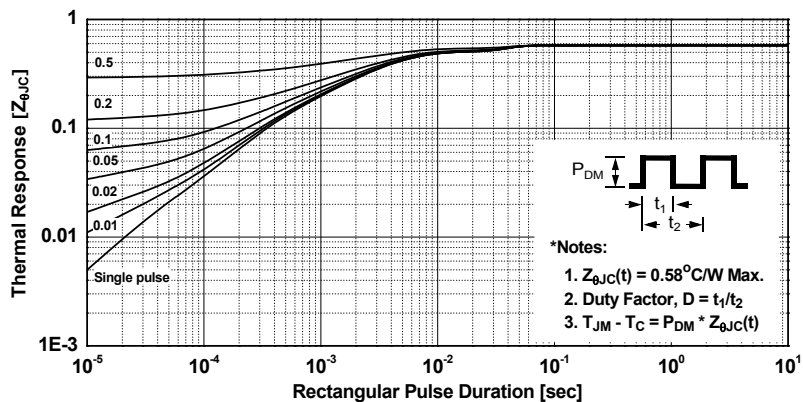
**Figure 9. Maximum Safe Operating Area**



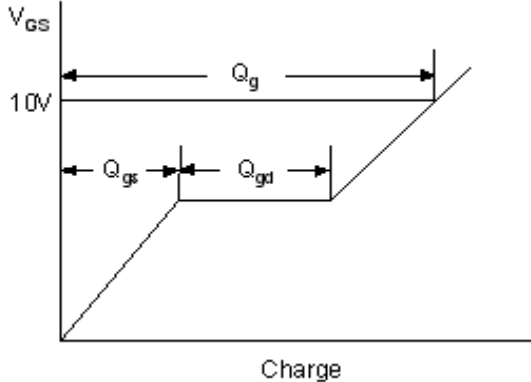
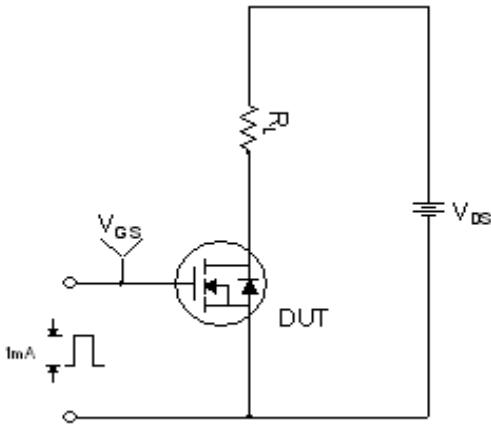
**Figure 10. Maximum Drain Current vs. Case Temperature**



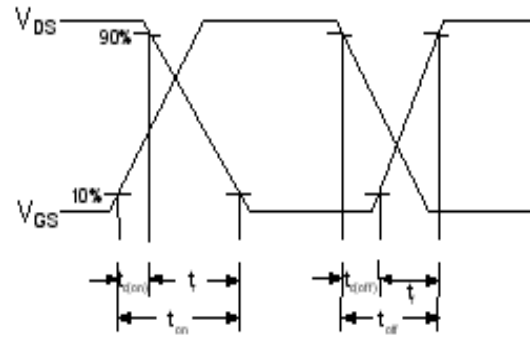
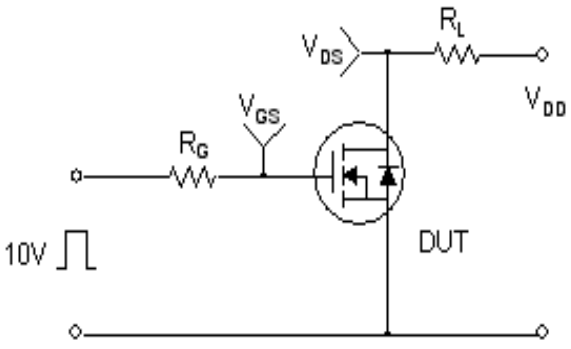
**Figure 11. Transient Thermal Response Curve**



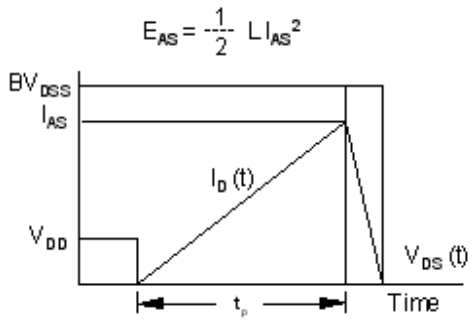
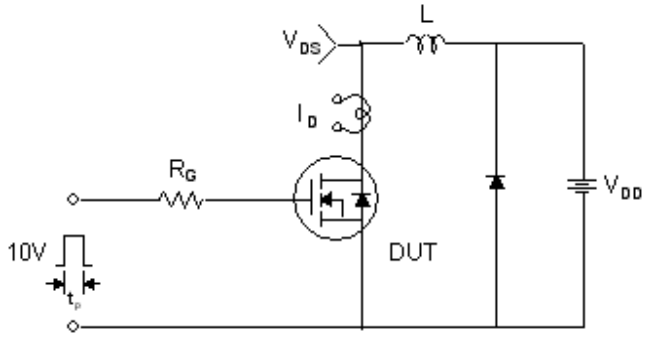
**Gate Charge Test Circuit & Waveform**



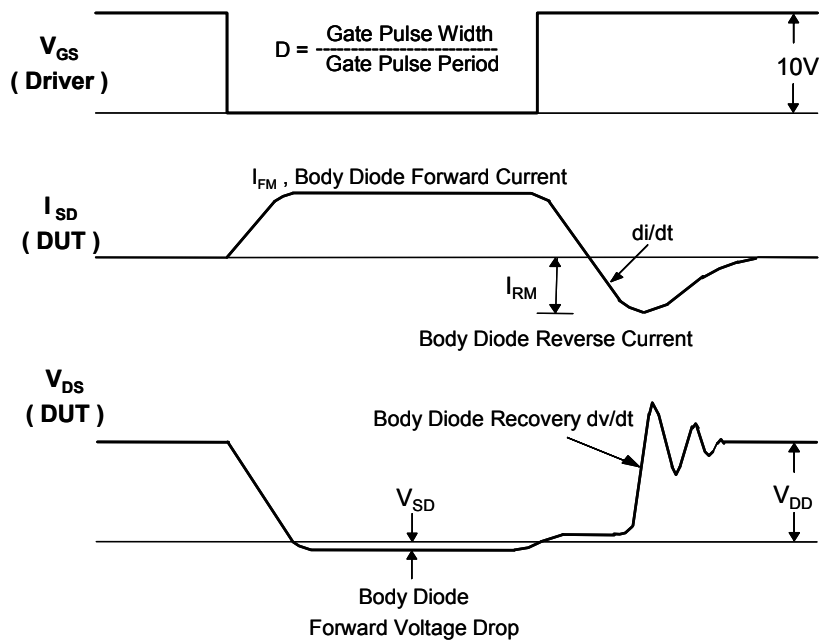
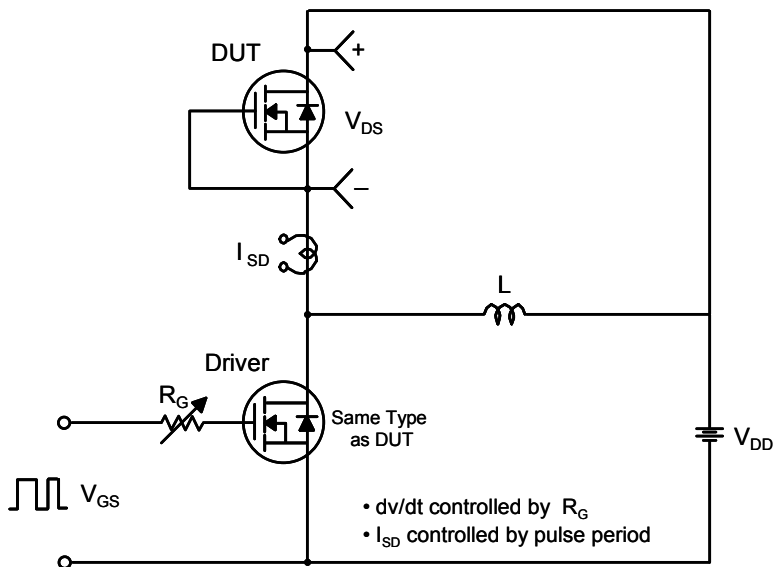
**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching Test Circuit & Waveforms**

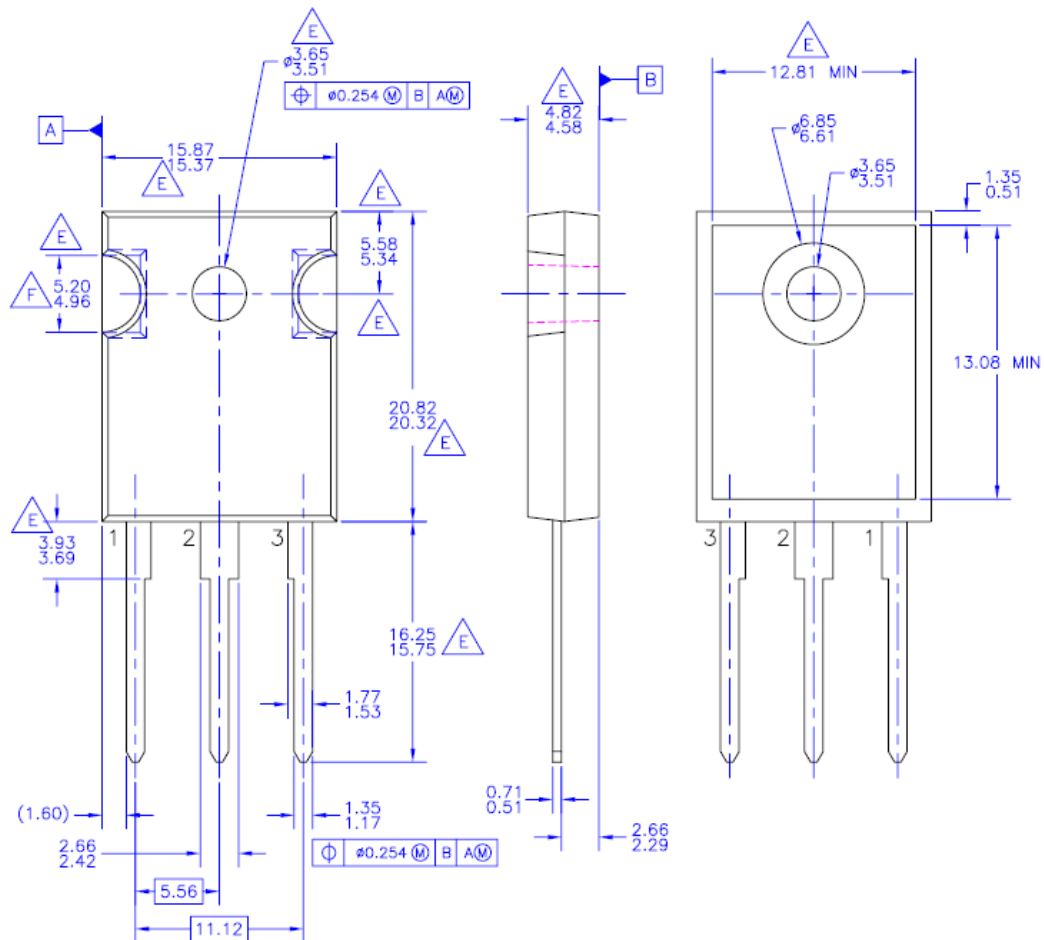


Peak Diode Recovery dv/dt Test Circuit & Waveforms



**Mechanical Dimensions**

**TO-247-3L**



- NOTES: UNLESS OTHERWISE SPECIFIED
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  - DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
  - ALL DIMENSIONS ARE IN MILLIMETERS.
  - DRAWING CONFORMS TO ASME Y14.5 - 1994

**E** DOES NOT COMPLY JEDEC STANDARD VALUE

**F** NOTCH MAY BE SQUARE




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Dimensions in Millimeters



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