

Vishay Siliconix

Automotive N-Channel 60 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	60				
$R_{DS(on)}(\Omega)$ at $V_{GS} = 10 \text{ V}$	0.006				
I _D (A)	120				
Configuration	Single				

TO-263 G D S Top View

N-Channel MOSFET

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- Package with Low Thermal Resistance
- AEC-Q101 Qualifiedd
- 100 % R_q and UIS Tested
- Compliant to RoHS Directive 2002/95/EC



FREE

ORDERING INFORMATION				
Package	TO-263			
Lead (Pb)-free and Halogen-free	SQM110N06-06-GE3			

ABSOLUTE MAXIMUM RATING	S (T _C = 25 °C, unles	s otherwise noted	i)	
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V _{GS}	± 20	
Continuous Drain Current	T _C = 25 °C ^a	1	120	
Continuous Drain Current	T _C = 125 °C	- I _D	80	
Continuous Source Current (Diode Conduction) ^a		I _S	120	Α
Pulsed Drain Current ^b		I _{DM}	480	
Single Pulse Avalanche Current	L = 0.1 mH	I _{AS}	65	
Single Pulse Avalanche Energy	L = 0.1 IIII	E _{AS}	211	mJ
Maximum Power Dissipation ^b	T _C = 25 °C	- P _D	230	W
	T _C = 125 °C		76	VV
Operating Junction and Storage Temperature	T _J , T _{stg}	- 55 to + 175	°C	

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	LIMIT	UNIT	
Junction-to-Ambient	PCB Mount ^c	R_{thJA}	40	°C/W	
Junction-to-Case (Drain)		R _{thJC}	0.65	C/VV	

Notes

- a. Package limited.
- b. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.
- c. When mounted on 1" square PCB (FR-4 material).
- d. Parametric verification ongoing.



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PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static					•			
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0, I_D = 250 \mu A$		60		-	V	
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$		2.5	3.0	3.5		
Gate-Source Leakage	I _{GSS}	V _{DS} =	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$		-	± 100	nA	
		V _{GS} = 0 V	V _{DS} = 60 V	-	-	1.0		
Zero Gate Voltage Drain Current	I _{DSS}	$V_{GS} = 0 V$	V _{DS} = 60 V, T _J = 125 °C	-	-	50	μΑ	
		V _{GS} = 0 V	V _{DS} = 60 V, T _J = 175 °C	-	-	250	7	
On-State Drain Current ^a	I _{D(on)}	V _{GS} = 10 V	$V_{DS} \ge 5 V$	120	-	-	Α	
		V _{GS} = 10 V	I _D = 30 A	-	0.0045	0.0060		
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V	I _D = 30 A, T _J = 125 °C	-	-	0.0104	Ω	
		V _{GS} = 10 V	I _D = 30 A, T _J = 175 °C	-	-	0.0129		
Forward Transconductanceb	9 _{fs}	V _{DS} = 15 V, I _D = 30 A		-	94	-	S	
Dynamic ^b								
Input Capacitance	C _{iss}			-	5196	6495		
Output Capacitance	Coss	$V_{GS} = 0 V$	$V_{DS} = 25 \text{ V}, f = 1 \text{ MHz}$	-	708	885	pF	
Reverse Transfer Capacitance	C _{rss}			ı	336	420		
Total Gate Charge ^c	Qg			1	96.5	145		
Gate-Source Charge ^c	Q_{gs}	V _{GS} = 10 V	$V_{DS} = 30 \text{ V}, I_D = 75 \text{ A}$	-	24.6	-	nC	
Gate-Drain Charge ^c	Q_{gd}			-	27.2	-		
Gate Resistance	R_{g}		f = 1 MHz		1.2	1.7	Ω	
Turn-On Delay Time ^c	t _{d(on)}				16	24		
Rise Time ^c	t _r	$V_{DD}=30$ V, $R_{L}=0.4$ Ω $I_{D}\cong75$ A, $V_{GEN}=10$ V, $R_{g}=1$ Ω		-	14	21	ns .	
Turn-Off Delay Time ^c	t _{d(off)}			-	34	51		
Fall Time ^c	t _f			-	9	14		
Source-Drain Diode Ratings and Chara	acteristics ^b							
Pulsed Current ^a	I _{SM}			1	-	480	Α	
Forward Voltage	V_{SD}	I _F = 75 A, V _{GS} = 0		-	0.9	1.5	V	

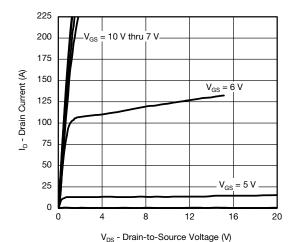
Notes

- a. Pulse test; pulse width $\leq 300~\mu s,~duty~cycle \leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

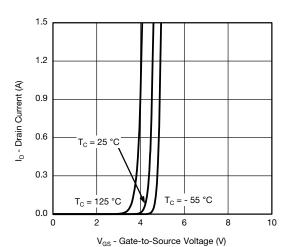
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



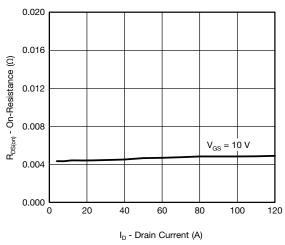
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



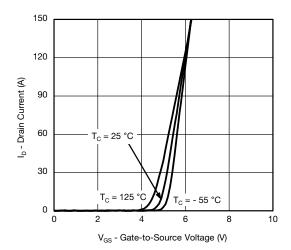
Output Characteristics



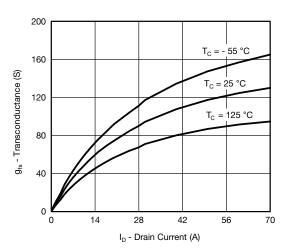
Transfer Characteristics



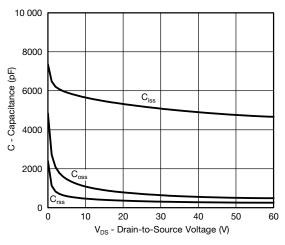
On-Resistance vs. Drain Current



Transfer Characteristics



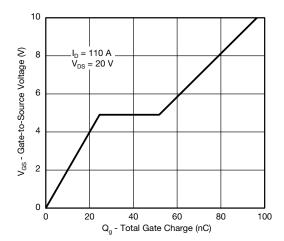
Transconductance



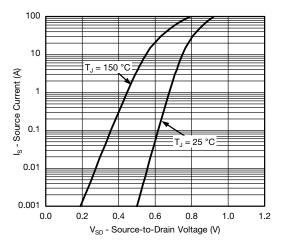
Capacitance



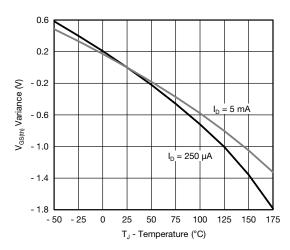
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



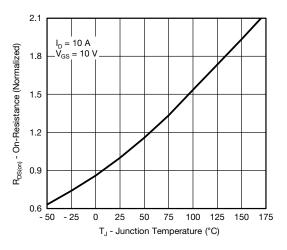
Gate Charge



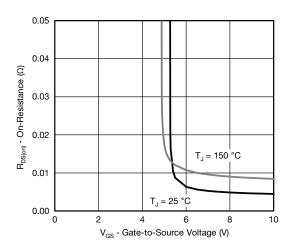
Source Drain Diode Forward Voltage



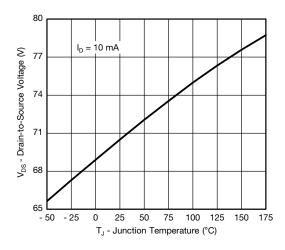
Threshold Voltage



On-Resistance vs. Junction Temperature



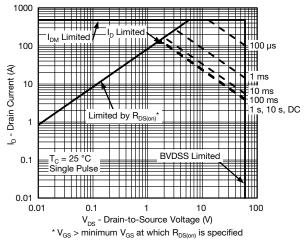
On-Resistance vs. Gate-to-Source Voltage



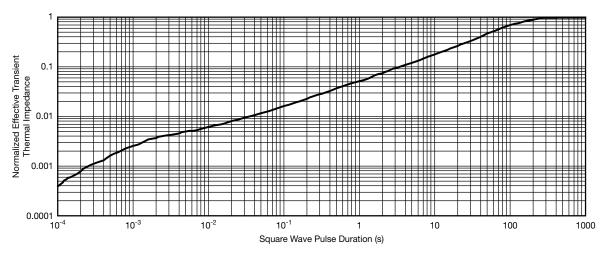
Drain Source Breakdown vs. Junction Temperature



THERMAL RATINGS ($T_A = 25$ °C, unless otherwise noted)



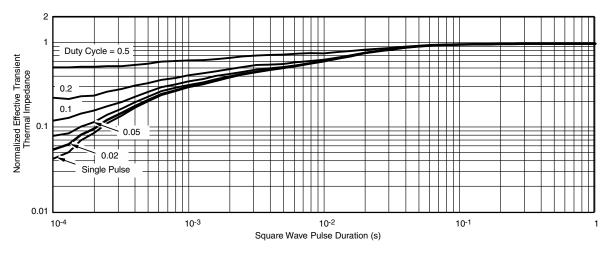
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient

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THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

Note

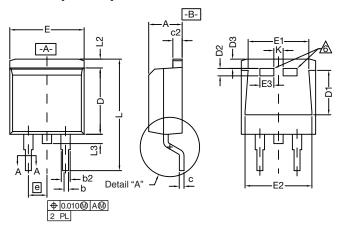
- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
 - Normalized Transient Thermal Impedance Junction-to-Case (25 °C) are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

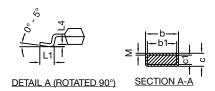
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg269065.





TO-263 (D²PAK): 3-LEAD





		INCHES		MILLIN	METERS
DIM.		MIN.	MAX.	MIN.	MAX.
Α		0.160	0.190	4.064	4.826
	b	0.020	0.039	0.508	0.990
	b1	0.020	0.035	0.508	0.889
	b2	0.045	0.055	1.143	1.397
c*	Thin lead	0.013	0.018	0.330	0.457
	Thick lead	0.023	0.028	0.584	0.711
c1	Thin lead	0.013	0.017	0.330	0.431
CI	Thick lead	0.023	0.027	0.584	0.685
	c2	0.045	0.055	1.143	1.397
D		0.340	0.380	8.636	9.652
D1		0.220	0.240	5.588	6.096
D2		0.038	0.042	0.965	1.067
D3		0.045	0.055	1.143	1.397
E		0.380	0.410	9.652	10.414
E1		0.245	-	6.223	-
E2		0.355	0.375	9.017 9.5	
E3		0.072	0.078	1.829	1.981
	e 0.100 BSC 2.54 BSC		BSC		
K		0.045	0.055	1.143	1.397
L		0.575	0.625	14.605	15.875
L1		0.090	0.110	2.286	2.794
L2		0.040	0.055	1.016	1.397
L3		0.050	0.070	1.270	1.778
L4		0.010 BSC		0.254 BSC	
М		-	0.002	-	0.050
ECN: T10-0738-Rev. J, 03-Jan-11 DWG: 5843					

Notes

- 1. Plane B includes maximum features of heat sink tab and plastic.
- 2. No more than 25 % of L1 can fall above seating plane by max.
- 3. Pin-to-pin coplanarity max. 4 mils.
- 4. *: Thin lead is for SUB, SYB. Thick lead is for SUM, SYM, SQM.





RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads Dimensions in Inches/(mm)

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