FAIRCHILD SEMICONDUCTOR®

October 2011

FDP027N08B_F102

N-Channel PowerTrench® MOSFET

80V, 223A, 2.7mΩ

Features

- $R_{DS(on)}$ = 2.21mΩ (Typ.) @ V_{GS} = 10V, I_D = 100A
- Low FOM $R_{DS(on)} * Q_G$
- Low reverse recovery charge, Q_{rr}
- Soft reverse recovery body diode
- Enables highly efficiency in synchronous rectification
- Fast Switching Speed
- 100% UIL Tested
- RoHS Compliant

Description

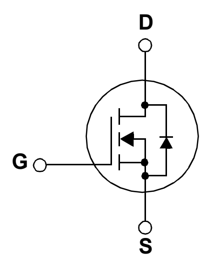
This N-Channel MOSFET is produced using Fairchild Semiconductor's advance PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

Application

- Synchronous Rectification for Server / Telecom PSU
- Battery Charger and Battery Protection circuit
- DC motor drives and Uninterruptible Power Supplies
- Micro Solar Inverter

G D S

TO-220



MOSFET Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain to Source Voltage		80	V
V_{GSS}	Gate to Source Voltage		±20	V
I_D	Drain Current	-Continuous (T_C = 25°C, Silicon Limited)	223*	A
		-Continuous (T_C = 100°C, Silicon Limited)	158*	
		-Continuous (T_C = 25°C, Package Limited)	120	
I_{DM}	Drain Current	- Pulsed (Note 1)	892	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		917	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		6.0	V/ns
P_D	Power Dissipation	(T_C = 25°C)	246	W
		- Derate above 25°C	1.64	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +175	°C
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds		300	°C

*Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 120A

Thermal Characteristics

Symbol	Parameter	Ratings	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.61	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	62.5	

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Package Marking and Ordering Information

Device Marking	Device	Package	Description	Quantity
FDP027N08B	FDP027N08B_F102	TO-220	F102: Trimmed Leads	50

Electrical Characteristics $T_C = 25^oC$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu A$, $V_{GS} = 0V$	80	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu A$, Referenced to 25^oC	-	0.05	-	$V/^oC$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 64V$, $V_{GS} = 0V$	-	-	1	μA
		$V_{DS} = 64V$, $T_C = 150^oC$	-	-	500	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20V$, $V_{DS} = 0V$	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu A$	2.5	-	4.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10V$, $I_D = 100A$	-	2.21	2.7	mΩ
g_{FS}	Forward Transconductance	$V_{DS} = 10V$, $I_D = 100A$ (Note 4)	-	227	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 40V$, $V_{GS} = 0V$ f = 1MHz	-	10170	13530	pF
C_{oss}	Output Capacitance		-	1670	2220	pF
C_{rss}	Reverse Transfer Capacitance		-	35	-	pF
$C_{oss}(er)$	Engry Related Output Capacitance	$V_{DS} = 40V$, $V_{GS} = 0V$	-	3025	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 40V$, $V_{GS} = 10V$ $I_D = 100A$ (Note 4, 5)	-	137	178	nC
Q_{gs}	Gate to Source Gate Charge		-	56	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau		-	25	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	28	-	nC
ESR	Equivalent Series Resistance (G-S)	Drain Open, f = 1MHz	-	2.4	-	Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 40V$, $I_D = 100A$ $V_{GS} = 10V$, $R_{GEN} = 4.7\Omega$ (Note 4, 5)	-	47	104	ns
t_r	Turn-On Rise Time		-	66	142	ns
$t_{d(off)}$	Turn-Off Delay Time		-	87	184	ns
t_f	Turn-Off Fall Time		-	41	92	ns
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	223*	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	892	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0V$, $I_{SD} = 100A$	-	-	1.3	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0V$, $V_{DD} = 40V$, $I_{SD} = 100A$ $dI_F/dt = 100A/\mu s$ (Note 4)	-	80	-	ns
Q_{rr}	Reverse Recovery Charge		-	112	-	nC

Notes:
1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. L = 3mH, $I_{AS} = 24.72A$, $R_G = 25\Omega$, Starting $T_J = 25°C$
3. $I_{SD} \le 100A$, $di/dt \le 200A/\mu s$, $V_{DD} \le BV_{DSS}$, Starting $T_J = 25°C$
4. Pulse Test: Pulse width ≤ 300μs, Dual Cycle ≤ 2%
5. Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

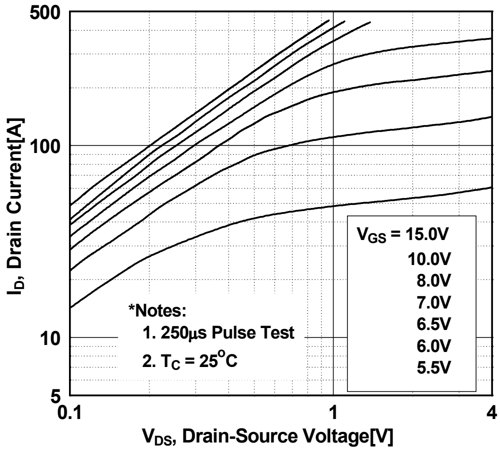


Figure 2. Transfer Characteristics

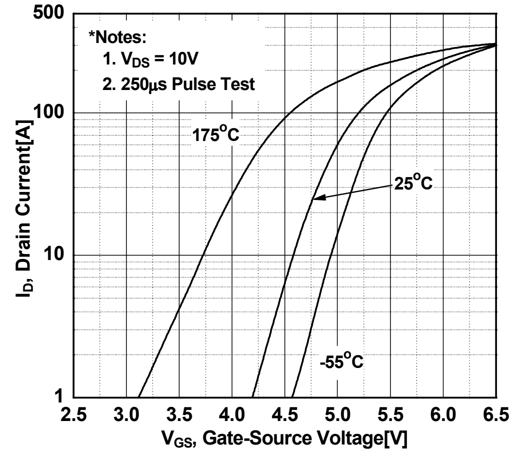


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

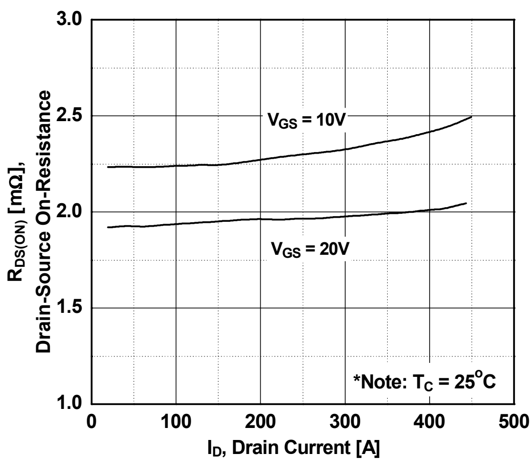


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

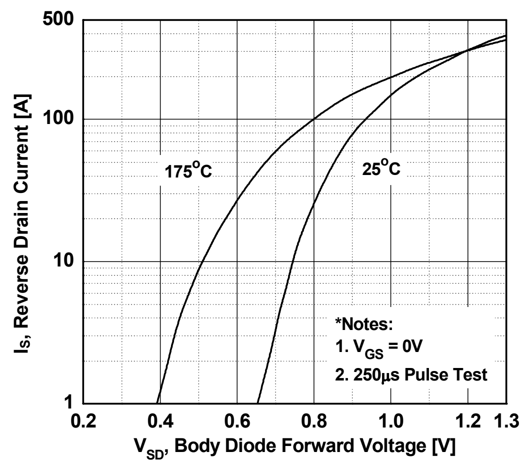


Figure 5. Capacitance Characteristics

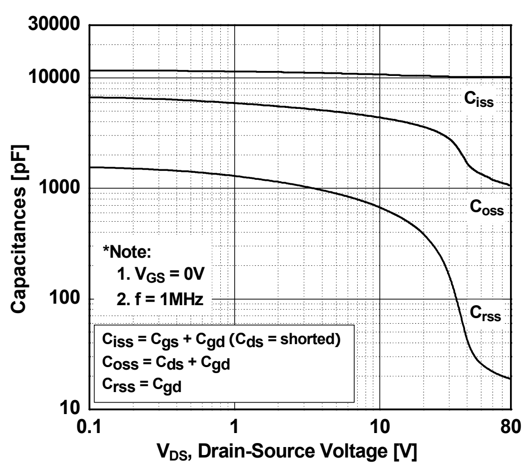
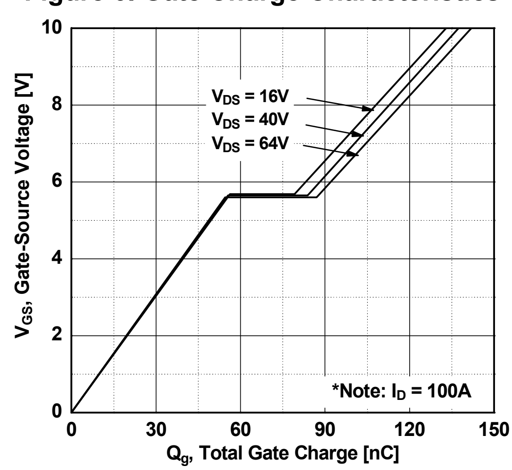


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

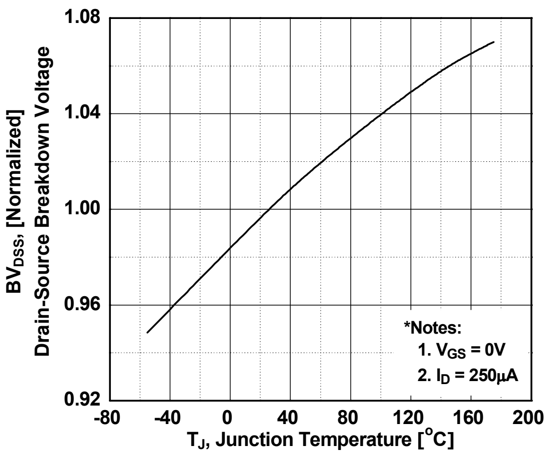


Figure 8. On-Resistance Variation vs. Temperature

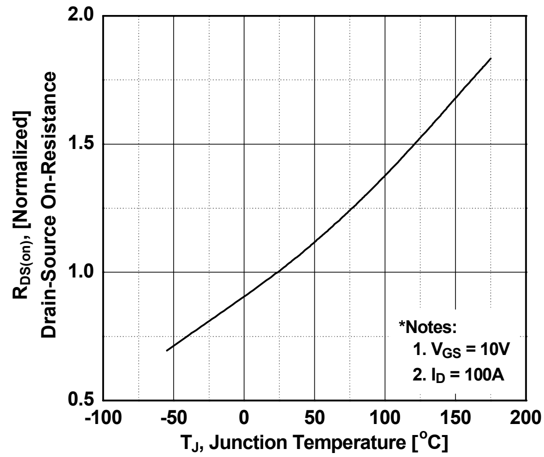


Figure 9. Maximum Safe Operating Area vs. Case Temperature

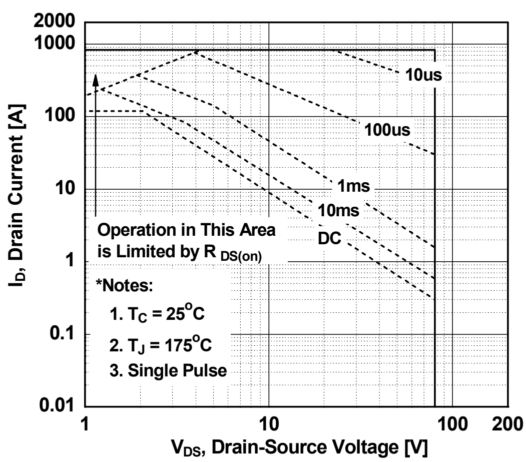


Figure 10. Maximum Drain Current

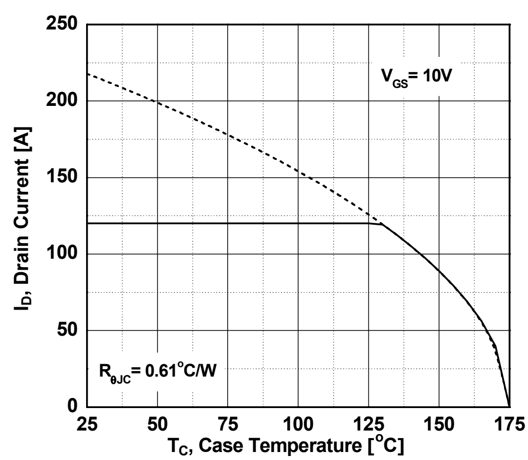


Figure 11. Eoss vs. Drain to Source Voltage Switching Capability

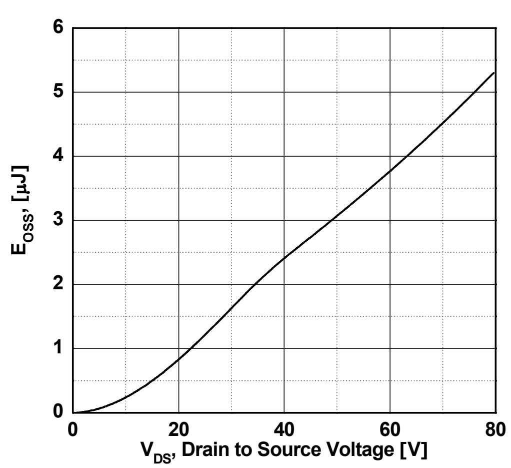
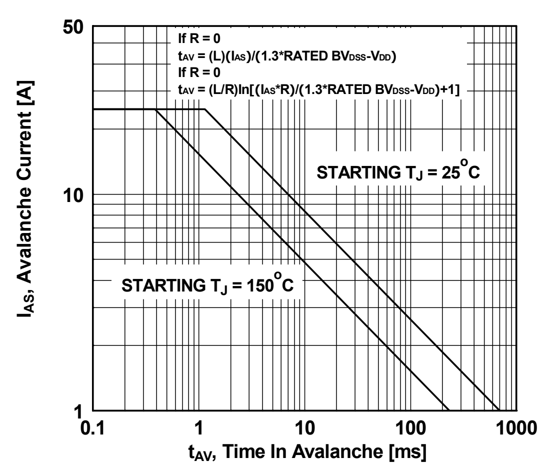
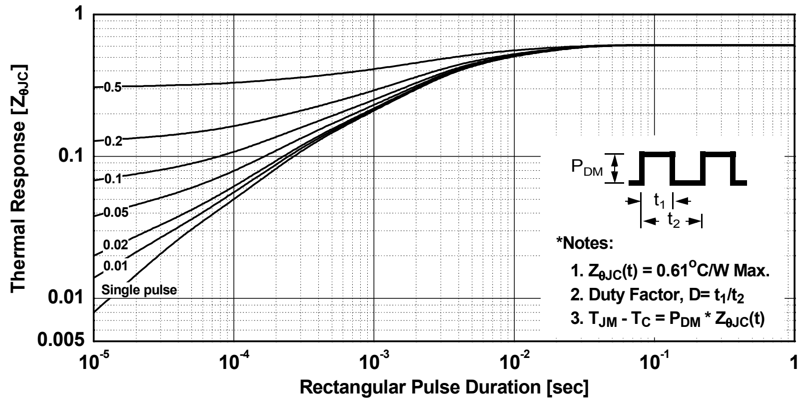


Figure 12. Unclamped Inductive

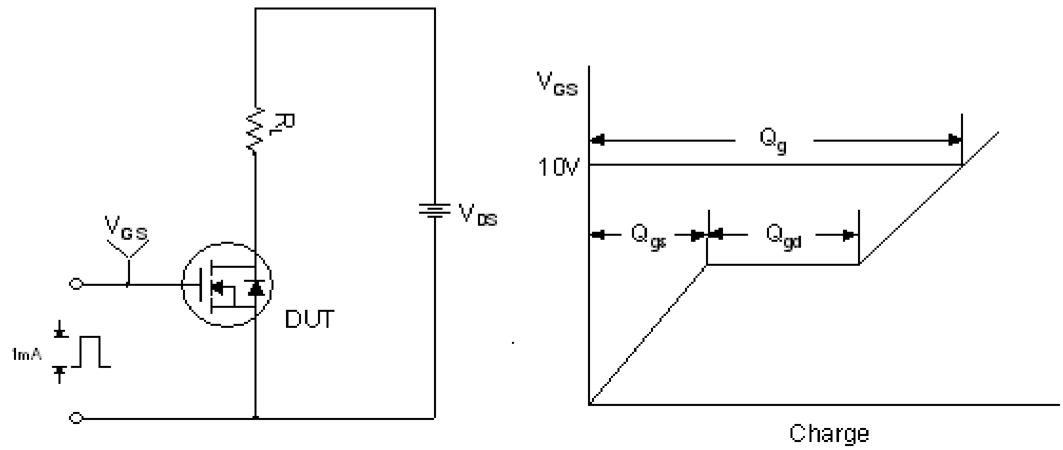


Typical Performance Characteristics (Continued)

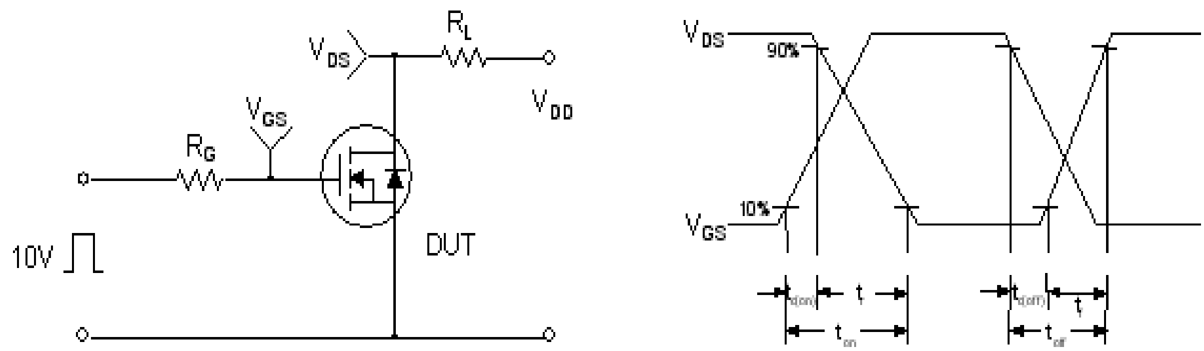
Figure 12. Transient Thermal Response Curve



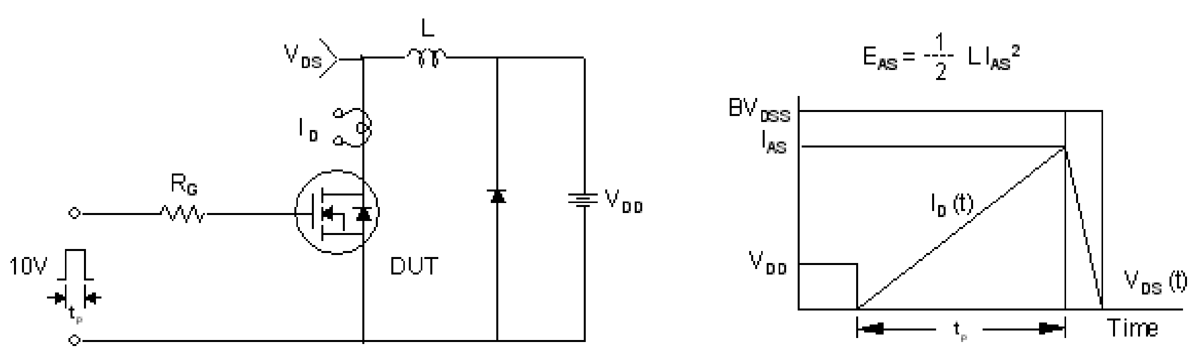
Gate Charge Test Circuit & Waveform



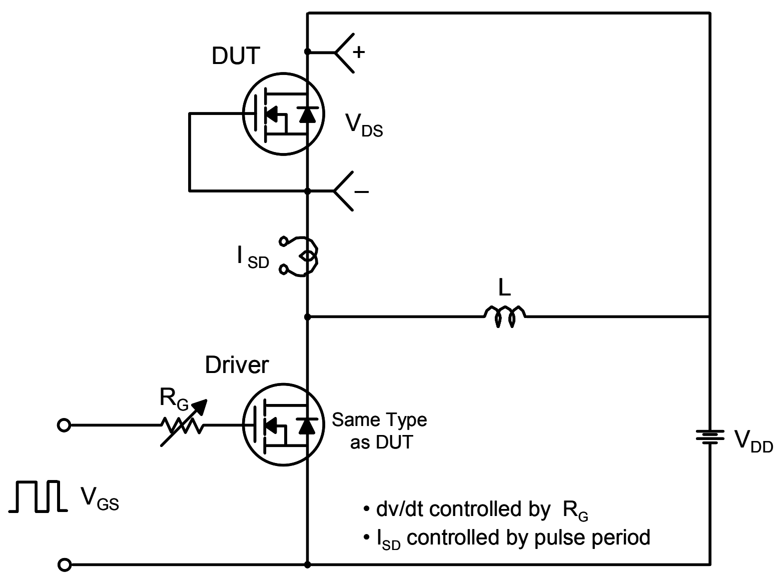
Resistive Switching Test Circuit & Waveforms

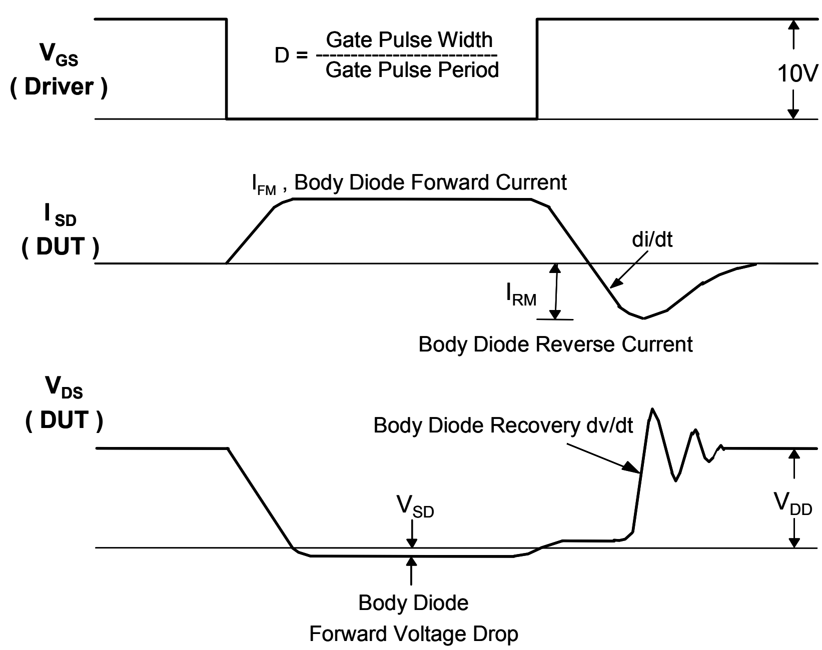


Unclamped Inductive Switching Test Circuit & Waveforms



Peak Diode Recovery dv/dt Test Circuit & Waveforms

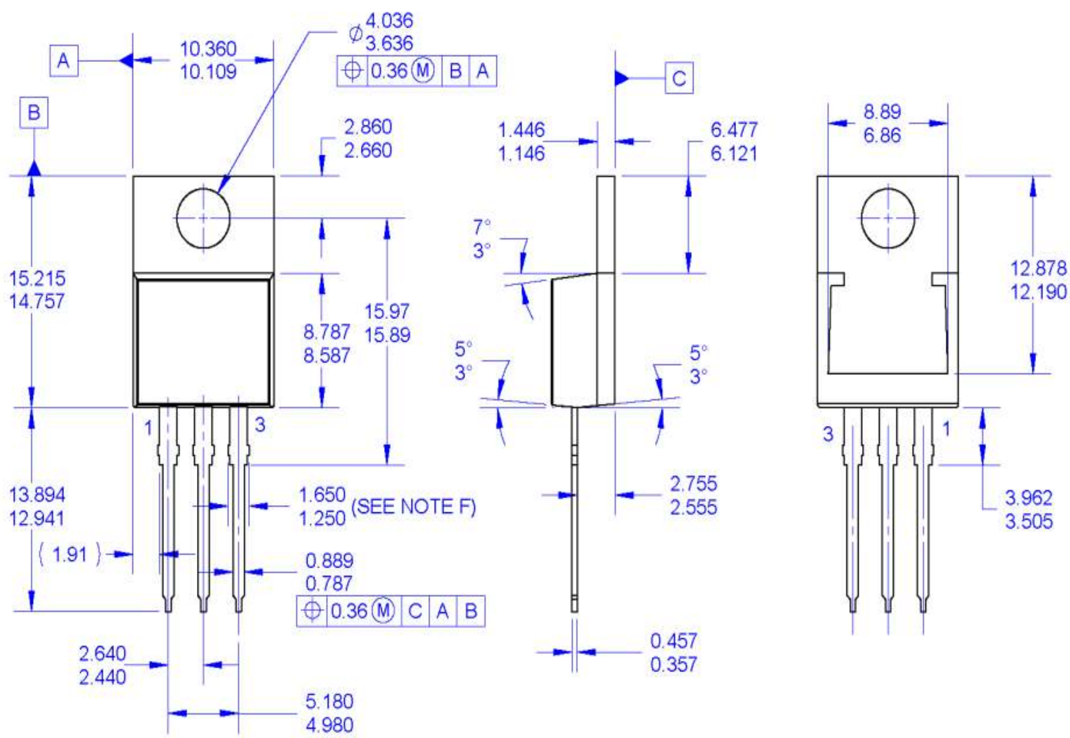


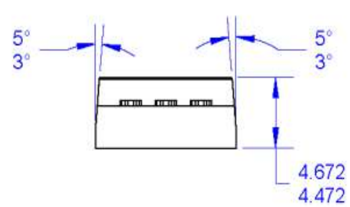


Package Dimensions

TO-220

F102: Trimmed Leads





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