

# N-Channel 100-V (D-S) MOSFET

PRODUCT	SUMMARY		
V <sub>DS</sub> (V)	<b>R<sub>DS(on)</sub> (Ω)</b>	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ.)
100	0.0183 at $V_{GS}$ = 10 V	60	48
100	0.023 at $V_{GS}$ = 8.0 V	53	40

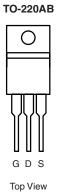
Ordering Information: SUP60N10-18P-E3 (Lead (Pb)-free)

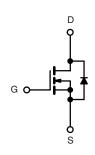
### **FEATURES**

- TrenchFET<sup>®</sup> Power MOSFET
- 100 %  $\rm R_g$  and UIS Tested
- Compliant to RoHS Directive 2002/95/EC

### **APPLICATIONS**

- Industrial
- Power Supply





N-Channel MOSFET

<b>ABSOLUTE MAXIMUM RATINGS</b> $T_C = 25 \degree C$ , unless otherwise noted						
Parameter		Symbol	Limit	Unit		
Drain-Source Voltage		V <sub>DS</sub>	100	N		
Gate-Source Voltage		V <sub>GS</sub>	± 20	V		
Continuous Drain Current ( $T_1 = 175 \text{ °C}$ )	T <sub>C</sub> = 25 °C	Ι <sub>D</sub>	60			
	T <sub>C</sub> = 70 °C		50			
Pulsed Drain Current		I <sub>DM</sub>	100			
Avalanche Current		I <sub>AS</sub>	45			
Single Avalanche Energy <sup>a</sup>	L = 0.1 mH	E <sub>AS</sub>	101	mJ		
	T <sub>C</sub> = 25 °C	Р	150 <sup>b</sup>	14/		
Maximum Power Dissipation <sup>a</sup>	um Power Dissipation <sup>a</sup> $P_D$ $T_A = 25 \ ^{\circ}C^{c}$		3.75	vv		
Operating Junction and Storage Temperature R	ange	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 175	°C		

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Limit	Unit
Junction-to-Ambient (PCB Mount) <sup>c</sup>	R <sub>thJA</sub>	40	°C/W
Junction-to-Case (Drain)	R <sub>thJC</sub>	1.0	C/VV

Notes:

a. Duty cycle  $\leq$  1 %.

b. See SOA curve for voltage derating.

c. When Mounted on 1" square PCB (FR-4 material).

# SUP60N10-18P

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{DS} = 0 \text{ V}, \text{ I}_{D} = 250 \mu\text{A}$	100			v
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250 \ \mu A$	2.5		4.5	v
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 V$ , $V_{GS} = \pm 20 V$			± 250	nA
		$V_{DS} = 100 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$			1	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{DS}$ = 100 V, $V_{GS}$ = 0 V, $T_{J}$ = 125 °C			50	μA
		$V_{DS}$ = 100 V, $V_{GS}$ = 0 V, $T_{J}$ = 175 °C			250	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 10 \text{ V}, \text{ V}_{GS} = 10 \text{ V}$	50			А
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 15 A		0.015	0.0183	
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS}$ = 10 V, I <sub>D</sub> = 15 A, T <sub>J</sub> = 125 °C		0.027	0.033	Ω S pF
		V <sub>GS</sub> = 8.0 V, I <sub>D</sub> = 10 A		0.018	0.023	
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 15 A		33		S
Dynamic <sup>b</sup>	•					
Input Capacitance	C <sub>iss</sub>			2600		pF
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 50 V, f = 1 MHz		230		
Reverse Transfer Capacitance	C <sub>rss</sub>			80		
Total Gate Charge <sup>c</sup>	Qg			48	75	
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>	$V_{DS} = 50 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 50 \text{ A}$		16		nC
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			13		
Gate Resistance	Rg	f = 1 MHz	0.25	1.1	2.4	Ω
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>			12	20	
Rise Time <sup>c</sup>	t <sub>r</sub>	$V_{DD}$ = 50 V, $R_L$ = 1.0 $\Omega$		10	20	ns
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>	$I_D \cong 50$ A, $V_{GEN}$ = 10 V, $R_g$ = 1 $\Omega$		18	35	
Fall Time <sup>c</sup>	t <sub>f</sub>			8	15	
Drain-Source Body Diode Character	istics T <sub>C</sub> = 25	°Cp				
Continuous Current	ا <sub>S</sub>				60	
Pulsed Current	I <sub>SM</sub>				100	A
Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>F</sub> = 15 A, V <sub>GS</sub> = 0 V		0.85	1.5	V
Reverse Recovery Time	t <sub>rr</sub>			80	120	ns
Peak Reverse Recovery Current	I <sub>RM(REC)</sub>	I <sub>F</sub> = 50 A, dl/dt = 100 A/μs		4		А
Reverse Recovery Charge	Q <sub>rr</sub>	1		160	240	nC

Notes:

a. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %.

b. Guaranteed by design, not subject to production testing.

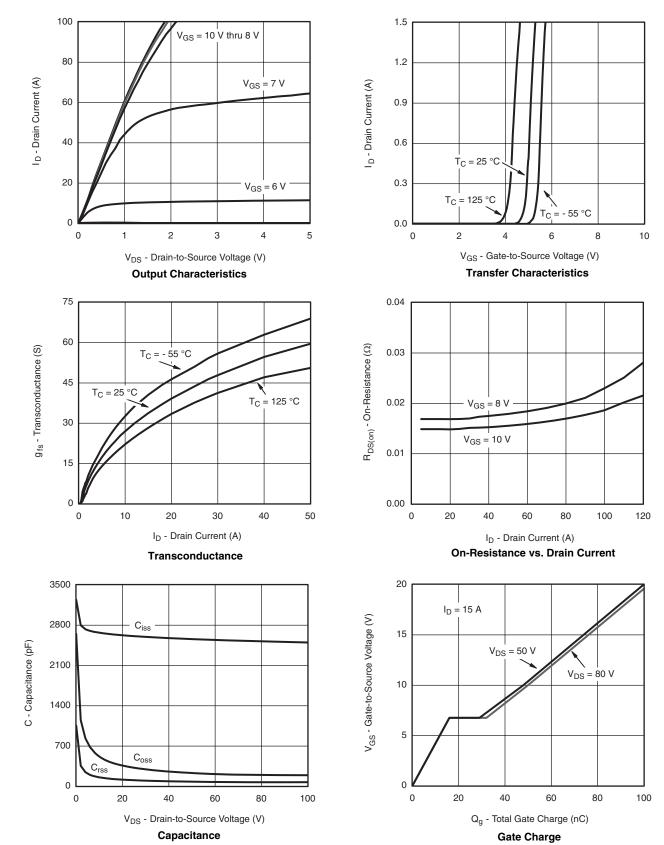
c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



# SUP60N10-18P

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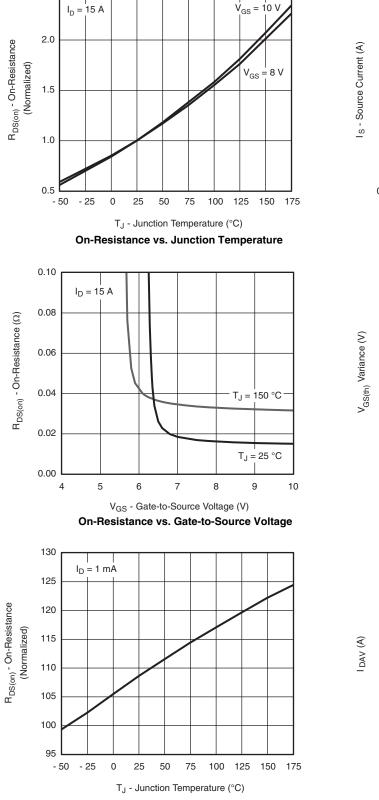


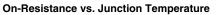
## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

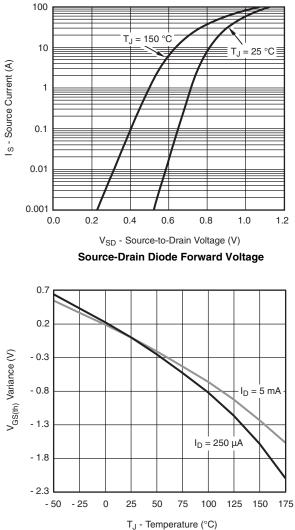
Document Number: 65003 S09-1096-Rev. A, 15-Jun-09

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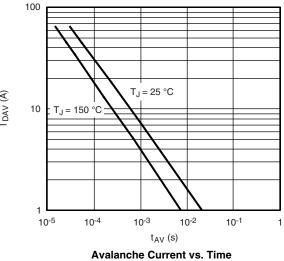






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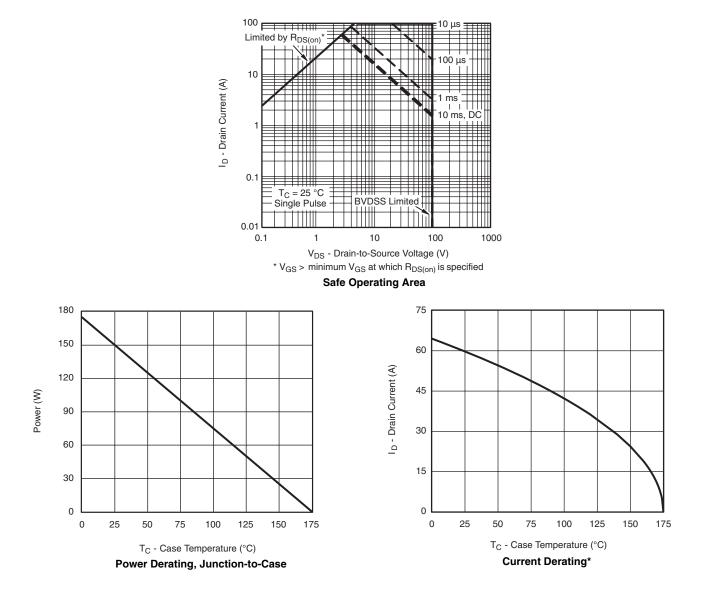
Threshold Voltage



SUP60N10-18P Vishay Siliconix



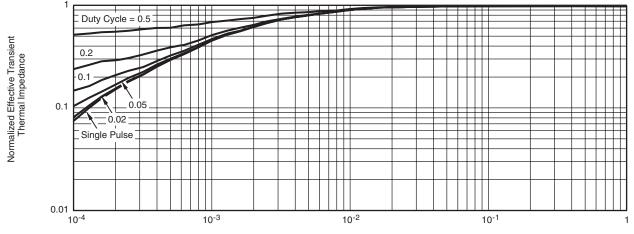
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\* The power dissipation  $P_D$  is based on  $T_{J(max.)} = 175 \text{ °C}$ , using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



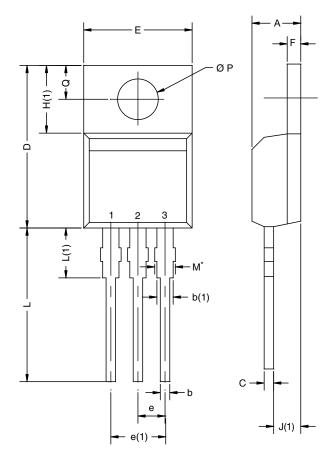
Square Wave Pulse Duration (s)

Normalized Thermal Transient Impedance, Junction-to-Case

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# **TO-220AB**

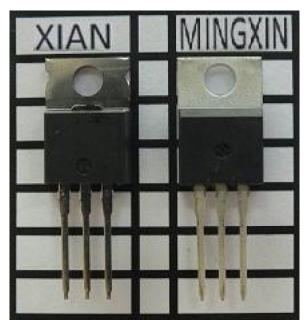


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
А	4.25	4.65	0.167	0.183
b	0.69	1.01	0.027	0.040
b(1)	1.20	1.73	0.047	0.068
С	0.36	0.61	0.014	0.024
D	14.85	15.49	0.585	0.610
E	10.04	10.51	0.395	0.414
е	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.09	6.48	0.240	0.255
J(1)	2.41	2.92	0.095	0.115
L	13.35	14.02	0.526	0.552
L(1)	3.32	3.82	0.131	0.150
ØΡ	3.54	3.94	0.139	0.155
Q	2.60	3.00	0.102	0.118

#### Notes

 $^{\star}$  M = 1.32 mm to 1.62 mm (dimension including protrusion) Heatsink hole for HVM

Xi'an and Mingxin actual photo



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