

Vishay Siliconix

COMPLIANT

N-Channel 55-V (D-S), 175 °C MOSFET

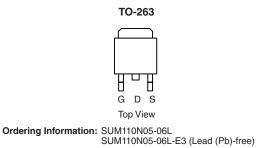
PRODUCT SUMMARY					
V _{(BR)DSS} (V)	r _{DS(on)} (Ω)	I _D (A)	Q _g (Typ)		
55	0.006 at V _{GS} = 10 V	110	65		
55	0.0085 at V_{GS} = 4.5 V	92	05		

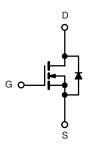
FEATURES

- TrenchFET[®] Power MOSFET
- 175 °C Junction Temperature
- Low Thermal Resistance Package

APPLICATIONS

Industrial





N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_{C} = 25 \text{ °C}$, unless otherwise noted						
Parameter	Symbol	Limit	Unit			
Drain-Source Voltage	V _{DS}	55	Ň			
Gate-Source Voltage	V _{GS}	± 20	V			
Continuous Drain Current ($T_1 = 175 ^{\circ}C$)	T _C = 25 °C	L	110			
Continuous Drain Current (1) = 175 C)	T _C = 125 °C	I _D	63			
Pulsed Drain Current	I _{DM}	240	A			
Avalanche Current	I _{AR}	60				
Repetitive Avalanche Energy ^a	L = 0.1 mH	E _{AR}	180	mJ		
Manimum Davies Dissignation	T _C = 25 °C	Р	158 ^b	w		
Maximum Power Dissipation	T _A = 25 °C ^c	P _D	3.7			
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 175	°C			

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Limit	Unit		
Junction-to-Ambient	PCB Mount ^c	R _{thJA}	40	°C/W		
Junction-to-Case		R _{thJC}	0.95	C/W		

Notes:

a. Duty cycle \leq 1 %.

b. See SOA curve for voltage derating.

c. When Mounted on 1" square PCB (FR-4 material).

* Pb containing terminations are not RoHS compliant, exemptions may apply.

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V _{(BR)DSS}	$V_{DS} = 0 V, I_{D} = 250 \mu A$	55			v	
Gate-Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \ \mu A$	1		3	v	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 100	nA	
		$V_{DS} = 55 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$			1		
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 55 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 125 ^{\circ}\text{C}$			50	μA	
		$V_{DS} = 55 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 175 ^{\circ}\text{C}$			250	-	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, \text{ V}_{GS} = 10 \text{ V}$	120			А	
		V _{GS} = 10 V, I _D = 30 A		0.0047	0.006	1	
		$V_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 20 \text{ A}$		0.0066	0.0085	-	
Drain-Source On-State Resistance ^a	r _{DS(on)}	V_{GS} = 10 V, I _D = 30 A, T _J = 125 °C			0.0102	Ω	
		$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 30 \text{ A}, \text{ T}_{J} = 175 ^{\circ}\text{C}$			0.0132		
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 30 A	30			S	
Dynamic ^b	•			•	ι ι		
Input Capacitance	C _{iss}			3300		pF	
Output Capacitance	C _{oss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		625			
Reverse Transfer Capacitance	C _{rss}			310			
Total Gate Charge ^c	Qg			65	100		
Gate-Source Charge ^c	Q _{gs}	$V_{DS} = 30$ V, $V_{GS} = 10$ V, $I_{D} = 110$ A		15		nC	
Gate-Drain Charge ^c	Q _{gd}			16			
Turn-On Delay Time ^c	t _{d(on)}			15	25		
Rise Time ^c	t _r	V_{DD} = 30 V, R_L = 0.27 Ω		15	25	ns	
Turn-Off Delay Time ^c	t _{d(off)}	$\text{I}_\text{D} \cong$ 110 A, V_GEN = 10 V, R_g = 2.5 Ω		35	55		
Fall Time ^c	t _f			15	25		
Source-Drain Diode Ratings and Cha	aracteristics 7	_C = 25 °C ^b			<u> </u>		
Continuous Current	ا _S	-			110		
Pulsed Current	I _{SM}				240	A	
Forward Voltage ^a	V _{SD}	I _F = 110 A, V _{GS} = 0 V		1.0	1.5	V	
Reverse Recovery Time	t _{rr}			70	125	ns	
Peak Reverse Recovery Charge	I _{RM(REC)}	I _F = 110 A, di/dt = 100 A/μs		2.5	5	А	
Reverse Recovery Charge	Q _{rr}			0.09	0.31	μC	

Notes:

a. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2 %.

b. Guaranteed by design, not subject to production testing.

c. Independent of operating temperature.

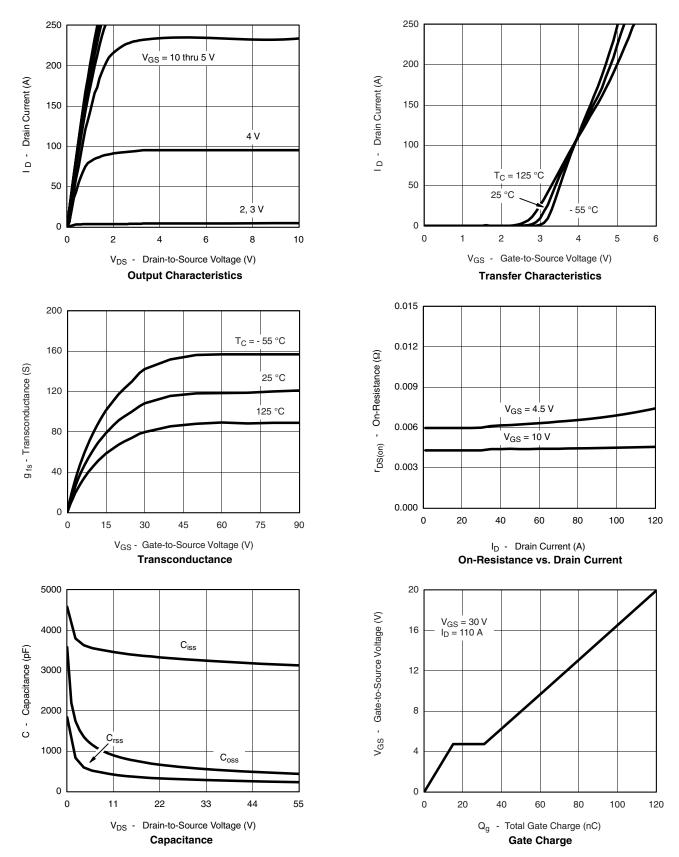
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

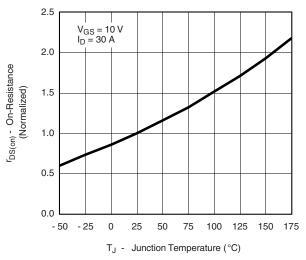


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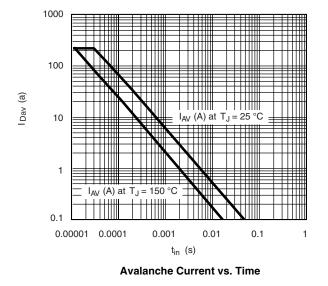


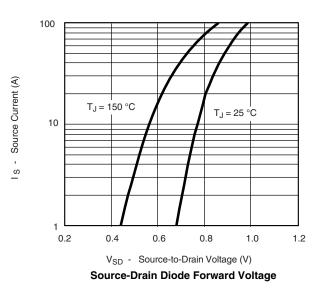
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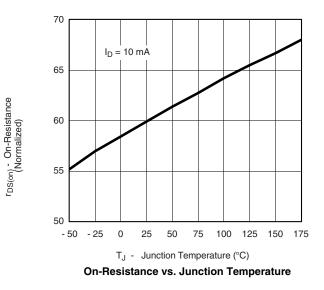
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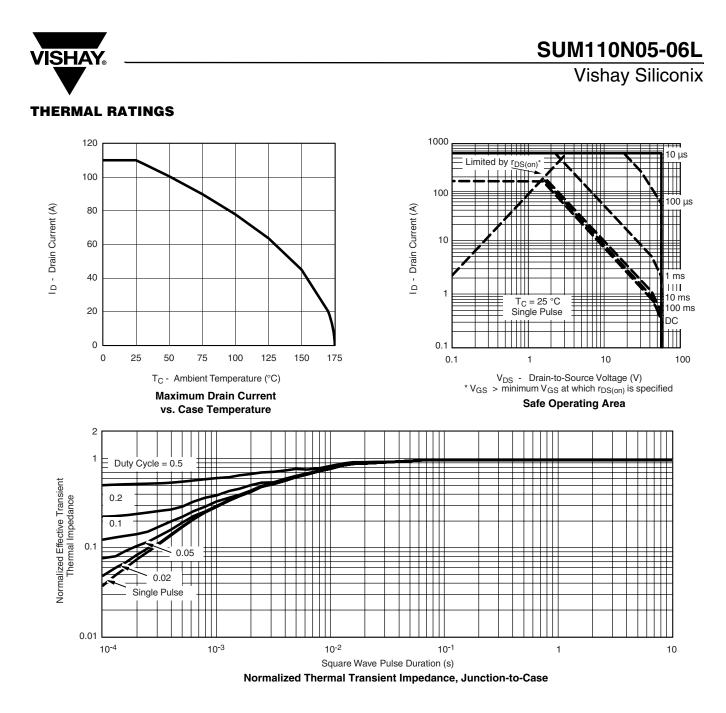


On-Resistance vs. Junction Temperature









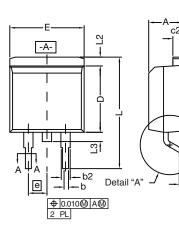
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?72005.

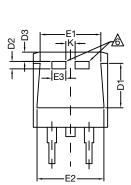


Package Information

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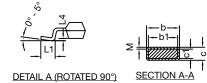
TO-263 (D²PAK): 3-LEAD





-B-

С



		INCHES		MILLIMETERS		
DIM.		MIN.	MAX.	MIN.	MAX.	
	А	0.160	0.190	4.064	4.826	
	b	0.020	0.039	0.508	0.990	
	b1	0.020	0.035	0.508	0.889	
	b2	0.045	0.055	1.143	1.397	
с*	Thin lead	0.013	0.018	0.330	0.457	
C	Thick lead	0.023	0.028		0.711	
c1	Thin lead	0.013	0.017	0.330	0.431	
CI	Thick lead	0.023	0.027	0.584	0.685	
	c2	0.045	0.055	1.143	1.397	
	D	0.340	0.380	8.636	9.652	
	D1	0.220	0.240	5.588	6.096	
	D2	0.038	0.042	0.965	1.067	
	D3	0.045	0.055	1.143	1.397	
	E	0.380	0.410	9.652	10.414	
	E1	0.245	-	6.223	-	
	E2	0.355	0.375	9.017	9.525	
	E3	0.072	0.078	1.829 1.981		
	е	0.100 BSC		2.54	BSC	
	К	0.045	0.055	1.143	1.397	
	L	0.575	0.625	14.605	15.875	
	L1	0.090	0.110	2.286	2.794	
	L2	0.040	0.055	1.016	1.397	
	L3	0.050	0.070	1.270	1.778	
	L4	0.010 BSC		0.254 BSC		
М		-	0.002	-	0.050	
ECN: T10-0738-Rev. J, 03-Jan-11 DWG: 5843						

Notes

- 1. Plane B includes maximum features of heat sink tab and plastic.
- 2. No more than 25 % of L1 can fall above seating plane by max. 8 mils.
- 3. Pin-to-pin coplanarity max. 4 mils.
- 4. *: Thin lead is for SUB, SYB.
- Thick lead is for SUM, SYM, SQM.
- 5. Use inches as the primary measurement.



RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads Dimensions in Inches/(mm)

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