

# FDMS86520L

## N-Channel PowerTrench® MOSFET

60 V, 22 A, 8.2 mΩ

### Features

- Max  $r_{DS(on)}$  = 8.2 mΩ at  $V_{GS} = 10$  V,  $I_D = 13.5$  A
- Max  $r_{DS(on)}$  = 11.7 mΩ at  $V_{GS} = 4.5$  V,  $I_D = 11.5$  A
- Advanced package and silicon combination for low  $r_{DS(on)}$  and high efficiency
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

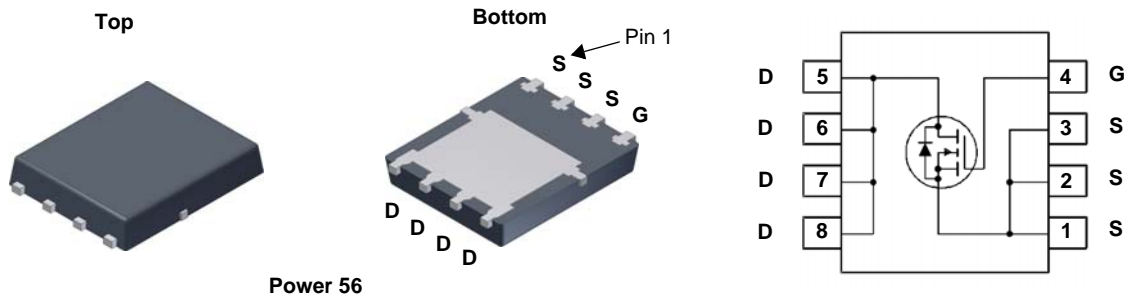


### General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency and to minimize switch node ringing of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low  $r_{DS(on)}$ , fast switching speed and body diode reverse recovery performance.

### Applications

- Primary Switch in isolated DC-DC
- Synchronous Rectifier
- Load Switch



Power 56

### MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Conditions	Rated Value	Units
$V_{DS}$	Drain to Source Voltage		60	V
$V_{GS}$	Gate to Source Voltage		$\pm 20$	V
$I_D$	Drain Current -Continuous (Package limited)	$T_C = 25^\circ\text{C}$	22	A
	-Continuous (Silicon limited)	$T_C = 25^\circ\text{C}$	71	
	-Continuous	$T_A = 25^\circ\text{C}$ (Note 1a)	13.5	
	-Pulsed		60	
$E_{AS}$	Single Pulse Avalanche Energy	(Note 3)	91	mJ
$P_D$	Power Dissipation	$T_C = 25^\circ\text{C}$	69	W
	Power Dissipation	$T_A = 25^\circ\text{C}$ (Note 1a)	2.5	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range		-55 to +150	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case		1.8	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	50	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS86520L	FDMS86520L	Power 56	13"	12 mm	3000 units

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}, V_{GS} = 0\text{ V}$	60			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		29		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 48\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	1	1.8	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-7		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 13.5\text{ A}$		6.7	8.2	m $\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 11.5\text{ A}$		9.1	11.7	
		$V_{GS} = 10\text{ V}, I_D = 13.5\text{ A}, T_J = 125\text{ }^\circ\text{C}$		9.6	11.8	
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 13.5\text{ A}$		51		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		3470	4615	pF
$C_{oss}$	Output Capacitance			625	835	pF
$C_{rss}$	Reverse Transfer Capacitance			25	45	pF
$R_g$	Gate Resistance			0.6		$\Omega$

### Switching Characteristics

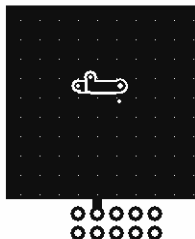
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 30\text{ V}, I_D = 13.5\text{ A}, V_{GS} = 10\text{ V}, R_{GEN} = 6\text{ }\Omega$		15	27	ns
$t_r$	Rise Time			5.6	11	ns
$t_{d(off)}$	Turn-Off Delay Time			32	52	ns
$t_f$	Fall Time			3.4	10	ns
$Q_g$	Total Gate Charge	$V_{GS} = 0\text{ V to } 10\text{ V}$		45	63	nC
$Q_g$	Total Gate Charge	$V_{GS} = 0\text{ V to } 4.5\text{ V}$	$V_{DD} = 30\text{ V}, I_D = 13.5\text{ A}$	21	30	nC
$Q_{gs}$	Gate to Source Charge			9.5		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			4.7		nC

### Drain-Source Diode Characteristics

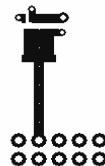
$V_{SD}$	Source-Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 2.1\text{ A}$ (Note 2)		0.72	1.2	V
		$V_{GS} = 0\text{ V}, I_S = 13.5\text{ A}$ (Note 2)		0.83	1.3	
$t_{rr}$	Reverse Recovery Time	$I_F = 13.5\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		37	60	ns
$Q_{rr}$	Reverse Recovery Charge			21	34	nC
$t_{rr}$	Reverse Recovery Time	$I_F = 13.5\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$		30	48	ns
$Q_{rr}$	Reverse Recovery Charge			37	59	nC

**Notes:**

1.  $R_{\theta JA}$  is determined with the device mounted on a  $1\text{ in}^2$  pad 2 oz copper pad on a  $1.5 \times 1.5\text{ in.}$  board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a.  $50\text{ }^\circ\text{C/W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper.



b.  $125\text{ }^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width <  $300\text{ }\mu\text{s}$ , Duty cycle < 2.0%.

3. Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 1\text{ mH}$ ,  $I_{AS} = 13.5\text{ A}$ ,  $V_{DD} = 54\text{ V}$ ,  $V_{GS} = 10\text{ V}$ .

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

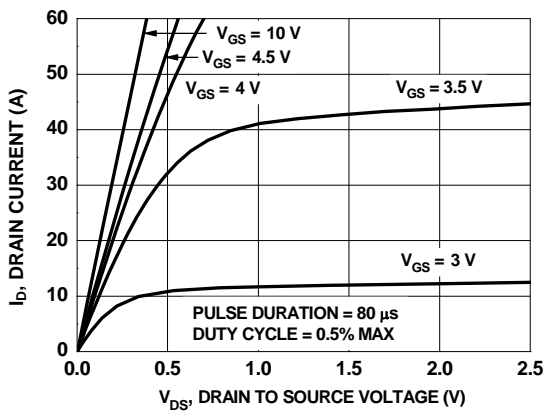


Figure 1. On Region Characteristics

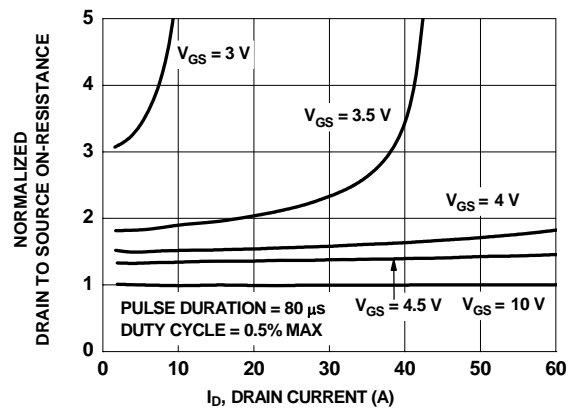


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

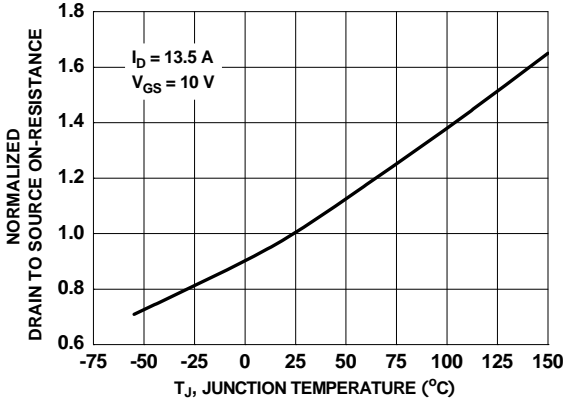


Figure 3. Normalized On Resistance vs Junction Temperature

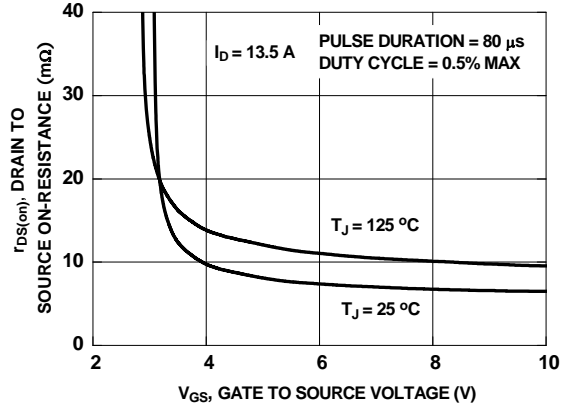


Figure 4. On-Resistance vs Gate to Source Voltage

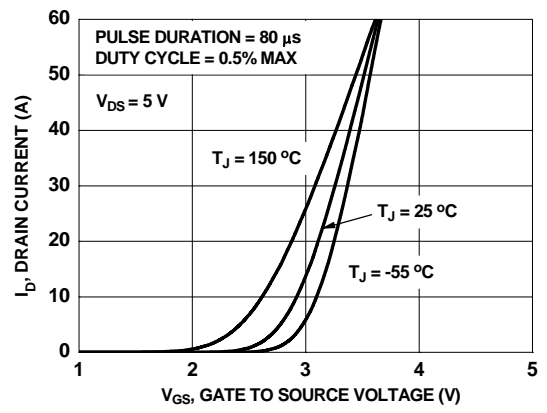


Figure 5. Transfer Characteristics

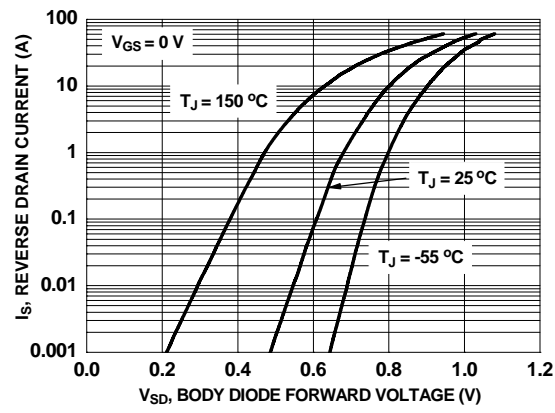
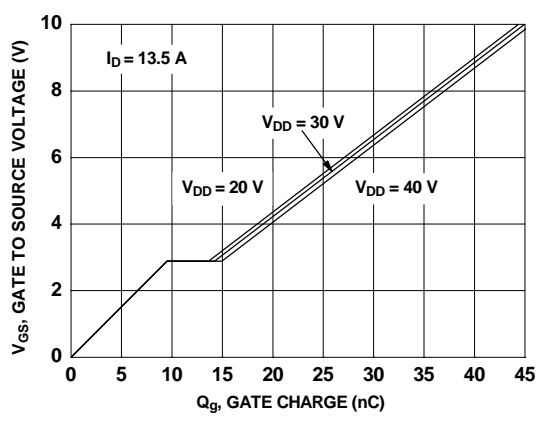
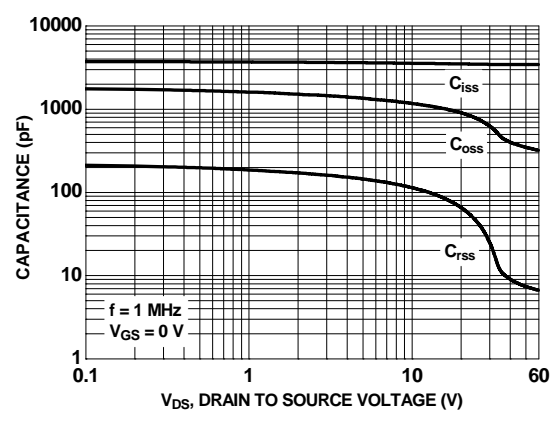


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

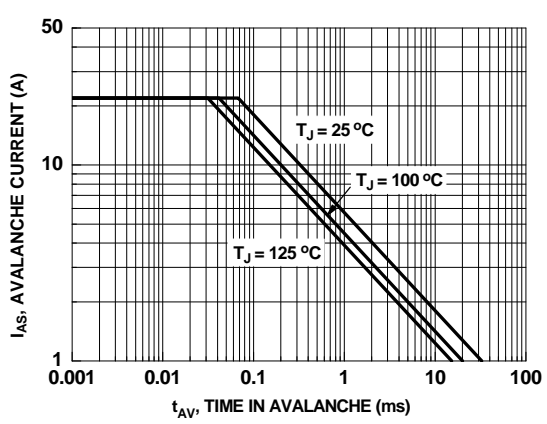
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



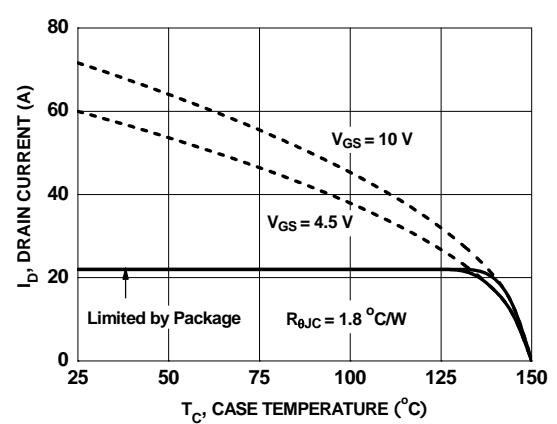
**Figure 7. Gate Charge Characteristics**



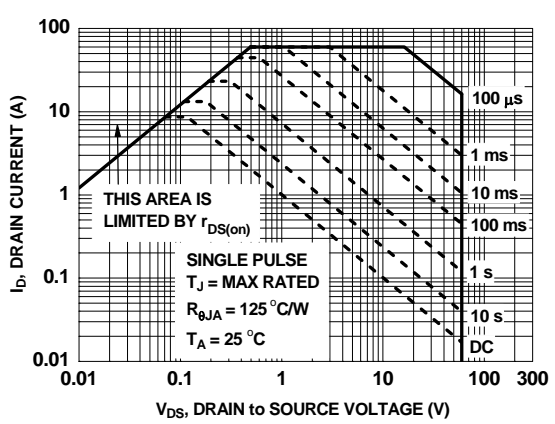
**Figure 8. Capacitance vs Drain to Source Voltage**



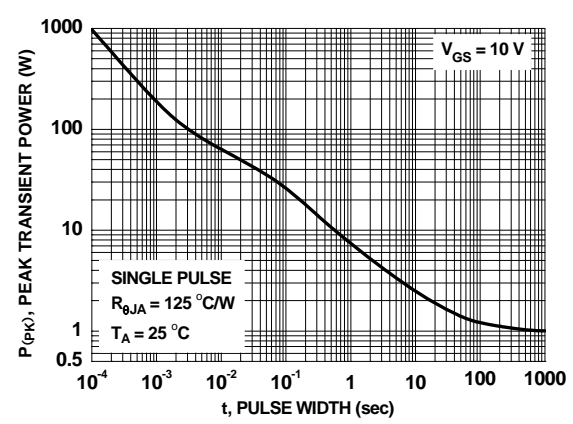
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

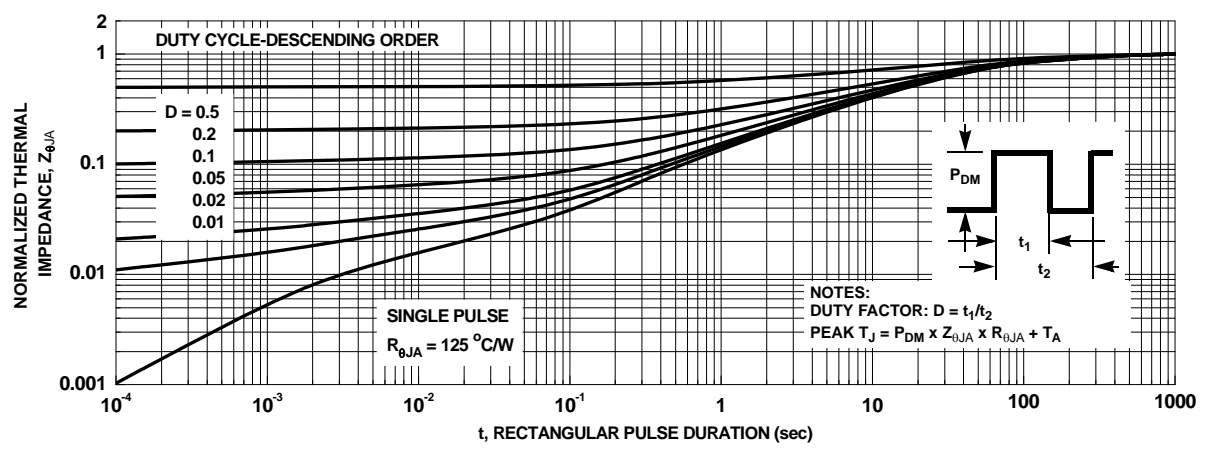


**Figure 11. Forward Bias Safe Operating Area**



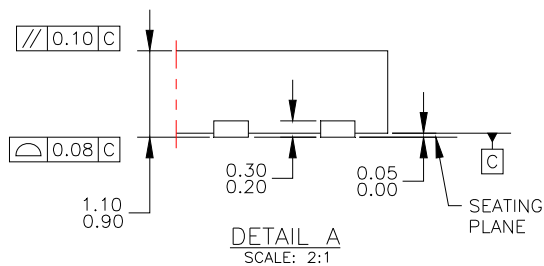
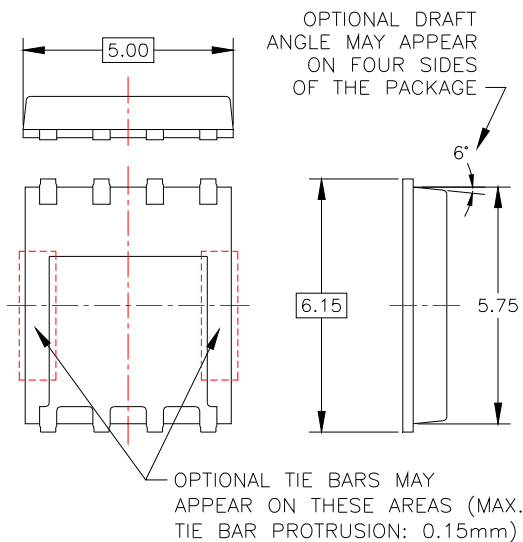
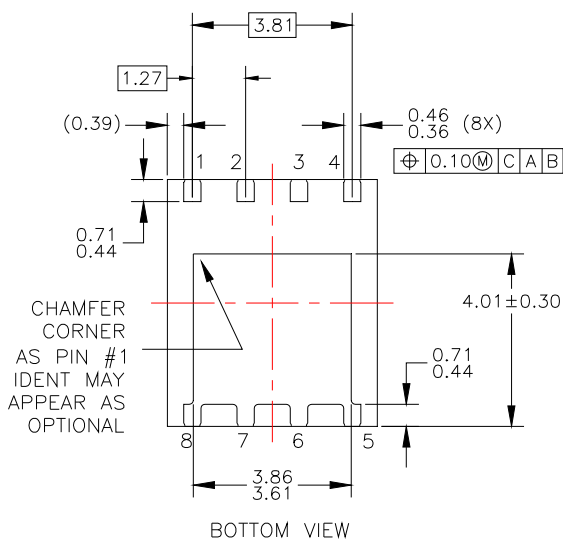
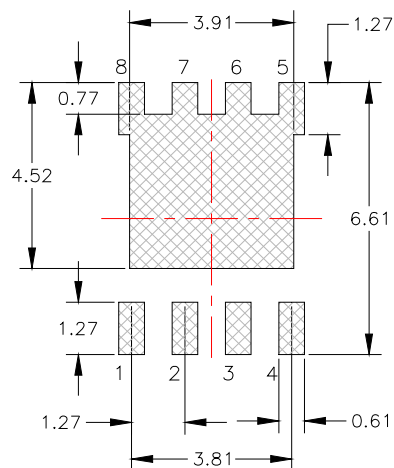
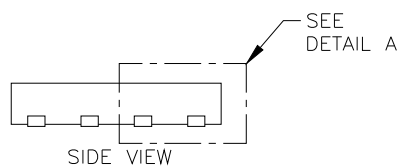
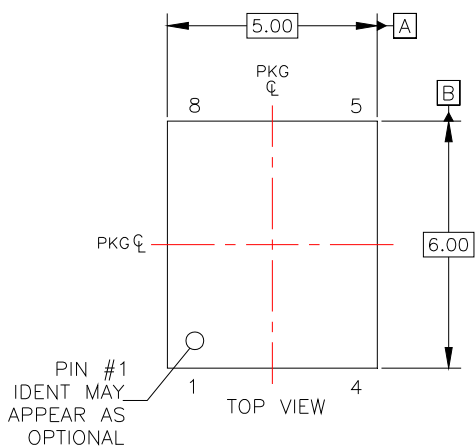
**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



**Figure 13. Junction-to-Ambient Transient Thermal Response Curve**

## Dimensional Outline and Pad Layout



NOTES: UNLESS OTHERWISE SPECIFIED

- A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA, DATED OCTOBER 2002.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- E) DRAWING FILE NAME: PQFN08AREV4



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**Definition of Terms**

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