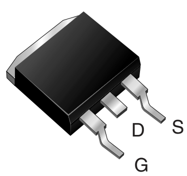
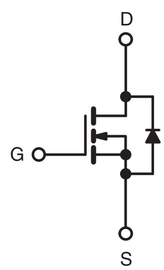
# Power MOSFET

| PRODUCT SUMMARY | | |
|---|---|---|
| $V_{DS}$ (V) | 200 | |
| $R_{DS(on)}$ (Ω) | $V_{GS}$ = 5 V | 0.18 |
| $Q_g$ (Max.) (nC) | 66 | |
| $Q_{gs}$ (nC) | 9.0 | |
| $Q_{gd}$ (nC) | 38 | |
| Configuration | Single | |

**SMD-220**




N-Channel MOSFET

## FEATURES

- **Halogen-free According to IEC 61249-2-21 Definition**
- Surface Mount
- Available in Tape and Reel
- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Logic-Level Gate Drive
- $R_{DS(on)}$ Specified at $V_{GS}$ = 4 V and 5 V
- Fast Switching
- Compliant to RoHS Directive 2002/95/EC

RoHS*
COMPLIANT
HALOGEN
FREE
Available

## DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SMD-220 is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The SMD-220 is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application.

| ORDERING INFORMATION | | | |
|---|---|---|---|
| Package | SMD-220 | SMD-220 | SMD-220 |
| Lead (Pb)-free and Halogen-free | SiHL640S-GE3 | SiHL640STRL-GE3[a] | SiHL640STRR-GE3[a] |
| Lead (Pb)-free | IRL640SPbF | IRL640STRLPbF[a] | IRL640STRRPbF[a] |
| | SiHL640S-E3 | SiHL640STL-E3[a] | SiHL640STR-E3[a] |

**Note**
a. See device orientation.

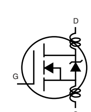
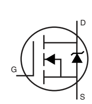
| ABSOLUTE MAXIMUM RATINGS ($T_C$ = 25 °C, unless otherwise noted) | | | | | |
|---|---|---|---|---|---|
| **PARAMETER** | | | **SYMBOL** | **LIMIT** | **UNIT** |
| Drain-Source Voltage | | | $V_{DS}$ | 200 | V |
| Gate-Source Voltage | | | $V_{GS}$ | ± 10 | |
| Continuous Drain Current | $V_{GS}$ at 5.0 V | $T_C$ = 25 °C | $I_D$ | 17 | A |
| | | $T_C$ = 100 °C | | 11 | |
| Pulsed Drain Current[a] | | | $I_{DM}$ | 68 | |
| Linear Derating Factor | | | | 1.0 | W/°C |
| Linear Derating Factor (PCB Mount)[e] | | | | 0.025 | |
| Single Pulse Avalanche Energy[b] | | | $E_{AS}$ | 580 | mJ |
| Repetitive Avalanche Current[a] | | | $I_{AR}$ | 10 | A |
| Repetitive Avalanche Energy[a] | | | $E_{AR}$ | 13 | mJ |
| Maximum Power Dissipation | $T_C$ = 25 °C | | $P_D$ | 125 | W |
| Maximum Power Dissipation (PCB Mount)[e] | $T_A$ = 25 °C | | | 3.1 | |
| Peak Diode Recovery dV/dt[c] | | | dV/dt | 5.0 | V/ns |
| Operating Junction and Storage Temperature Range | | | $T_J$, $T_{stg}$ | - 55 to + 150 | °C |
| Soldering Temperature | for 10 s | | | 300[d] | |

**Notes**
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. $V_{DD}$ = 50 V, starting $T_J$ = 25 °C, L = 3.0 mH, $R_g$ = 25 Ω, $I_{AS}$ = 17 A (see fig. 12).
c. $I_{SD} \leq$ 17 A, dI/dt ≤ 150 A/μs, $V_{DD} \leq V_{DS}$, $T_J \leq$ 150 °C.
d. 1.6 mm from case.
e. When mounted on 1" square PCB (FR-4 or G-10 Material).

* Pb containing terminations are not RoHS compliant, exemptions may apply

| THERMAL RESISTANCE RATINGS | | | | | |
|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **MIN.** | **TYP.** | **MAX.** | **UNIT** |
| Maximum Junction-to-Ambient | $R_{thJA}$ | - | - | 62 | °C/W |
| Maximum Junction-to-Ambient (PCB Mount)[a] | $R_{thJA}$ | - | - | 40 | |
| Maximum Junction-to-Case (Drain) | $R_{thJC}$ | - | - | 1.0 | |

**Note**
a. When mounted on 1" square PCB (FR-4 or G-10 material).

| **SPECIFICATIONS** ($T_J$ = 25 °C, unless otherwise noted) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TEST CONDITIONS** | | **MIN.** | **TYP.** | **MAX.** | **UNIT** |
| **Static** | | | | | | | |
| Drain-Source Breakdown Voltage | $V_{DS}$ | $V_{GS}$ = 0, $I_D$ = 250 μA | | 200 | - | - | V |
| $V_{DS}$ Temperature Coefficient | $\Delta V_{DS}/T_J$ | Reference to 25 °C, $I_D$ = 1 mA | | - | 0.27 | - | V/°C |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 μA | | 1.0 | - | 2.0 | V |
| Gate-Source Leakage | $I_{GSS}$ | $V_{GS}$ = ± 10 V | | - | - | ± 100 | nA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 200 V, $V_{GS}$ = 0 V | | - | - | 25 | μA |
| | | $V_{DS}$ = 160 V, $V_{GS}$ = 0 V, $T_J$ = 125 °C | | - | - | 250 | |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS}$ = 5.0 V | $I_D$ = 10 A[b] | - | - | 0.18 | Ω |
| | | $V_{GS}$ = 4.0 V | $I_D$ = 8.5 A[b] | - | - | 0.27 | |
| Forward Transconductance | $g_{fs}$ | $V_{DS}$ = 50 V, $I_D$ = 10 A[b] | | 16 | - | - | S |
| **Dynamic** | | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{GS}$ = 0 V, $V_{DS}$ = 25 V, f = 1.0 MHz, see fig. 5 | | - | 1800 | - | pF |
| Output Capacitance | $C_{oss}$ | | | - | 400 | - | |
| Reverse Transfer Capacitance | $C_{rss}$ | | | - | 120 | - | |
| Total Gate Charge | $Q_g$ | $V_{GS}$ = 5.0 V | $I_D$ = 17 A, $V_{DS}$ = 160 V, see fig. 6 and 13[b] | - | - | 66 | nC |
| Gate-Source Charge | $Q_{gs}$ | | | - | - | 9.0 | |
| Gate-Drain Charge | $Q_{gd}$ | | | - | - | 38 | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = 100 V, $I_D$ = 17 A, $R_g$ = 4.6 Ω, $R_D$ = 5.7 Ω, see fig. 10[b] | | - | 8.0 | - | ns |
| Rise Time | $t_r$ | | | - | 83 | - | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | - | 44 | - | |
| Fall Time | $t_f$ | | | - | 52 | - | |
| Internal Drain Inductance | $L_D$ | Between lead, 6 mm (0.25") from package and center of die contact |  | - | 4.5 | - | nH |
| Internal Source Inductance | $L_S$ | | | - | 7.5 | - | |
| **Drain-Source Body Diode Characteristics** | | | | | | | |
| Continuous Source-Drain Diode Current | $I_S$ | MOSFET symbol showing the integral reverse p - n junction diode |  | - | - | 17 | A |
| Pulsed Diode Forward Current[a] | $I_{SM}$ | | | - | - | 68 | |
| Body Diode Voltage | $V_{SD}$ | $T_J$ = 25 °C, $I_S$ = 17 A, $V_{GS}$ = 0 V[b] | | - | - | 2.0 | V |
| Body Diode Reverse Recovery Time | $t_{rr}$ | $T_J$ = 25 °C, $I_F$ = 17 A, dI/dt = 100 A/μs[b] | | - | 310 | 470 | ns |
| Body Diode Reverse Recovery Charge | $Q_{rr}$ | | | - | 3.2 | 4.8 | μC |
| Forward Turn-On Time | $t_{on}$ | Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$) | | | | | |

**Notes**
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

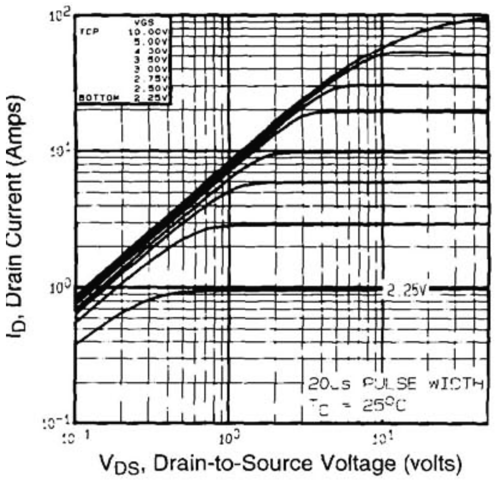



**Fig. 1 - Typical Output Characteristics, $T_C$ = 25 °C**

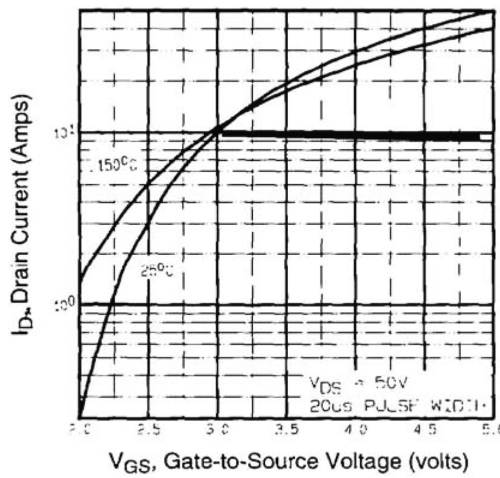



**Fig. 3 - Typical Transfer Characteristics**

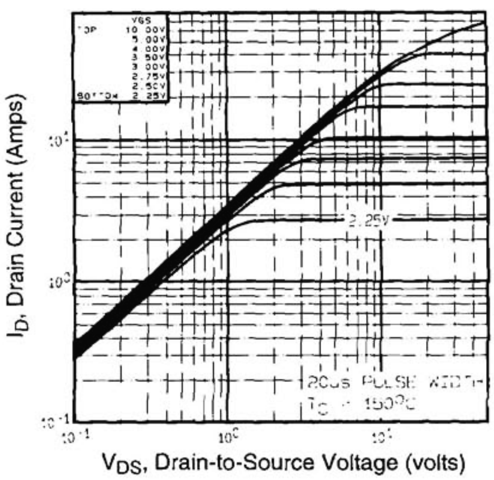



**Fig. 2 - Typical Output Characteristics, $T_C$ = 150 °C**

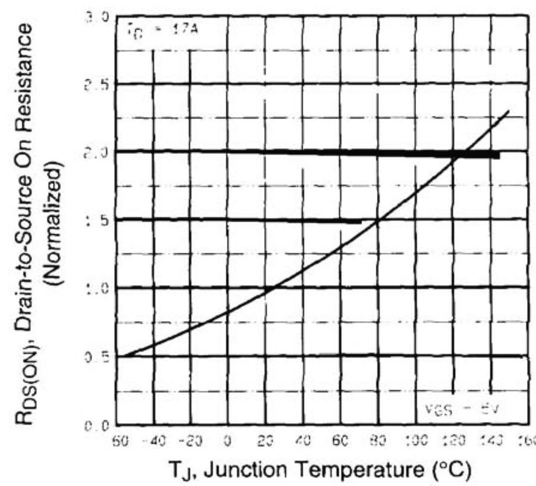



**Fig. 4 - Normalized On-Resistance vs. Temperature**

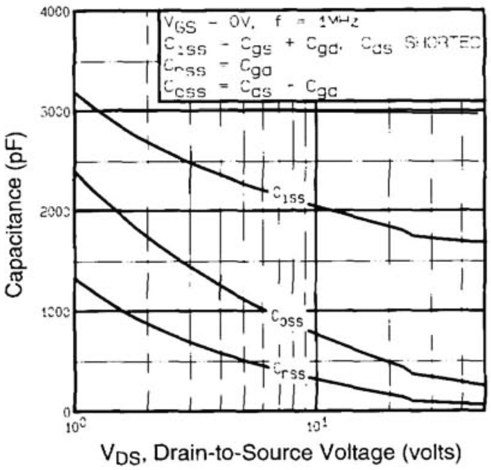



**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**

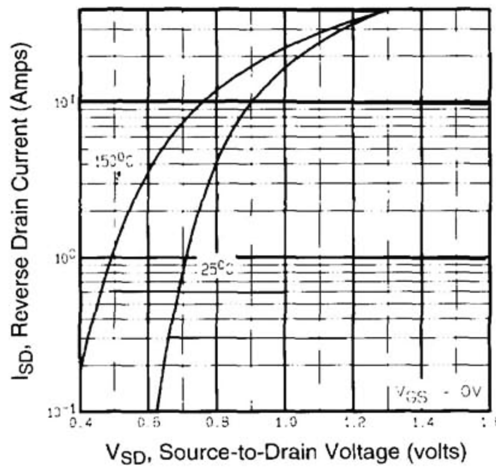



**Fig. 7 - Typical Source-Drain Diode Forward Voltage**

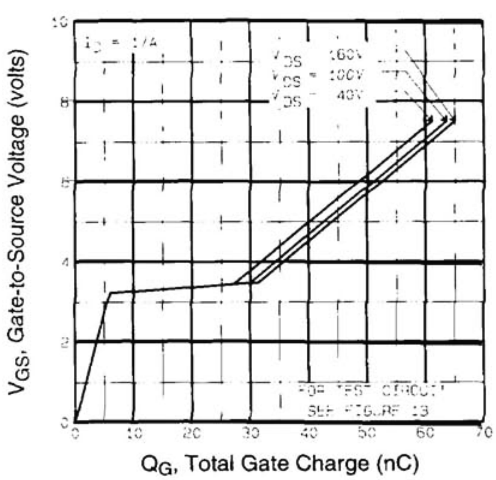



**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**

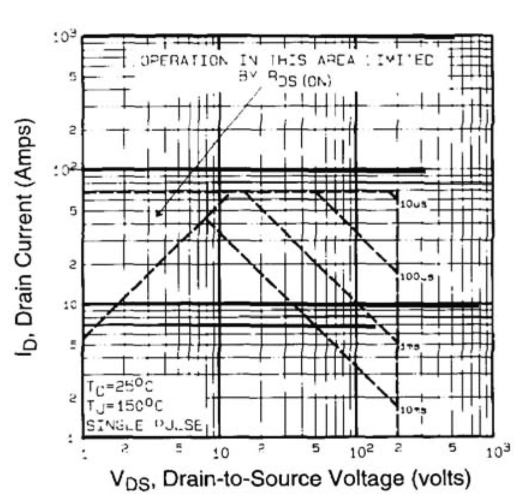



**Fig. 8 - Maximum Safe Operating Area**

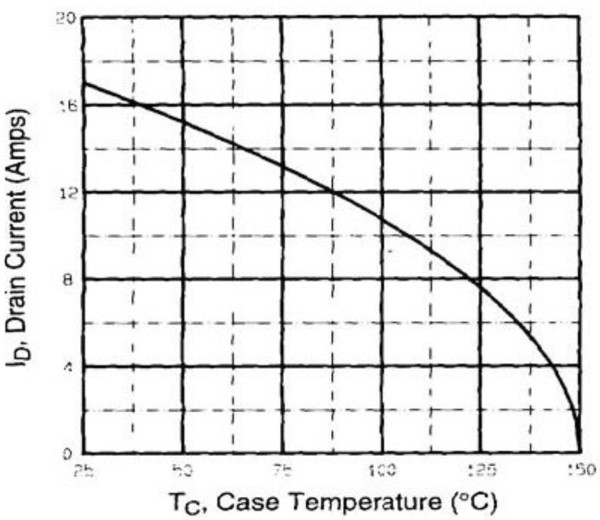



Fig. 9 - Maximum Drain Current vs. Case Temperature

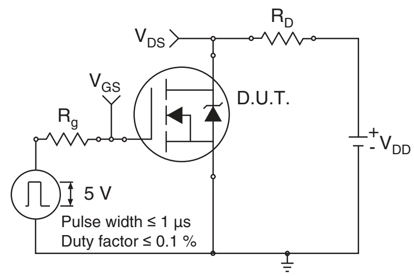



Fig. 10a - Switching Time Test Circuit

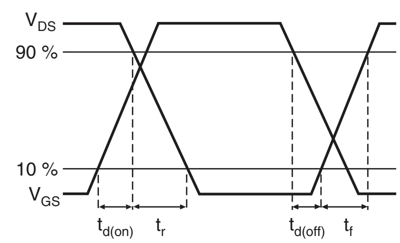



Fig. 10b - Switching Time Waveforms

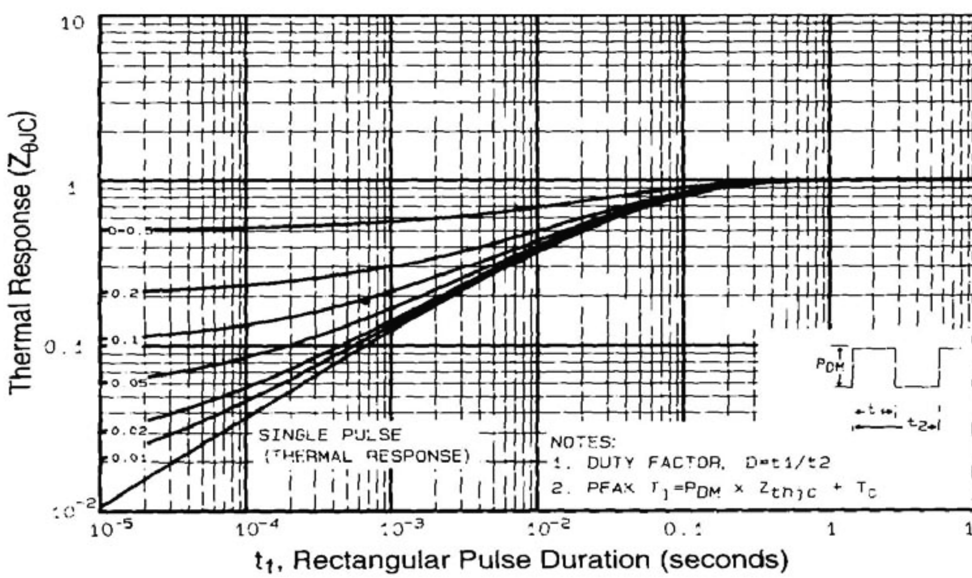



Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

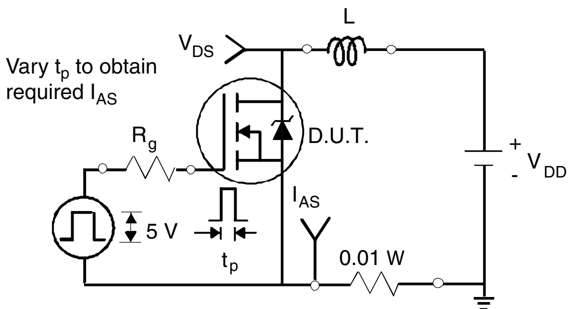



Fig. 12a - Unclamped Inductive Test Circuit

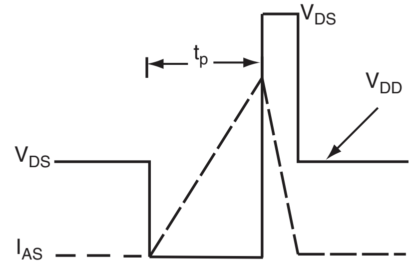



Fig. 12b - Unclamped Inductive Waveforms

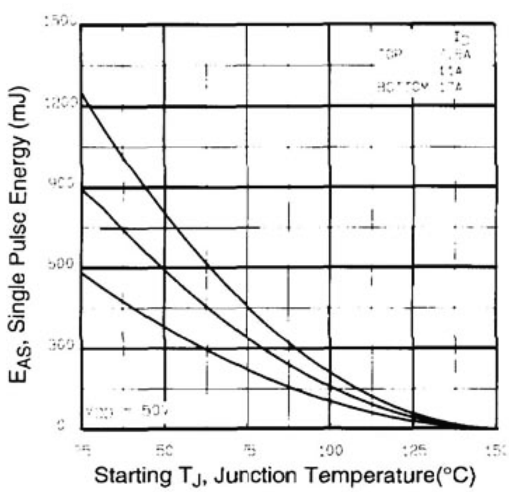



Fig. 12c - Maximum Avalanche Energy vs. Drain Current

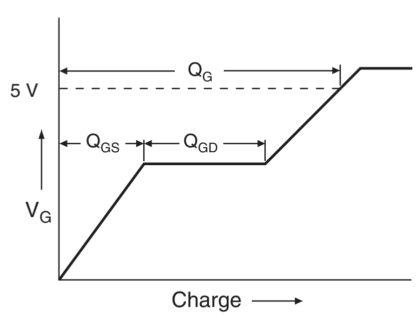



Fig. 13a - Basic Gate Charge Waveform

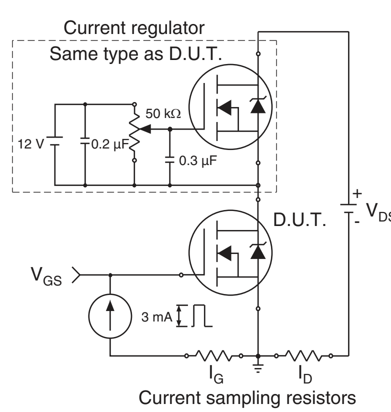
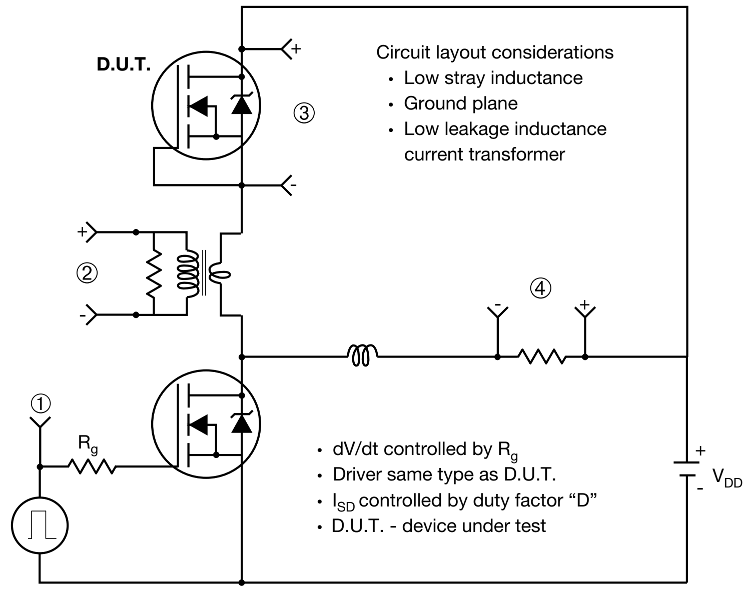
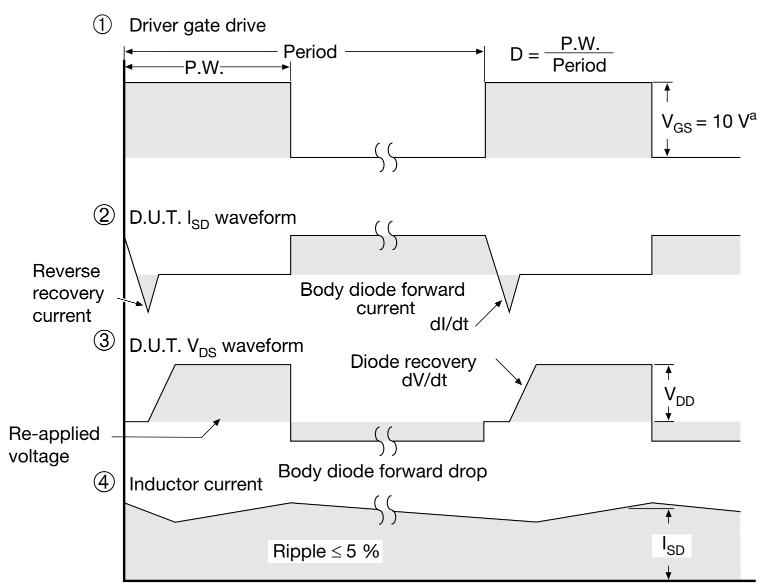



Fig. 13b - Gate Charge Test Circuit

**Peak Diode Recovery dV/dt Test Circuit**



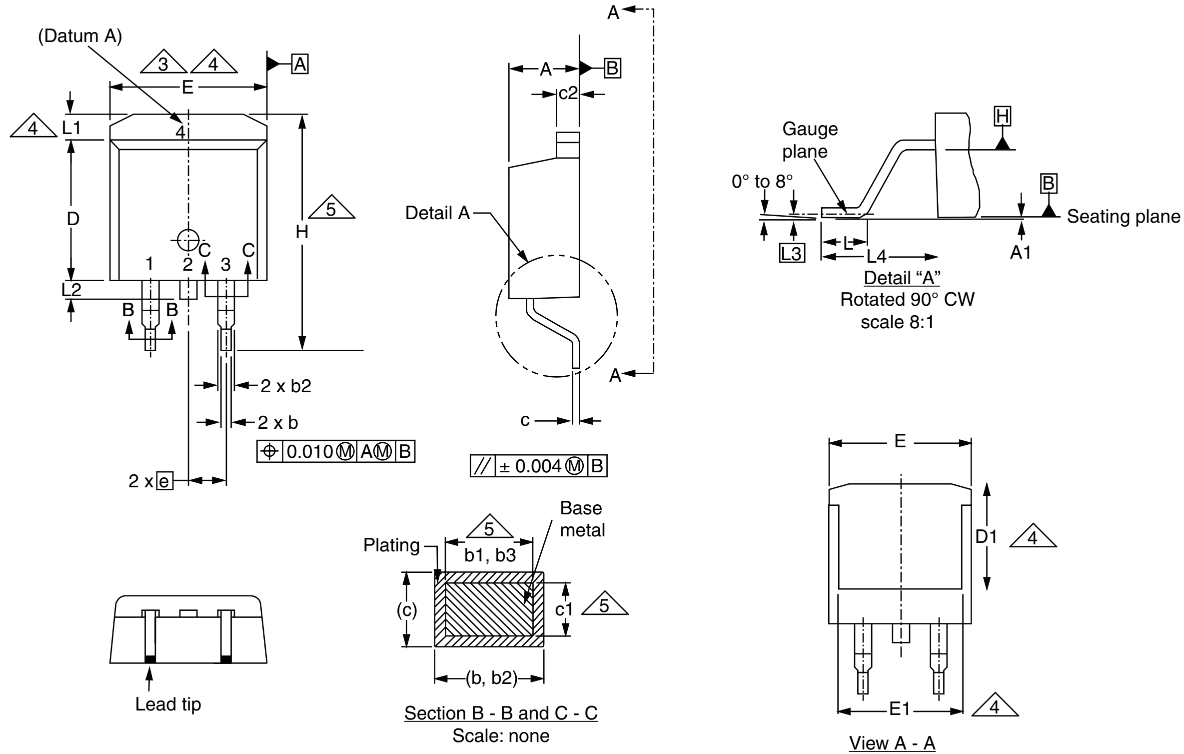

**Note**

a. $V_{GS}$ = 5 V for logic level devices

**Fig. 14 - For N-Channel**

*Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91306.*

## TO-263AB (HIGH VOLTAGE)




| DIM. | MILLIMETERS MIN. | MILLIMETERS MAX. | INCHES MIN. | INCHES MAX. |
|---|---|---|---|---|
| A | 4.06 | 4.83 | 0.160 | 0.190 |
| A1 | 0.00 | 0.25 | 0.000 | 0.010 |
| b | 0.51 | 0.99 | 0.020 | 0.039 |
| b1 | 0.51 | 0.89 | 0.020 | 0.035 |
| b2 | 1.14 | 1.78 | 0.045 | 0.070 |
| b3 | 1.14 | 1.73 | 0.045 | 0.068 |
| c | 0.38 | 0.74 | 0.015 | 0.029 |
| c1 | 0.38 | 0.58 | 0.015 | 0.023 |
| c2 | 1.14 | 1.65 | 0.045 | 0.065 |
| D | 8.38 | 9.65 | 0.330 | 0.380 |

| DIM. | MILLIMETERS MIN. | MILLIMETERS MAX. | INCHES MIN. | INCHES MAX. |
|---|---|---|---|---|
| D1 | 6.86 | - | 0.270 | - |
| E | 9.65 | 10.67 | 0.380 | 0.420 |
| E1 | 6.22 | - | 0.245 | - |
| e | 2.54 BSC | | 0.100 BSC | |
| H | 14.61 | 15.88 | 0.575 | 0.625 |
| L | 1.78 | 2.79 | 0.070 | 0.110 |
| L1 | - | 1.65 | - | 0.066 |
| L2 | - | 1.78 | - | 0.070 |
| L3 | 0.25 BSC | | 0.010 BSC | |
| L4 | 4.78 | 5.28 | 0.188 | 0.208 |

ECN: S-82110-Rev. A, 15-Sep-08
DWG: 5970

**Notes**

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

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**Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.**