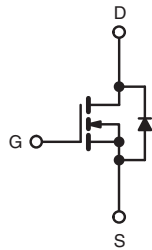
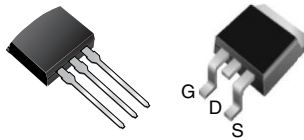




## Power MOSFET

PRODUCT SUMMARY	
$V_{DS}$ (V)	600
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$ 2.2
$Q_g$ (Max.) (nC)	23
$Q_{gs}$ (nC)	5.4
$Q_{gd}$ (nC)	11
Configuration	Single

I<sup>2</sup>PAK (TO-262) D<sup>2</sup>PAK (TO-263)



N-Channel MOSFET

### FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Low Gate Charge  $Q_g$  Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic  $dV/dt$  Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Effective  $C_{OSS}$  Specified
- Compliant to RoHS Directive 2002/95/EC



RoHS\* COMPLIANT HALOGEN FREE Available

### APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching

### TYPICAL SMPS TOPOLOGIES

- Single Transistor Flyback

ORDERING INFORMATION				
Package	D <sup>2</sup> PAK (TO-263)	D <sup>2</sup> PAK (TO-263)	D <sup>2</sup> PAK (TO-263)	I <sup>2</sup> PAK (TO-262)
Lead (Pb)-free and Halogen-free	SiHFBC30AS-GE3	SiHFBC30ASTRL-GE3 <sup>a</sup>	SiHFBC30ASTRR-GE3 <sup>a</sup>	SiHFBC30AL-GE3
Lead (Pb)-free	IRFBC30ASPbF	IRFBC30ASTRLPbF <sup>a</sup>	IRFBC30ASTRRPbF <sup>a</sup>	IRFBC30ALPbF
	SiHFBC30AS-E3	SiHFBC30ASTL-E3 <sup>a</sup>	SiHFBC30ASTR-E3 <sup>a</sup>	SiHFBC30AL-E3

#### Note

- a. See device orientation.

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	$V_{DS}$	600	V	
Gate-Source Voltage	$V_{GS}$	$\pm 30$		
Continuous Drain Current	$V_{GS}$ at 10 V	$T_C = 25\text{ }^\circ\text{C}$	A	
		$T_C = 100\text{ }^\circ\text{C}$		
Pulsed Drain Current <sup>a, e</sup>	$I_{DM}$	14		
Linear Derating Factor		0.69	W/ $^\circ\text{C}$	
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	290	mJ	
Avalanche Current <sup>a</sup>	$I_{AR}$	3.6	A	
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$	7.4	mJ	
Maximum Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	$P_D$	74	W
Peak Diode Recovery $dV/dt$ <sup>c, e</sup>		$dV/dt$	7.0	V/ns
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$		- 55 to + 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s		300 <sup>d</sup>	

#### Notes


- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).  
 b. Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 46\text{ mH}$ ,  $R_g = 25\text{ }^\circ\Omega$ ,  $I_{AS} = 3.6\text{ A}$  (see fig. 12).  
 c.  $I_{SD} \leq 3.6\text{ A}$ ,  $dI/dt \leq 170\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150\text{ }^\circ\text{C}$ .  
 d. 1.6 mm from case.  
 e. Uses IRFBC30A/SiHFBC30A data and test conditions.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB Mounted, steady-state) <sup>a</sup>	$R_{thJA}$	-	40	°C/W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	1.7	

### Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0, I_D = 250\text{ }\mu\text{A}$	600	-	-	V	
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}^d$	-	0.67	-	V/°C	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	-	4.5	V	
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 30\text{ V}$	-	-	$\pm 100$	nA	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	-	-	25	$\mu\text{A}$	
		$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	250		
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$   $I_D = 2.2\text{ A}^b$	-	-	2.2	$\Omega$	
Forward Transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}, I_D = 2.2\text{ A}$	2.1	-	-	S	
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$ , see fig. 5	-	510	-	pF	
Output Capacitance	$C_{oss}$		-	70	-		
Reverse Transfer Capacitance	$C_{rss}$		-	3.5	-		
Output Capacitance	$C_{oss}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 1.0\text{ V}, f = 1.0\text{ MHz}$	-	730	-	
Effective Output Capacitance	$C_{oss\text{ eff.}}$		$V_{DS} = 480\text{ V}, f = 1.0\text{ MHz}$	-	19	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}$	$I_D = 3.6\text{ A}, V_{DS} = 480\text{ V}$ , see fig. 6 and 13 <sup>b</sup>	-	-	23	nC
Gate-Source Charge	$Q_{gs}$			-	-	5.4	
Gate-Drain Charge	$Q_{gd}$			-	-	11	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 300\text{ V}, I_D = 3.6\text{ A}, R_g = 12\text{ }\Omega, R_D = 82\text{ }\Omega$ , see fig. 10 <sup>b, d</sup>	-	9.8	-	ns	
Rise Time	$t_r$		-	13	-		
Turn-Off Delay Time	$t_{d(off)}$		-	19	-		
Fall Time	$t_f$		-	12	-		
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	3.6	A	
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$		-	-	14		
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 3.6\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	1.6	V	
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = 3.6\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^b$	-	400	600	ns	
Body Diode Reverse Recovery Charge	$Q_{rr}$		-	1.1	1.7	$\mu\text{C}$	
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- $C_{oss\text{ eff.}}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80 %  $V_{DS}$ .
- Uses IRFBC30A/SiHFBC30A data and test conditions.



## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

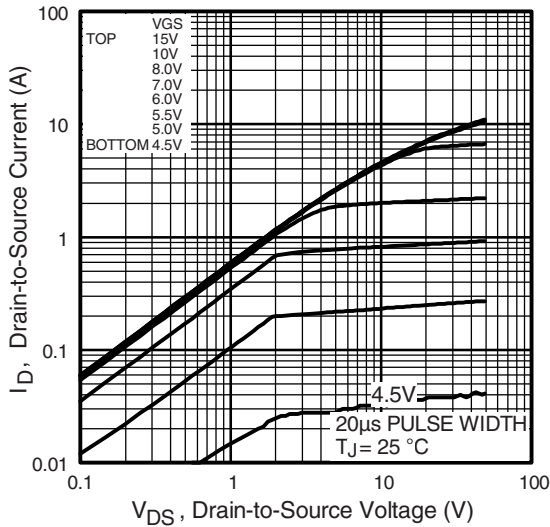


Fig. 1 - Typical Output Characteristics

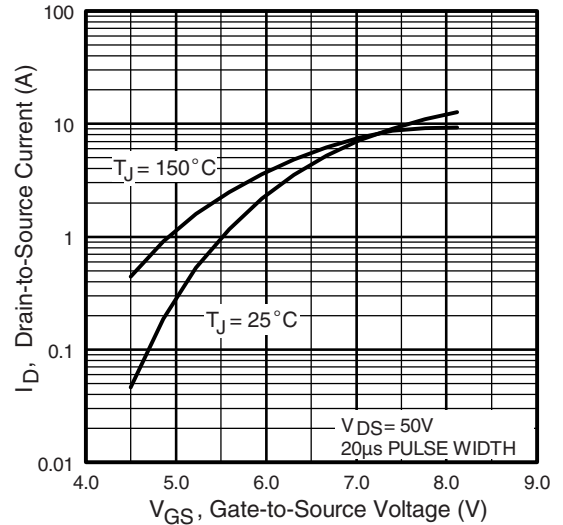


Fig. 3 - Typical Transfer Characteristics

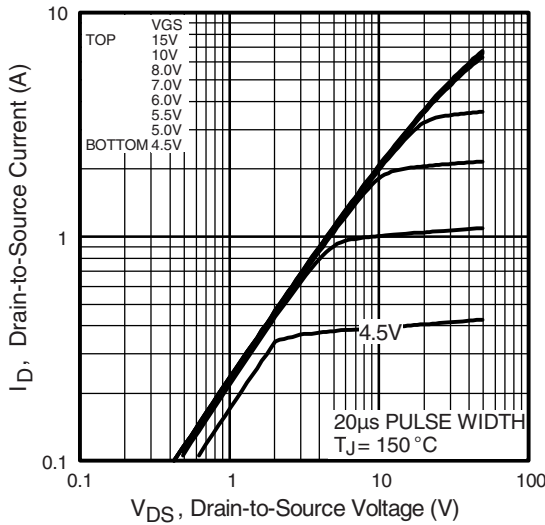


Fig. 2 - Typical Output Characteristics

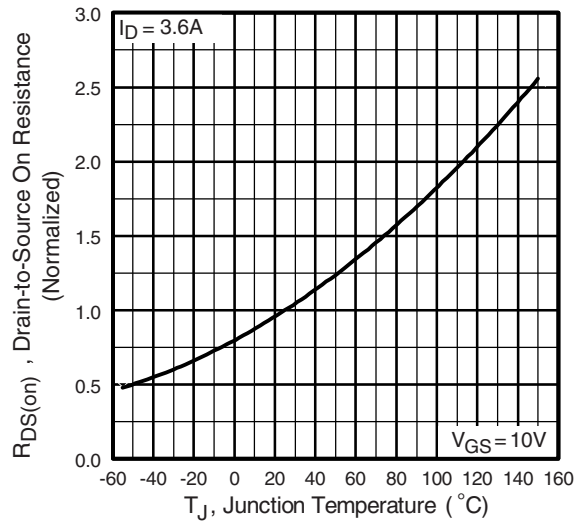


Fig. 4 - Normalized On-Resistance vs. Temperature

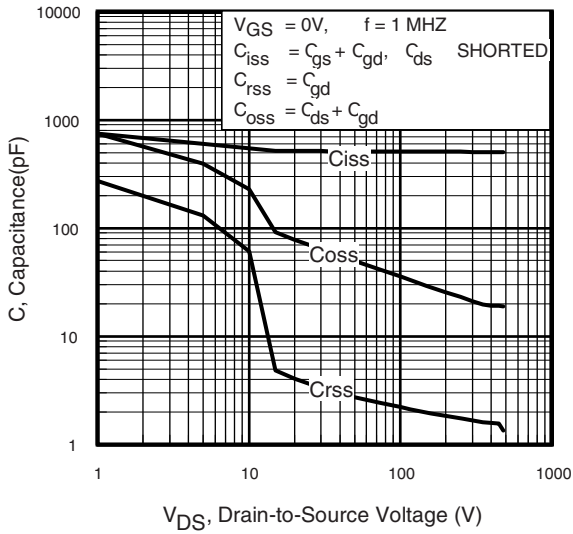


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

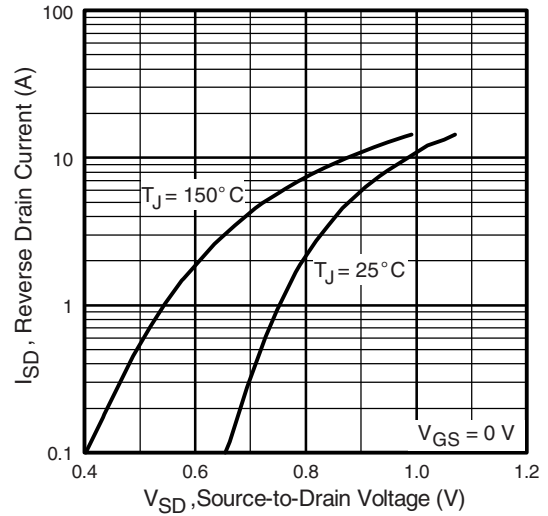


Fig. 7 - Typical Source-Drain Diode Forward Voltage

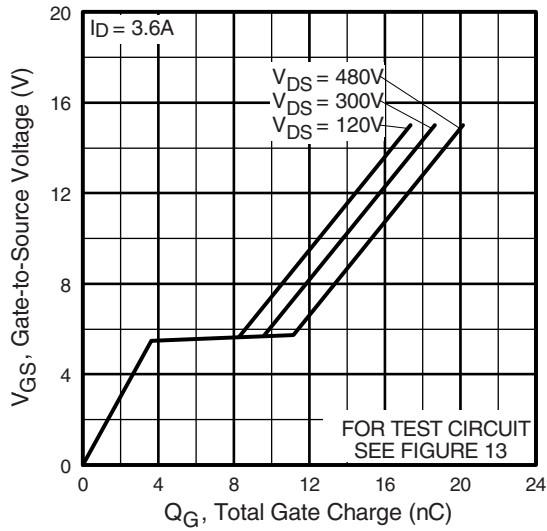


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

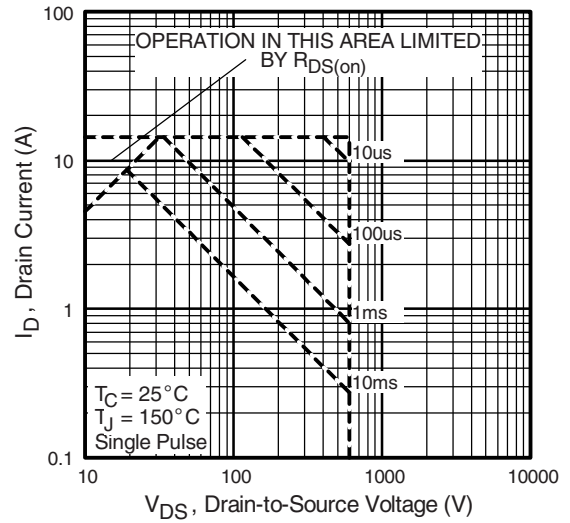
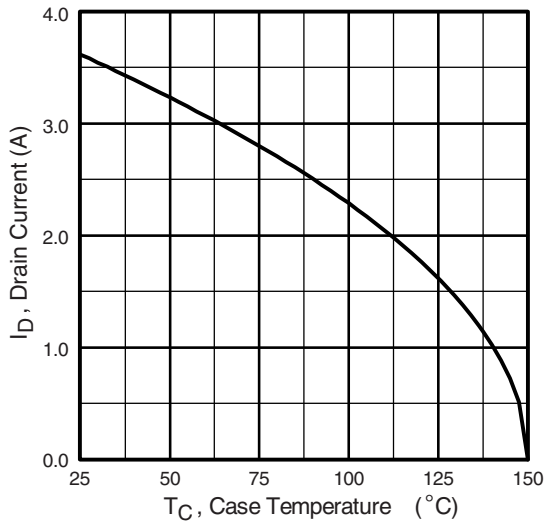
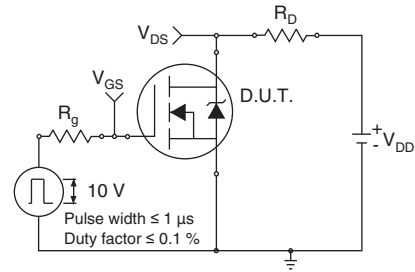


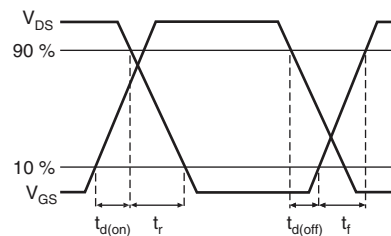
Fig. 8 - Maximum Safe Operating Area



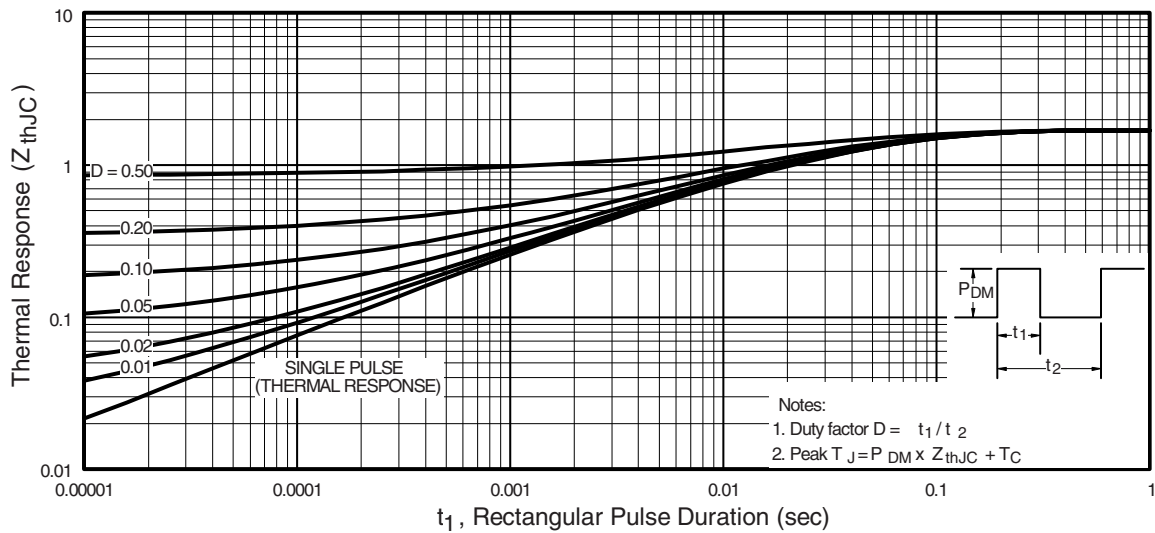
**Fig. 9 - Maximum Drain Current vs. Case Temperature**



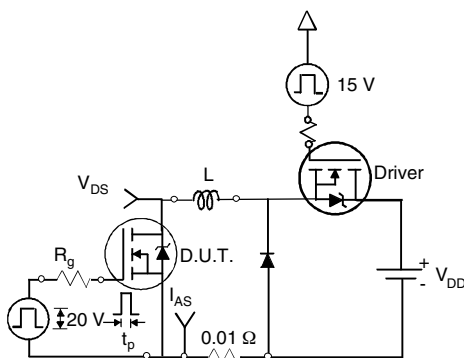
**Fig. 10a - Switching Time Test Circuit**



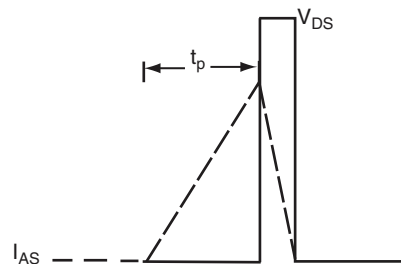
**Fig. 10b - Switching Time Waveforms**



**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**



**Fig. 12a - Unclamped Inductive Test Circuit**



**Fig. 12b - Unclamped Inductive Waveforms**

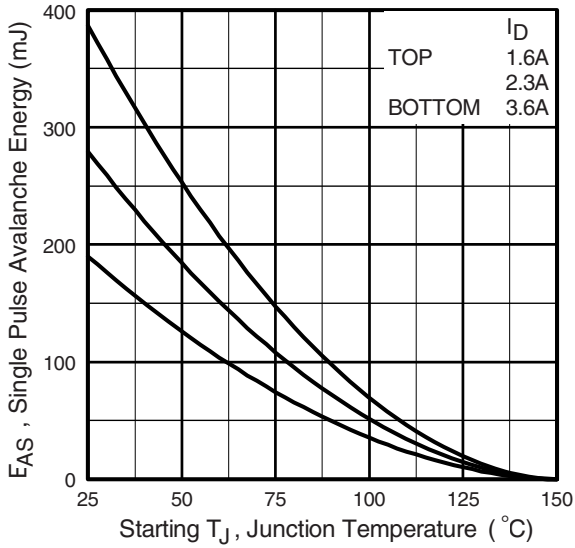


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

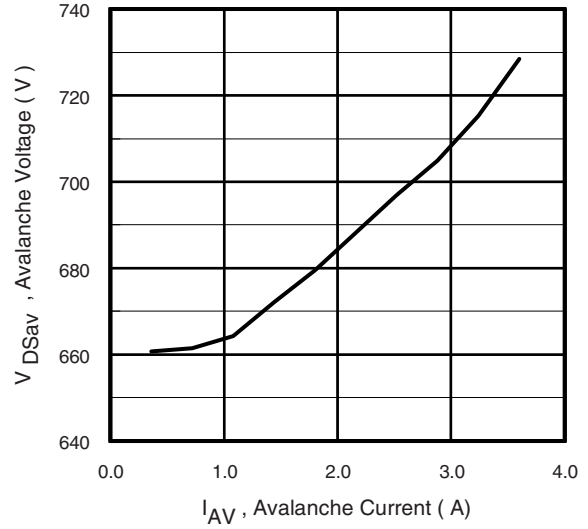


Fig. 12d - Typical Drain-to-Source Voltage vs. Avalanche Current

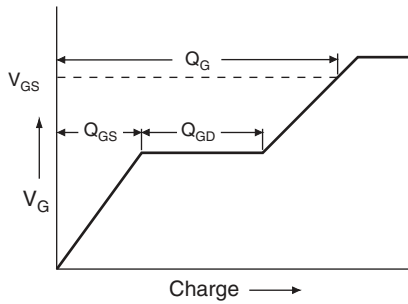


Fig. 13a - Basic Gate Charge Waveform

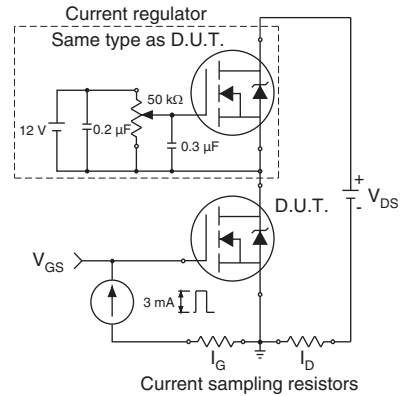
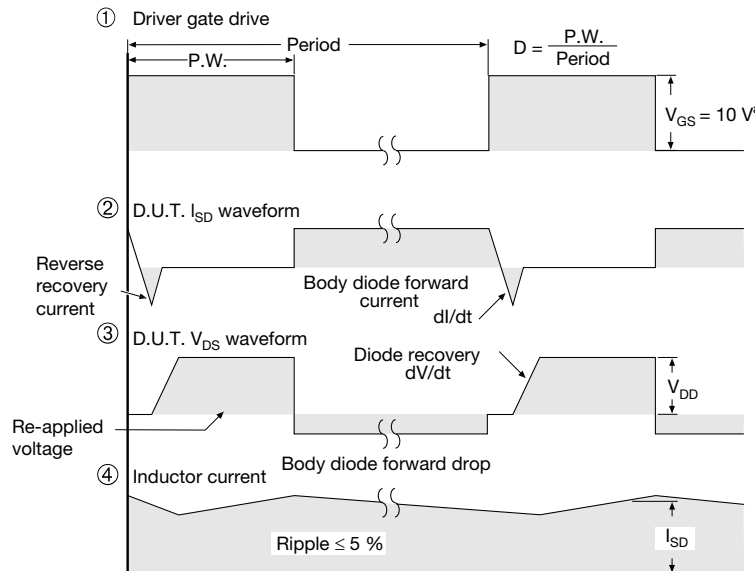


Fig. 13b - Gate Charge Test Circuit



**Note**  
 a.  $V_{GS} = 5 V$  for logic level devices

**Fig. 14 - For N-Channel**

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## TO-220AB

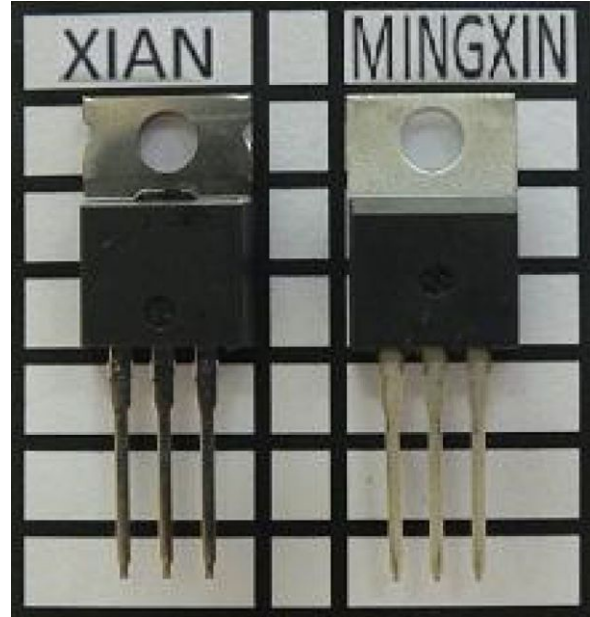


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.25	4.65	0.167	0.183
b	0.69	1.01	0.027	0.040
b(1)	1.20	1.73	0.047	0.068
c	0.36	0.61	0.014	0.024
D	14.85	15.49	0.585	0.610
E	10.04	10.51	0.395	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.09	6.48	0.240	0.255
J(1)	2.41	2.92	0.095	0.115
L	13.35	14.02	0.526	0.552
L(1)	3.32	3.82	0.131	0.150
$\varnothing P$	3.54	3.94	0.139	0.155
Q	2.60	3.00	0.102	0.118

ECN: X12-0208-Rev. N, 08-Oct-12  
DWG: 5471

### Notes

- \* M = 1.32 mm to 1.62 mm (dimension including protrusion)  
Heatsink hole for HVM
- Xi'an and Mingxin actual photo







**RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead**



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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