

# FDB86102LZ

## N-Channel PowerTrench® MOSFET

### 100 V, 30 A, 24 mΩ

#### Features

- Max  $r_{DS(on)}$  = 24 mΩ at  $V_{GS} = 10$  V,  $I_D = 8.3$  A
- Max  $r_{DS(on)}$  = 35 mΩ at  $V_{GS} = 4.5$  V,  $I_D = 6.8$  A
- HBM ESD protection level > 6 kV typical (Note 4)
- Very low Qg and Qgd compared to competing trench technologies
- Fast switching speed
- 100% UIL Tested
- RoHS Compliant

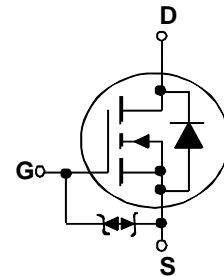
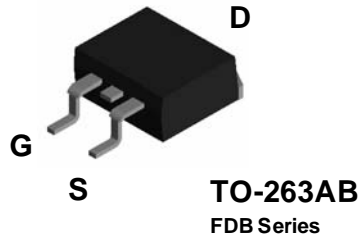


#### General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been especially tailored to minimize the on-state resistance and switching loss. G-S zener has been added to enhance ESD voltage level.

#### Applications

- DC-DC conversion
- Inverter
- Synchronous Rectifier



#### MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

Symbol	Parameter	Conditions	Rated Value	Units
$V_{DS}$	Drain to Source Voltage		100	V
$V_{GS}$	Gate to Source Voltage		±20	V
$I_D$	Drain Current	-Continuous (Package limited)	$T_C = 25$ °C	30
		-Continuous (Silicon limited)	$T_C = 25$ °C	40
		-Continuous	$T_A = 25$ °C (Note 1a)	8.3
		-Pulsed		50
$E_{AS}$	Single Pulse Avalanche Energy	(Note 3)	121	mJ
$P_D$	Power Dissipation	$T_A = 25$ °C (Note 1a)	3.1	W
	Power Dissipation	$T_A = 25$ °C (Note 1b)	2	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range		-55 to +150	°C

#### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Note 1)	1.9	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	40	

#### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB86102LZ	FDB86102LZ	TO-263AB	330mm	24 mm	800 units

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}, V_{GS} = 0\text{ V}$	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		69		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			$\pm 10$	$\mu\text{A}$

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	1.0	1.5	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-6		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 8.3\text{ A}$		18	24	m $\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 6.8\text{ A}$		23	35	
		$V_{GS} = 10\text{ V}, I_D = 8.3\text{ A}, T_J = 125\text{ }^\circ\text{C}$		31	42	
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 8.3\text{ A}$		29		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$		959	1275	pF
$C_{oss}$	Output Capacitance			181	240	pF
$C_{rss}$	Reverse Transfer Capacitance			9	13	pF
$R_g$	Gate Resistance			0.4		$\Omega$

### Switching Characteristics

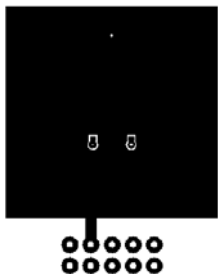
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\text{ V}, I_D = 8.3\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\text{ }\Omega$		6.6	13	ns	
$t_r$	Rise Time			2.1	10	ns	
$t_{d(off)}$	Turn-Off Delay Time			18.2	33	ns	
$t_f$	Fall Time			2.3	10	ns	
$Q_{g(TOT)}$	Total Gate Charge		$V_{GS} = 0\text{ V to } 10\text{ V}$		15.2	21	nC
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\text{ V to } 4.5\text{ V}$	$V_{DD} = 50\text{ V},$ $I_D = 8.3\text{ A}$		7.6	11	nC
$Q_{gs}$	Gate to Source Charge				2.4		nC
$Q_{gd}$	Gate to Drain "Miller" Charge				2.5		nC

### Drain-Source Diode Characteristics

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 8.3\text{ A}$ (Note 2)		0.8	1.3	V
		$V_{GS} = 0\text{ V}, I_S = 2.4\text{ A}$ (Note 2)		0.7	1.2	
$t_{rr}$	Reverse Recovery Time	$I_F = 8.3\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		42	67	ns
$Q_{rr}$	Reverse Recovery Charge			40	64	nC

#### NOTES:

- $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a) 40  $^\circ\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b) 62.5  $^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0 %.

3. Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 3\text{ mH}$ ,  $I_{AS} = 9\text{ A}$ ,  $V_{DD} = 100\text{ V}$ ,  $V_{GS} = 10\text{ V}$ .

4. The diode connected between gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

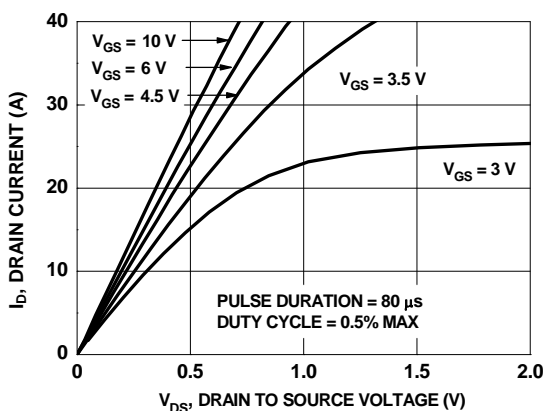


Figure 1. On Region Characteristics

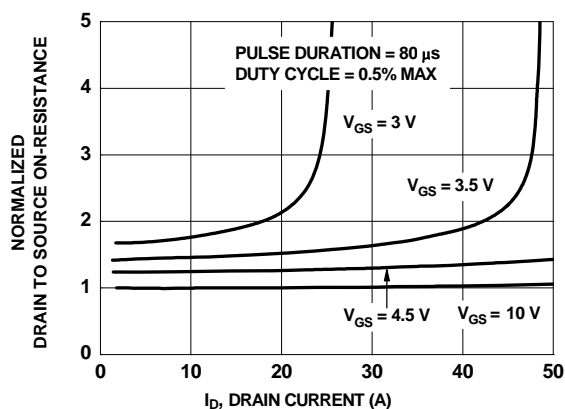


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

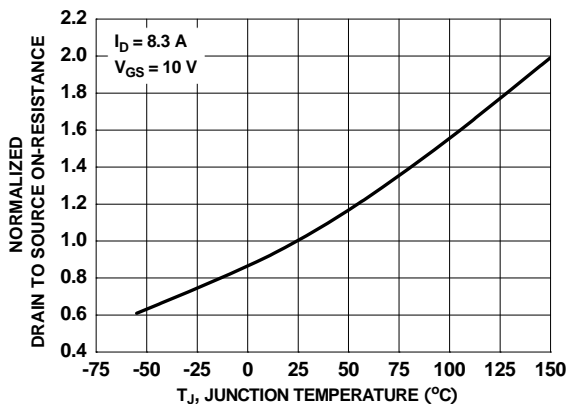


Figure 3. Normalized On Resistance vs Junction Temperature

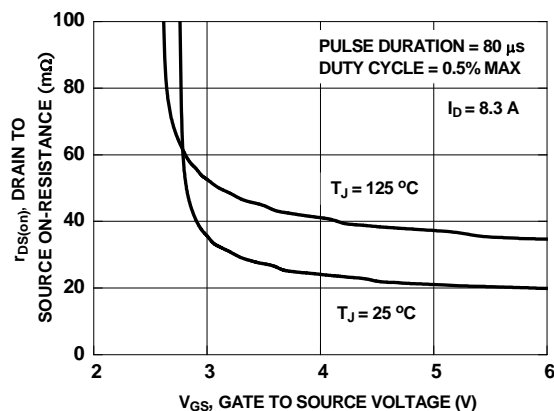


Figure 4. On-Resistance vs Gate to Source Voltage

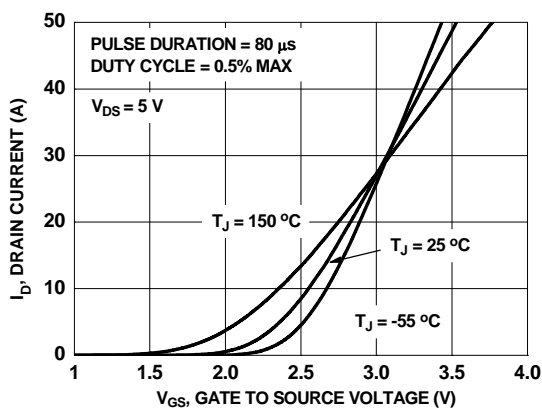


Figure 5. Transfer Characteristics

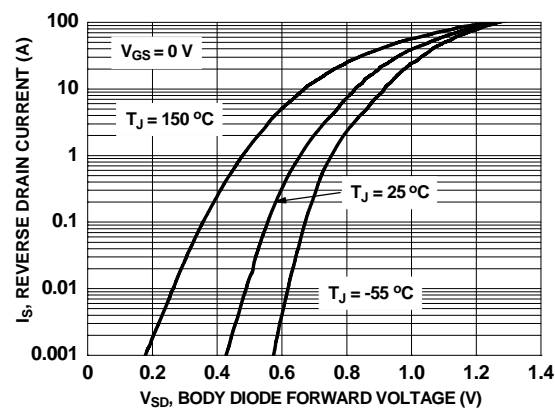
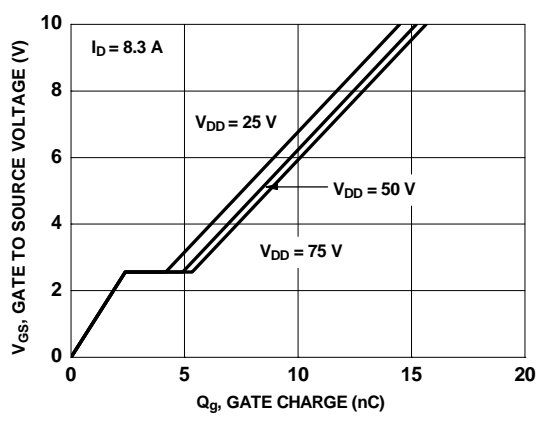
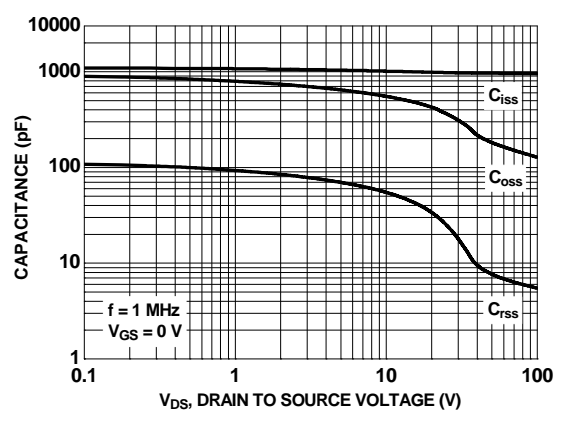


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

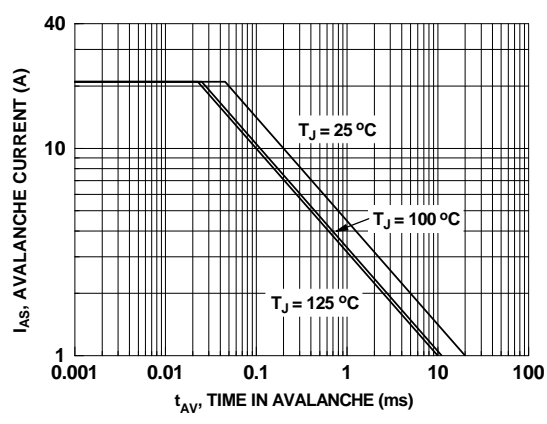
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



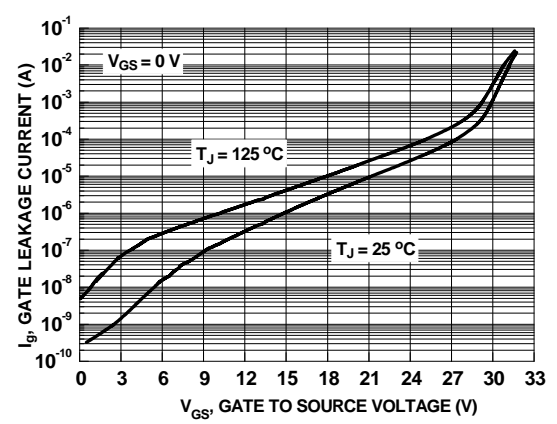
**Figure 7. Gate Charge Characteristics**



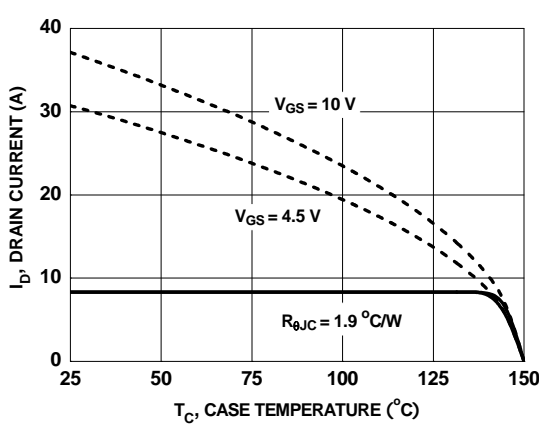
**Figure 8. Capacitance vs Drain to Source Voltage**



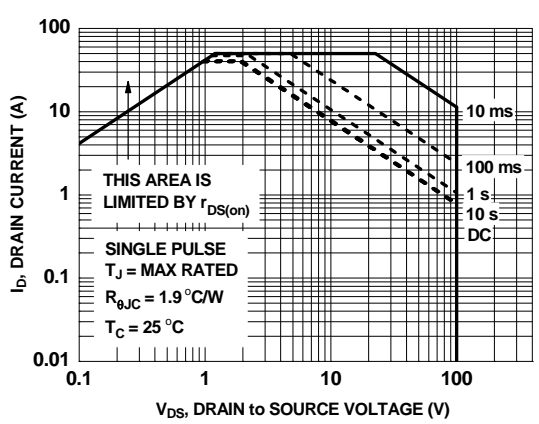
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Gate Leakage Current vs Gate to Source Voltage**

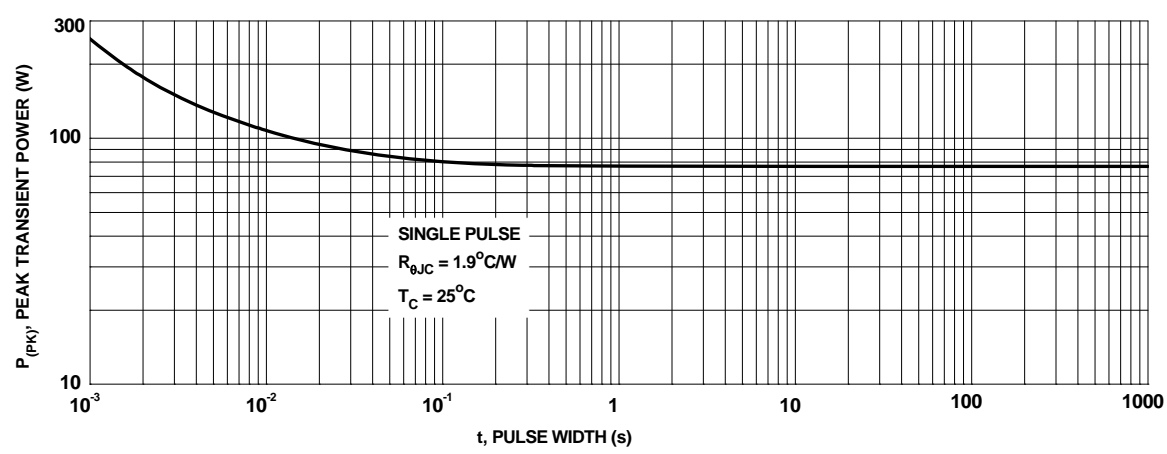


**Figure 11. Maximum Continuous Drain Current vs Case Temperature**

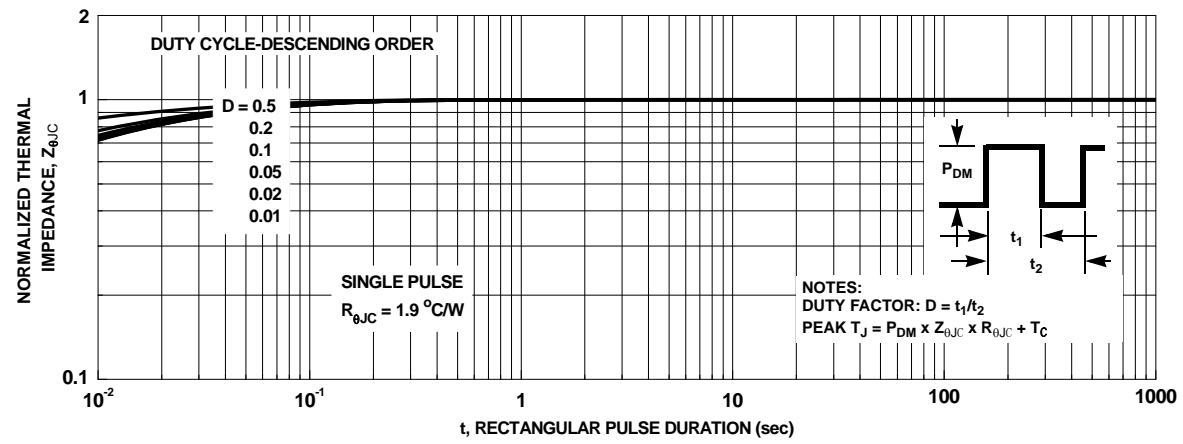


**Figure 12. Forward Bias Safe Operating Area**

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



**Figure 13. Single Pulse Maximum Power Dissipation**



**Figure 14. Junction-to-Case Transient Thermal Response Curve**



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