



N-Channel 20-V (D-S), 175 °C MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ)
20	0.0033 at V _{GS} = 10 V	40	30 nC
	0.0044 at V _{GS} = 4.5 V	40	

FEATURES

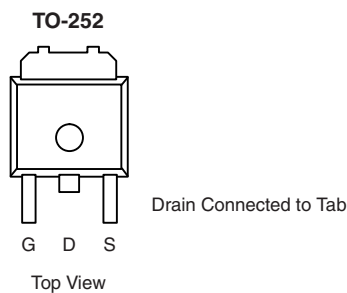
- TrenchFET[®] Power MOSFET
- 100 % R_g Tested



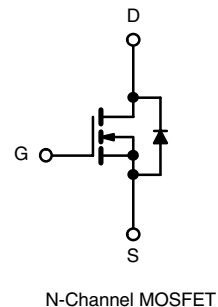
RoHS
COMPLIANT

APPLICATIONS

- Server



Order Number:
SUD40N02-3m3P-E3 (Lead (Pb)-free)



ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	20	V	
Gate-Source Voltage	V _{GS}	± 20		
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	40 ^a	A
		T _C = 100 °C	40 ^a	
		T _A = 25 °C	24.4 ^b	
		T _A = 100 °C	17.2 ^b	
Pulsed Drain Current	I _{DM}	100		
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	40 ^a	
		T _A = 25 °C	2.8 ^b	
Maximum Power Dissipation	P _D	T _C = 25 °C	79	W
		T _C = 100 °C	39.5	
		T _A = 25 °C	3.3 ^b	
		T _A = 100 °C	1.6 ^b	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 175	°C	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^b	Steady State	R _{thJA}	37	45	°C/W
Maximum Junction-to-Case	Steady State	R _{thJC}	1.5	1.9	

Notes:

a. Package limited.

b. Surface Mounted on 1" x 1" FR4 board.

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	20			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		21		mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 6.9		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1		3	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, T_J = 100\text{ }^\circ\text{C}$			20	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	30			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$		0.0027	0.0033	Ω
		$V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$		0.0036	0.0044	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 20\text{ A}$		100		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		6520		pF
Output Capacitance	C_{oss}			1430		
Reverse Transfer Capacitance	C_{rss}			770		
Total Gate Charge	Q_g	$V_{DS} = 10\text{ V}, V_{GS} = 10\text{ V}, I_D = 50\text{ A}$		105	160	nC
				50	75	
Gate-Source Charge	Q_{gs}	$V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 50\text{ A}$		17		nC
Gate-Drain Charge	Q_{gd}			14		
Gate Resistance	R_g		$f = 1\text{ MHz}$		1.2	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\text{ V}, R_L = 0.2\text{ }\Omega$ $I_D \cong 50\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$		40	60	ns
Rise Time	t_r			30	45	
Turn-Off Delay Time	$t_{d(off)}$			67	101	
Fall Time	t_f			33	50	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\text{ V}, R_L = 0.2\text{ }\Omega$ $I_D \cong 50\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		13	20	ns
Rise Time	t_r			7	11	
Turn-Off Delay Time	$t_{d(off)}$			40	60	
Fall Time	t_f			9	14	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			40	A
Pulse Diode Forward Current ^a	I_{SM}				100	
Body Diode Voltage	V_{SD}	$I_S = 20\text{ A}$		0.81	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 50\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		38	57	ns
Body Diode Reverse Recovery Charge	Q_{rr}			34	51	nC
Reverse Recovery Fall Time	t_a			18		ns
Reverse Recovery Rise Time	t_b			20		

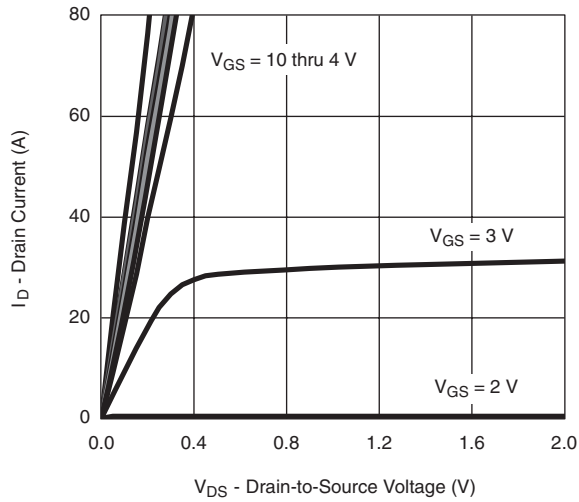
Notes:

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

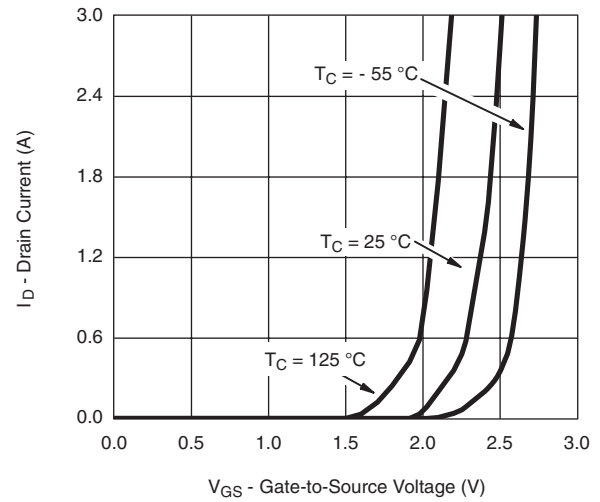
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



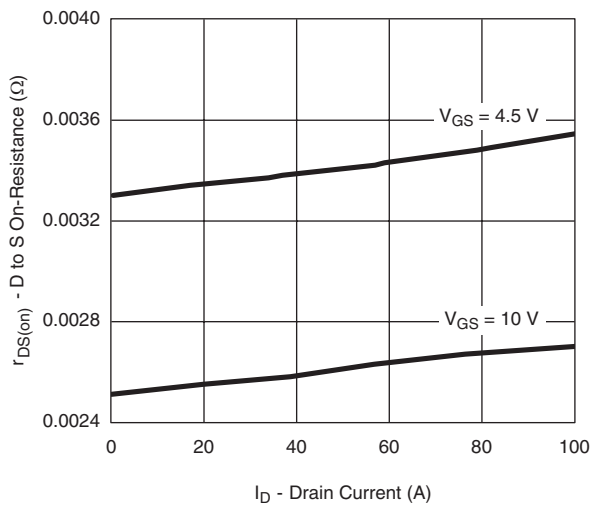
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



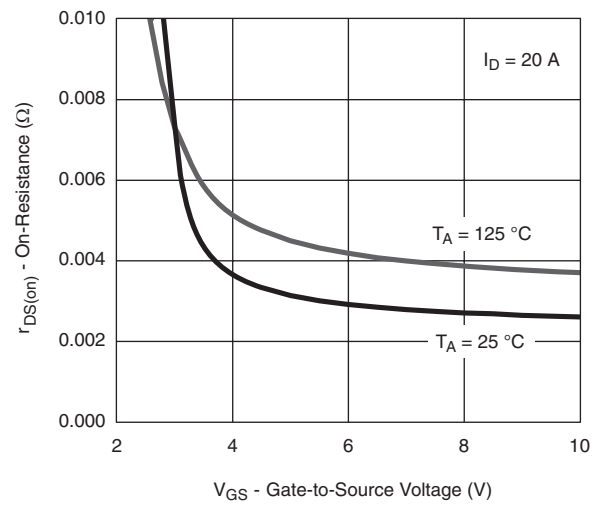
Output Characteristics



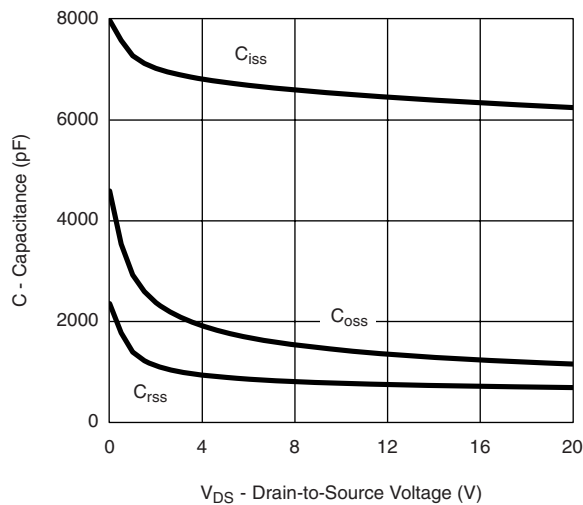
Transfer Characteristics



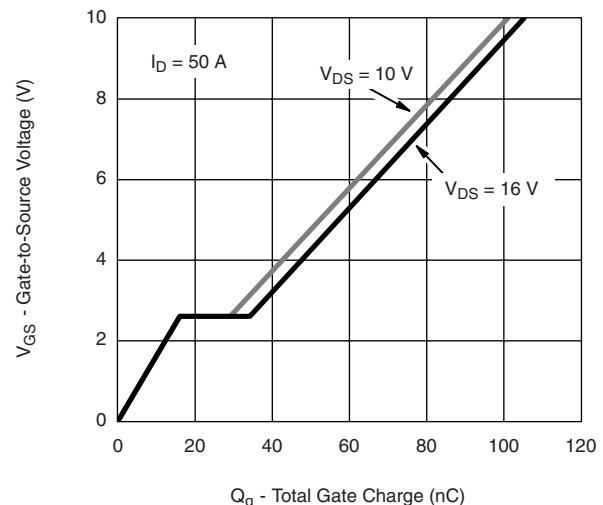
On-Resistance vs. Drain Current



On-Resistance vs. V_{GS} vs. Temperature



Capacitance



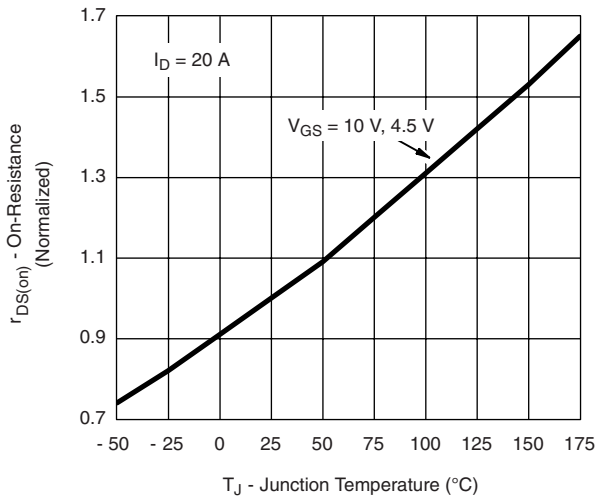
Gate Charge

SUD40N02-3m3P

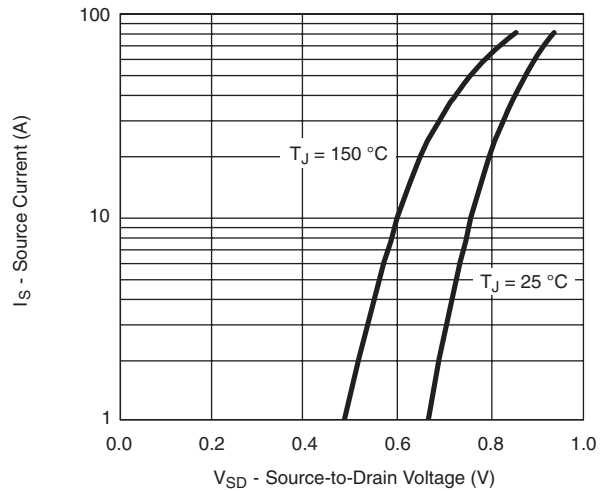


Vishay Siliconix

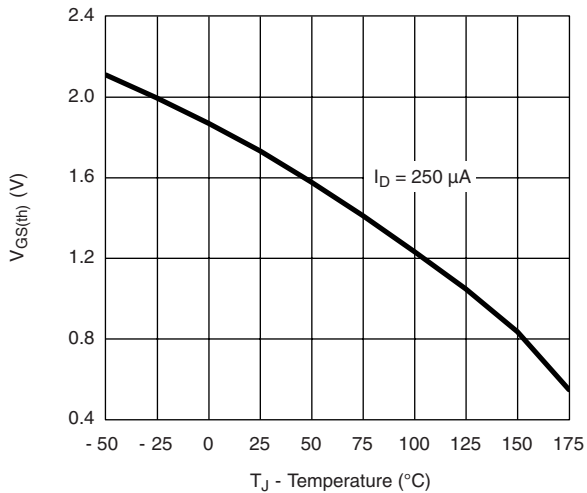
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



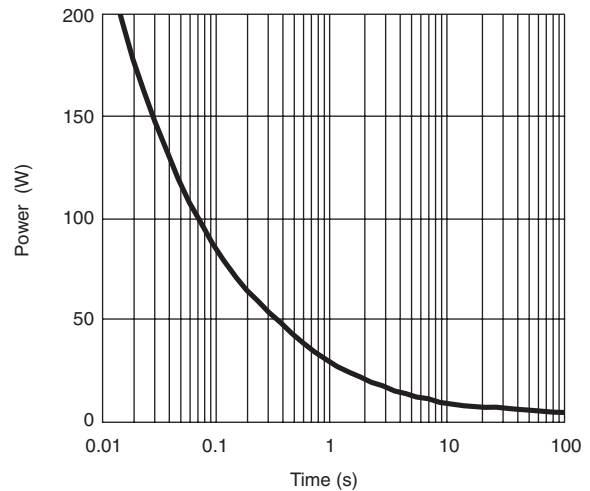
On-Resistance vs. Junction Temperature



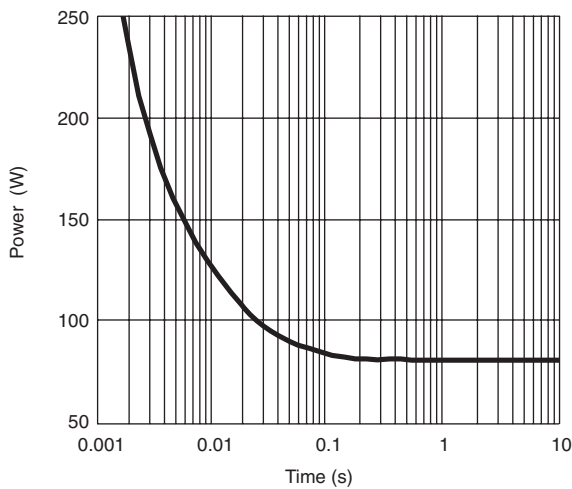
Forward Diode Voltage vs. Temperature



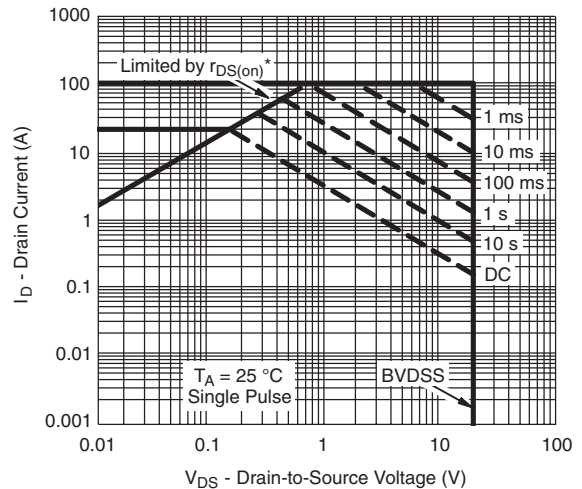
Threshold Voltage



Single Pulse Power, Junction-to-Ambient



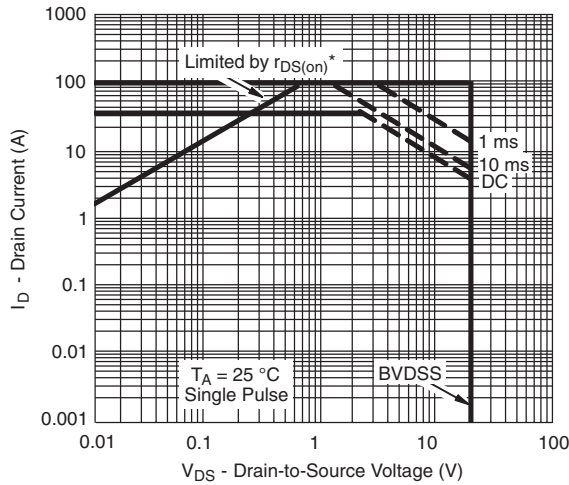
Single Pulse Power, Junction-to-Case



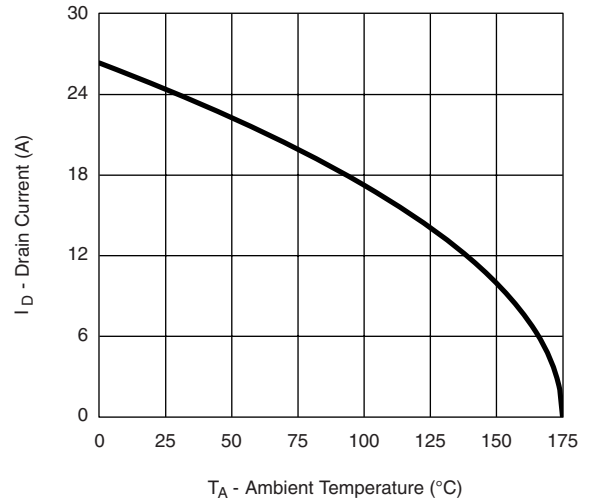
Safe Operating Area, Junction-to-Ambient



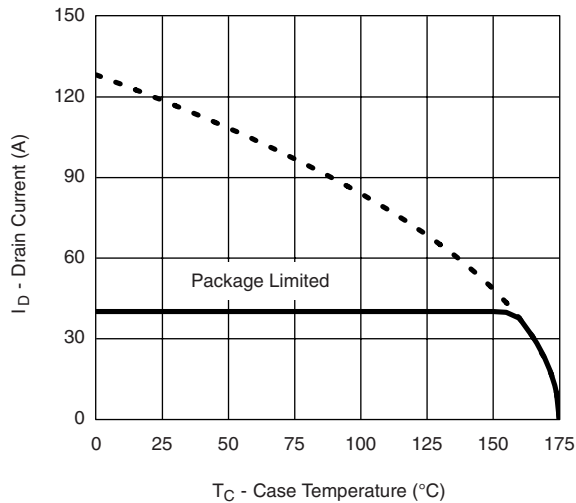
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



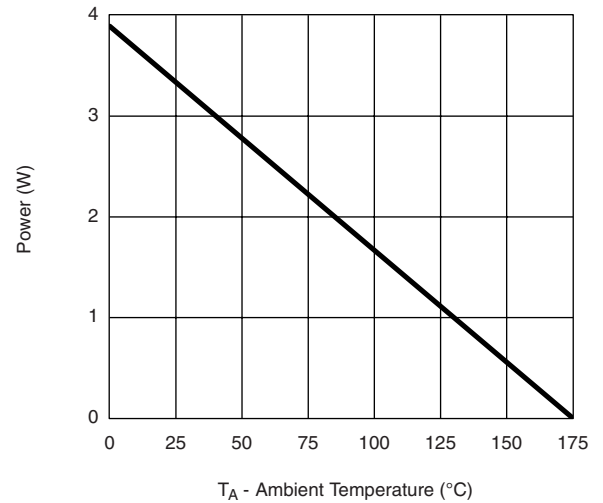
* $V_{GS} >$ minimum V_{GS} at which $r_{DS(on)}$ is specified
Safe Operating Area, Junction-to-Case



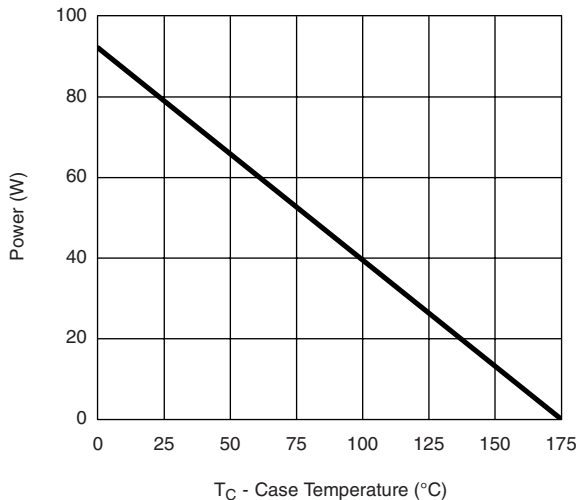
Current Derating, Junction-to-Ambient**



Current Derating, Junction-to-Case**



Power Derating, Junction-to-Ambient**



Power Derating, Junction-to-Case**

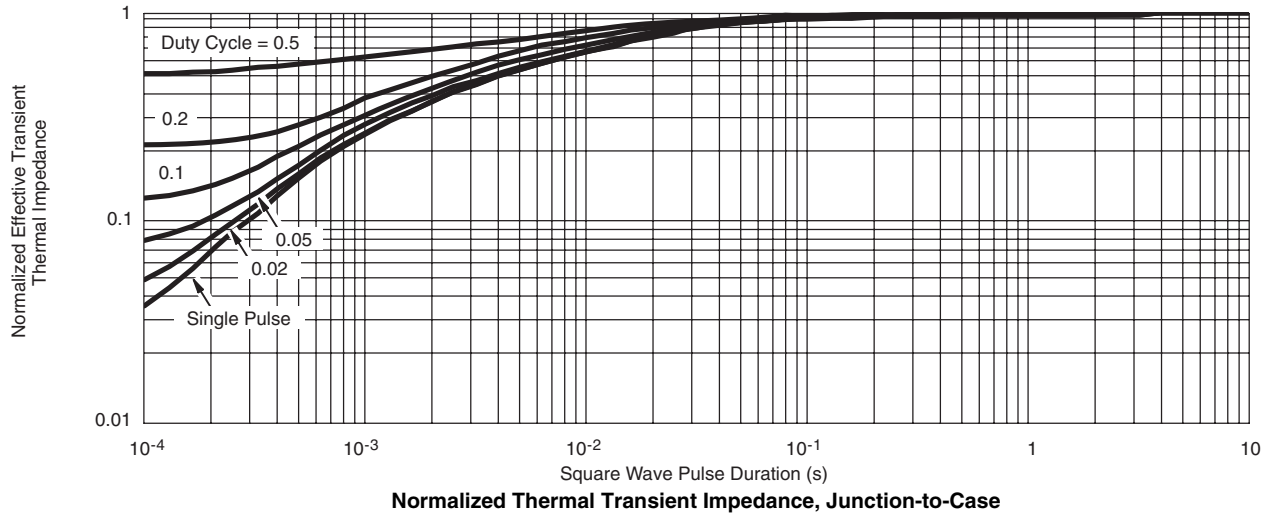
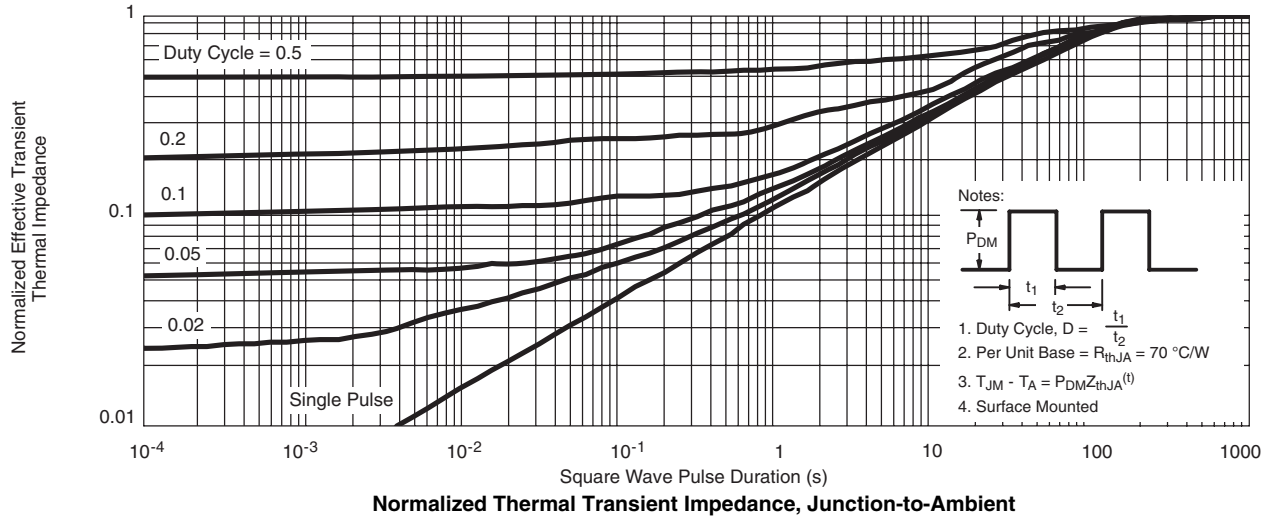
** The power dissipation P_D is based on $T_{J(max)} = 175$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

SUD40N02-3m3P



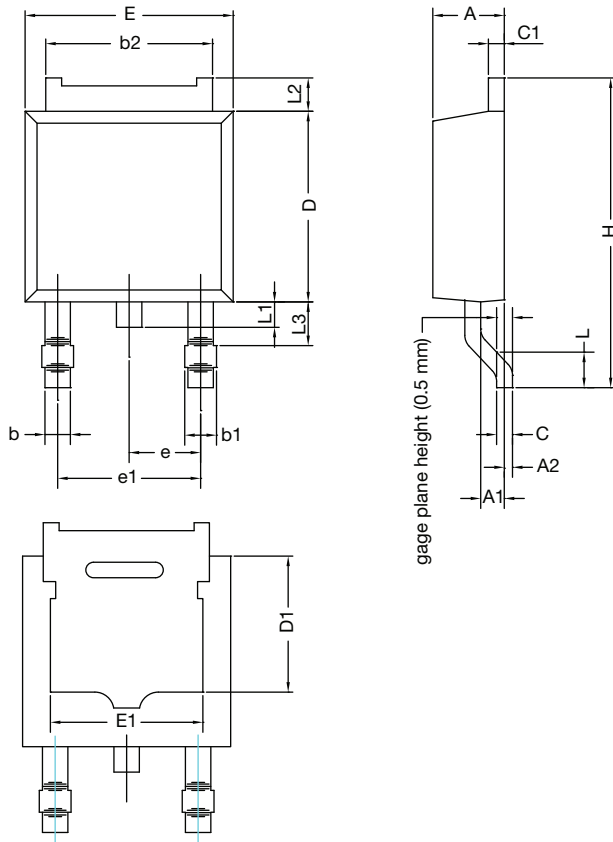
Vishay Siliconix

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?69819>.

TO-252AA CASE OUTLINE



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.21	2.38	0.087	0.094
A1	0.89	1.14	0.035	0.045
A2	0.030	0.127	0.001	0.005
b	0.71	0.88	0.028	0.035
b1	0.76	1.14	0.030	0.045
b2	5.23	5.44	0.206	0.214
C	0.46	0.58	0.018	0.023
C1	0.46	0.58	0.018	0.023
D	5.97	6.22	0.235	0.245
D1	4.10	4.45	0.161	0.175
E	6.48	6.73	0.255	0.265
E1	4.49	5.50	0.177	0.217
e	2.28 BSC		0.090 BSC	
e1	4.57 BSC		0.180 BSC	
H	9.65	10.41	0.380	0.410
L	1.40	1.78	0.055	0.070
L1	0.64	1.02	0.025	0.040
L2	0.89	1.27	0.035	0.050
L3	1.15	1.52	0.040	0.060

ECN: T11-0110-Rev. L, 18-Apr-11
DWG: 5347

Note

- Dimension L3 is for reference only.

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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