

P-Channel 40-V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ.)
- 40	0.0081 at $V_{GS} = - 10$ V	- 50 ^d	60
	0.0117 at $V_{GS} = - 4.5$ V	- 48 ^d	

FEATURES

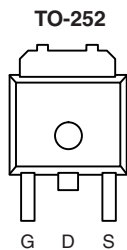
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFET
- 100 % R_g and UIS Tested
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE

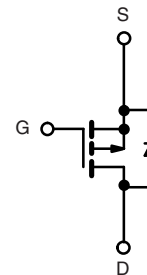
APPLICATIONS

- Power Switch
- Load Switch in High Current Applications
- DC/DC Converters



Top View

Drain Connected to Tab

Ordering Information: SUD50P04-08-GE3 (Lead (Pb)-free and Halogen-free)


P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V_{DS}	- 40	V	
Gate-Source Voltage	V_{GS}	± 20		
Continuous Drain Current ($T_J = 150$ °C)	I_D	$T_C = 25$ °C	- 50 ^d	A
		$T_C = 70$ °C	- 50 ^d	
Pulsed Drain Current	I_{DM}	- 100		
Avalanche Current	I_{AS}	- 46		
Single Avalanche Energy ^a	E_{AS}	106	mJ	
Maximum Power Dissipation ^a	P_D	$T_C = 25$ °C	73.5 ^b	W
		$T_A = 25$ °C ^c	2.5	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Limit	Unit	
Junction-to-Ambient (PCB Mount) ^c	R_{thJA}	50	°C/W	
Junction-to-Case (Drain)	R_{thJC}	1.7		

Notes:

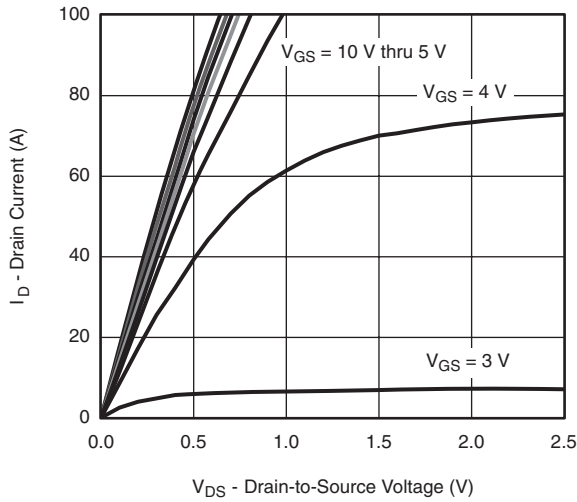
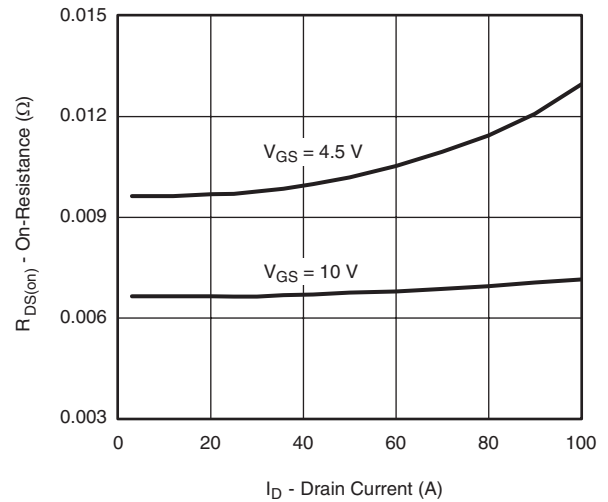
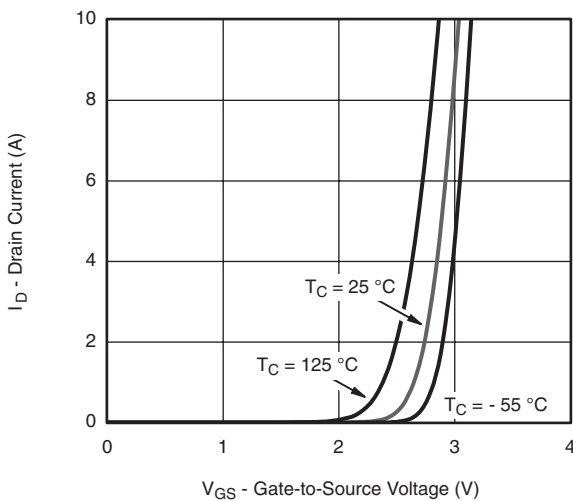
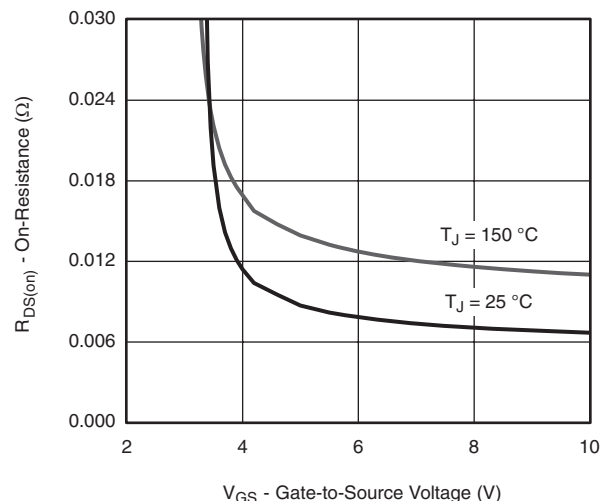
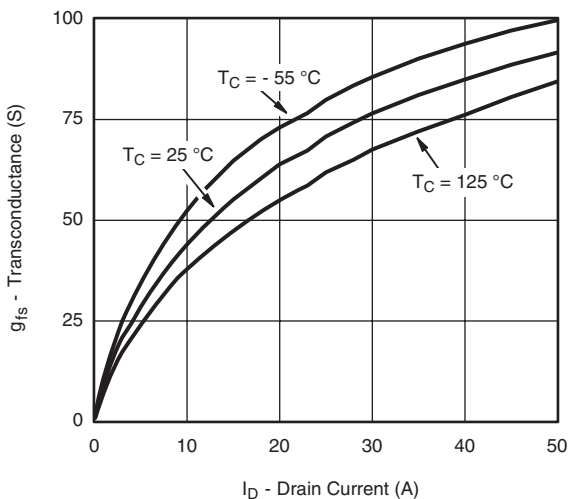
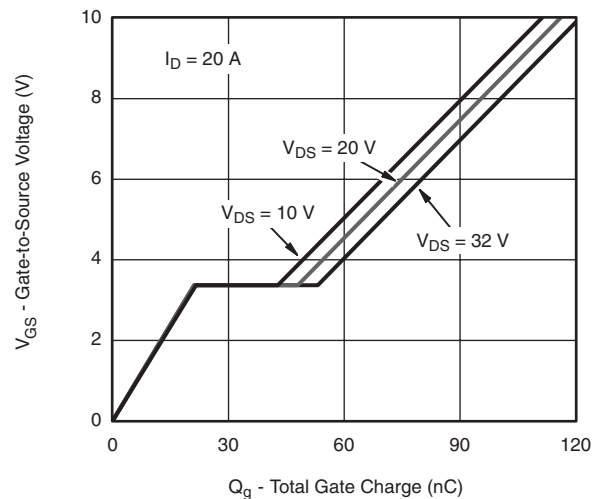
- Duty cycle ≤ 1 %.
- See SOA curve for voltage derating.
- When Mounted on 1" square PCB (FR-4 material).
- Package limited.

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{DS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	- 40			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	- 1		- 2.5	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 250	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -40\text{ V}, V_{GS} = 0\text{ V}$			- 1	μA
		$V_{DS} = -40\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$			- 50	
		$V_{DS} = -40\text{ V}, V_{GS} = 0\text{ V}, T_J = 150\text{ }^\circ\text{C}$			- 250	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \leq -10\text{ V}, V_{GS} = -10\text{ V}$	- 50			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -22\text{ A}$		0.0067	0.0081	Ω
		$V_{GS} = -4.5\text{ V}, I_D = -19\text{ A}$		0.0097	0.0117	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -15\text{ V}, I_D = -22\text{ A}$		45		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = -20\text{ V}, f = 1\text{ MHz}$		5380		μF
Output Capacitance	C_{oss}			570		
Reverse Transfer Capacitance	C_{rss}			500		
Total Gate Charge ^c	Q_g	$V_{DS} = -20\text{ V}, V_{GS} = -10\text{ V}, I_D = -20\text{ A}$		106	159	nC
		$V_{DS} = -20\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -20\text{ A}$		60	90	
Gate-Source Charge ^c	Q_{gs}			22		
Gate-Drain Charge ^c	Q_{gd}		27			
Gate Resistance	R_g	$f = 1\text{ MHz}$	0.4	1.8	3.6	Ω
Turn-On Delay Time ^c	$t_{d(on)}$	$V_{DD} = -20\text{ V}, R_L = 2\text{ }\Omega$ $I_D \cong -10\text{ A}, V_{GEN} = -10\text{ V}, R_g = 1\text{ }\Omega$		15	23	ns
Rise Time ^c	t_r			12	18	
Turn-Off Delay Time ^c	$t_{d(off)}$			70	105	
Fall Time ^c	t_f			18	27	
Drain-Source Body Diode Ratings and Characteristics $T_C = 25\text{ }^\circ\text{C}$ ^b						
Continuous Current	I_S				- 50	A
Pulsed Current	I_{SM}				- 100	
Forward Voltage ^a	V_{SD}	$I_F = -10\text{ A}, V_{GS} = 0\text{ V}$		- 0.8	- 1.5	V
Reverse Recovery Time	t_{rr}	$I_F = -10\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}$		35	53	ns
Peak Reverse Recovery Current	$I_{RM(REC)}$			- 2	- 3	A
Reverse Recovery Charge	Q_{rr}			33	50	nC

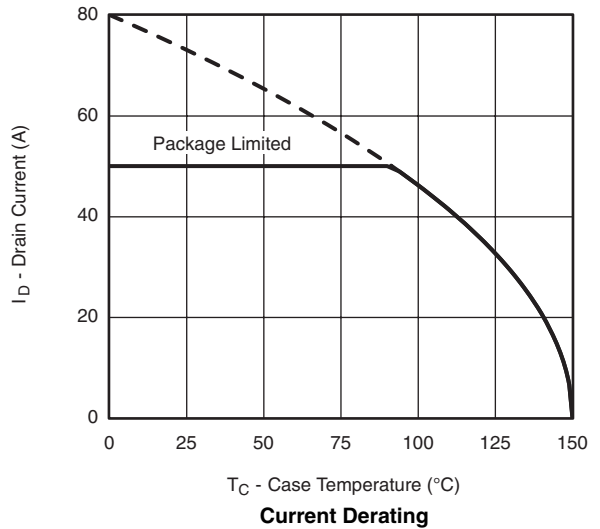
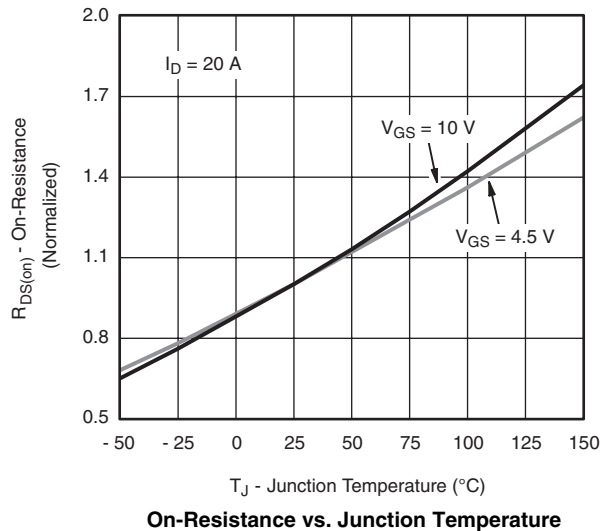
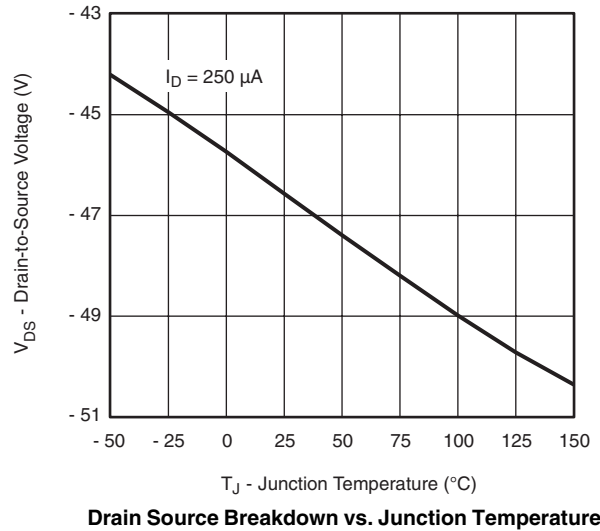
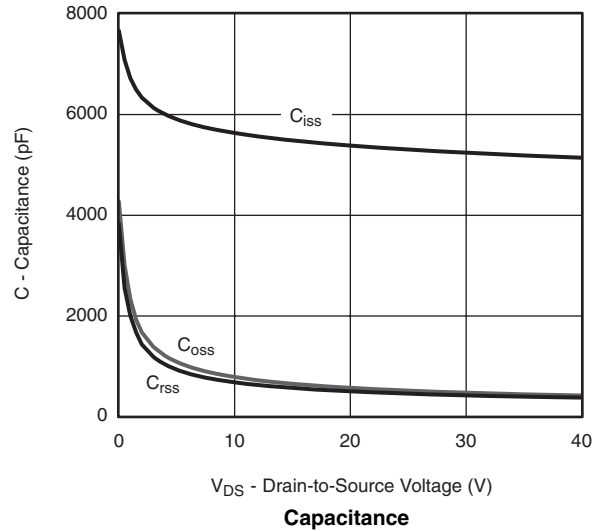
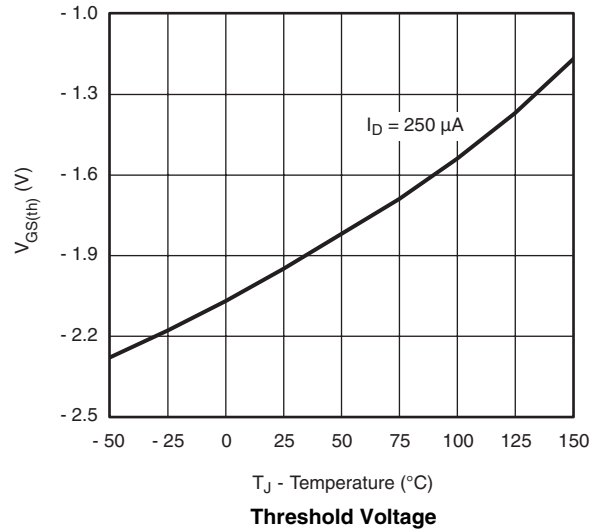
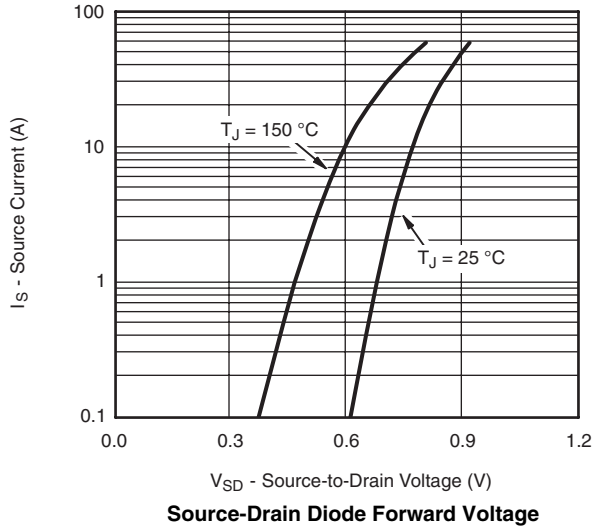
Notes:

- Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.
- Independent of operating temperature.

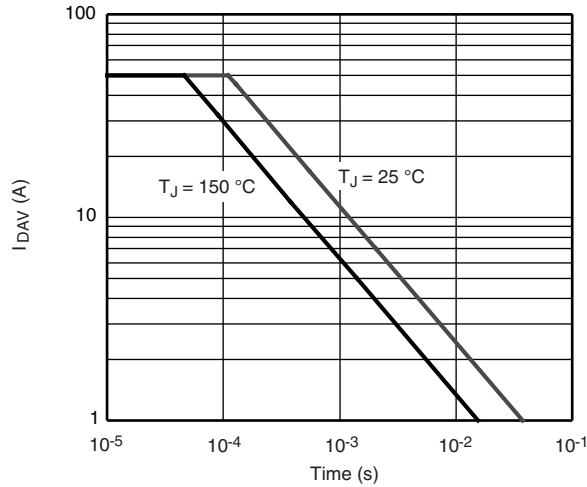
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

Output Characteristics

On-Resistance vs. Drain Current

Transfer Characteristics

On-Resistance vs. Gate-to-Source Voltage

Transconductance

Gate Charge

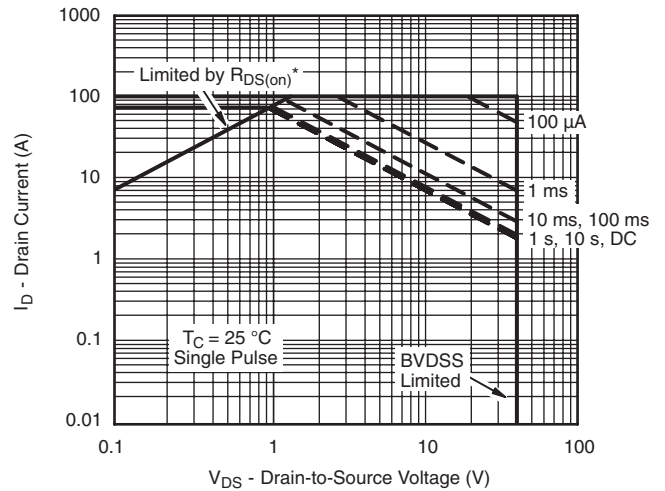
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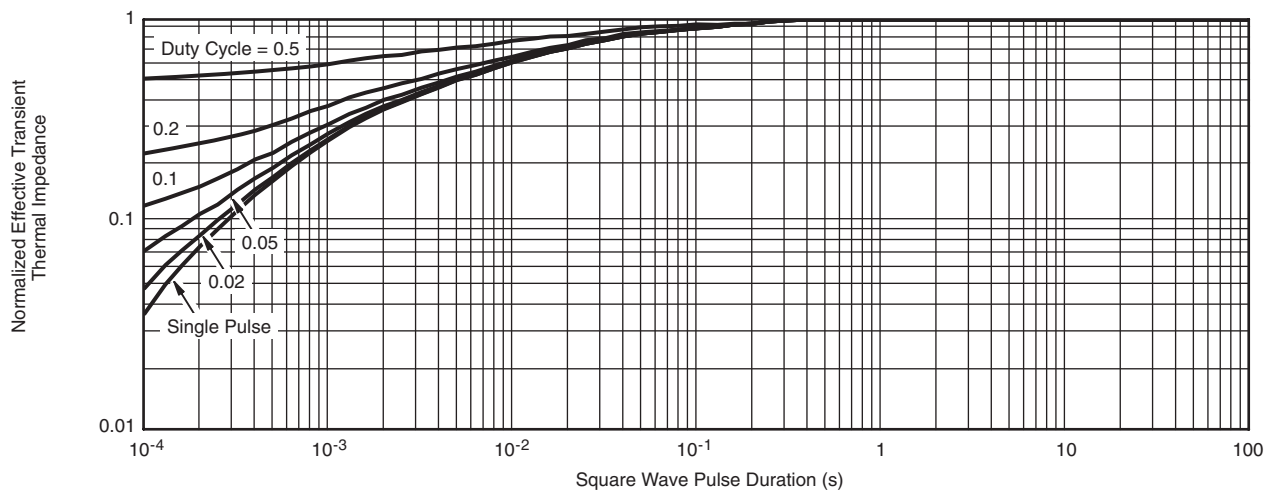


Single Pulse Avalanche Current Capability vs. Time



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

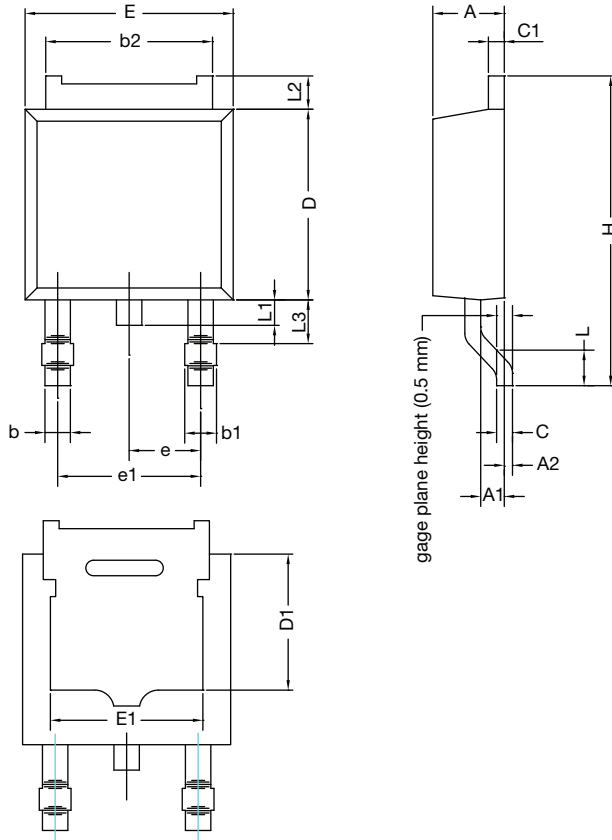
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case

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TO-252AA CASE OUTLINE



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.21	2.38	0.087	0.094
A1	0.89	1.14	0.035	0.045
A2	0.030	0.127	0.001	0.005
b	0.71	0.88	0.028	0.035
b1	0.76	1.14	0.030	0.045
b2	5.23	5.44	0.206	0.214
C	0.46	0.58	0.018	0.023
C1	0.46	0.58	0.018	0.023
D	5.97	6.22	0.235	0.245
D1	4.10	4.45	0.161	0.175
E	6.48	6.73	0.255	0.265
E1	4.49	5.50	0.177	0.217
e	2.28 BSC		0.090 BSC	
e1	4.57 BSC		0.180 BSC	
H	9.65	10.41	0.380	0.410
L	1.40	1.78	0.055	0.070
L1	0.64	1.02	0.025	0.040
L2	0.89	1.27	0.035	0.050
L3	1.15	1.52	0.040	0.060
ECN: T11-0110-Rev. L, 18-Apr-11 DWG: 5347				

Note

- Dimension L3 is for reference only.

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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