



# P-Channel 1.8 V (G-S) MOSFET

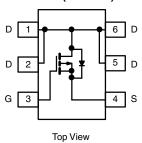
PRODUCT SUMMARY				
V <sub>DS</sub> (V)	$R_{DS(on)}(\Omega)$	I <sub>D</sub> (A)		
	0.195 at V <sub>GS</sub> = - 4.5 V	- 0.84		
- 20	0.260 at V <sub>GS</sub> = - 2.5 V	- 0.73		
	0.350 at V <sub>GS</sub> = - 1.8 V	- 0.64		

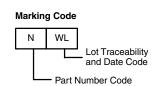
### **FEATURES**

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET<sup>®</sup> Power MOSFET
- Low Threshold
- Smallest LITTLE FOOT<sup>®</sup> Package: 1.6 mm x 1.6 mm
- Low 0.6 mm Profile
- Compliant to RoHS Directive 2002/95/EC









Ordering Information: Si1037X-T1-GE3 (Lead (Pb)-free and Halogen-free)

### **APPLICATIONS**

- Cell Phones and Pagers
  - Load Switch
- · Battery Operated Systems

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C, unless otherwise noted)					
Parameter		Symbol	5 s	Steady State	Unit
Drain-Source Voltage		V <sub>DS</sub>	- 20		V
Gate-Source Voltage		V <sub>GS</sub>	± 8		
Continuous Drain Current /T 150 °C\a	T <sub>A</sub> = 25 °C	- I <sub>D</sub>	- 0.84	- 0.77	A
Continuous Drain Current (T <sub>J</sub> = 150 °C) <sup>a</sup>	T <sub>A</sub> = 70 °C		- 0.68	- 0.62	
Pulsed Drain Current		I <sub>DM</sub>	- 4		A
Continuous Diode Current (Diode Conduction) <sup>a</sup>		I <sub>S</sub>	- 0.18	- 0.14	
Mariana Barra Biraira kand	T <sub>A</sub> = 25 °C	- P <sub>D</sub>	0.21	0.17	W
Maximum Power Dissipation <sup>a</sup>	T <sub>A</sub> = 70 °C		0.13	0.10	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150		°C

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maniana da Ambianta	t ≤ 5 s	R <sub>thJA</sub>	500	600	°C/W	
Maximum Junction-to-Ambient <sup>a</sup>	Steady State	' ¹thJA	600	720	C/ <b>VV</b>	

#### Notes

a. Surface mounted on 1" x 1" FR4 board with minimum copper.

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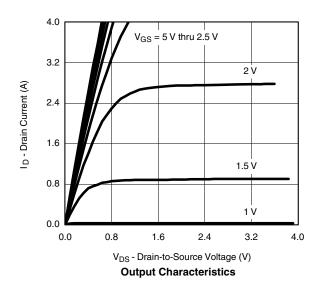
<b>SPECIFICATIONS</b> (T <sub>J</sub> = 25 °C, unless otherwise noted)							
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	- 0.45			V	
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 8 \text{ V}$			± 100	nA	
Zava Cata Valtaga Dvain Current	,	V <sub>DS</sub> = - 20 V, V <sub>GS</sub> = 0 V	V -1		- 1		
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = - 20 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 70 °C			- 5 μA		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = - 5 V, V <sub>GS</sub> = - 4.5 V	- 4			Α	
		V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 0.77 A		0.160	0.195	Ω	
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = - 2.5 V, I <sub>D</sub> = - 0.67 A		0.212	0.260		
		V <sub>GS</sub> = - 1.8 V, I <sub>D</sub> = - 0.2 A		0.290	0.350		
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = - 10 V, I <sub>D</sub> = - 0.77 A		3.1		S	
Diode Forward Voltage <sup>a</sup>	$V_{SD}$	I <sub>S</sub> = - 0.14 A, V <sub>GS</sub> = 0 V		- 0.78	- 1.2	V	
Dynamic <sup>b</sup>							
Total Gate Charge	Qg			3.5	5.5		
Gate-Source Charge	Q <sub>gs</sub>	$V_{DS} = -10 \text{ V}, V_{GS} = -4.5 \text{ V}, I_{D} = -0.77 \text{ A}$		0.65		nC	
Gate-Drain Charge	$Q_{gd}$			0.60		1	
Turn-On Delay Time	t <sub>d(on)</sub>			10	20		
Rise Time	t <sub>r</sub>	$V_{DD}$ = - 10 V, $R_L$ = 20 $\Omega$		15	30		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_{D} \cong -0.5 \text{ A}, V_{GEN} = -4.5 \text{ V}, R_{G} = 6 \Omega$		30	60	ns	
Fall Time	t <sub>f</sub>			10	20		
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = - 0.14 A, dl/dt = 100 A/μs		20	40		

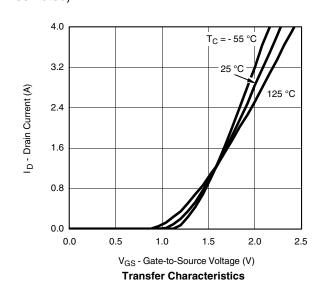
### Notes:

- a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

# **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)

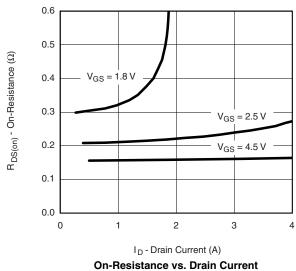


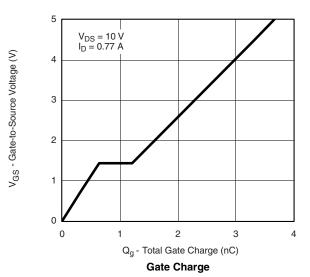


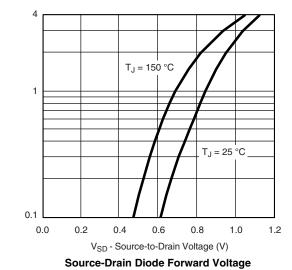


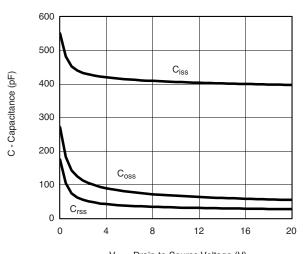


# **TYPICAL CHARACTERISTICS** ( $T_A = 25$ °C, unless otherwise noted)



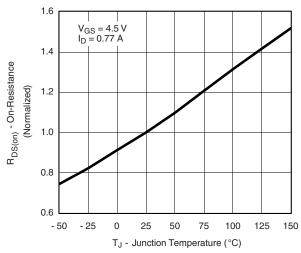




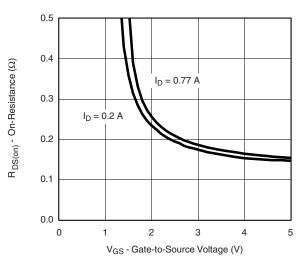


V<sub>DS</sub> - Drain-to-Source Voltage (V)





On-Resistance vs. Junction Temperature



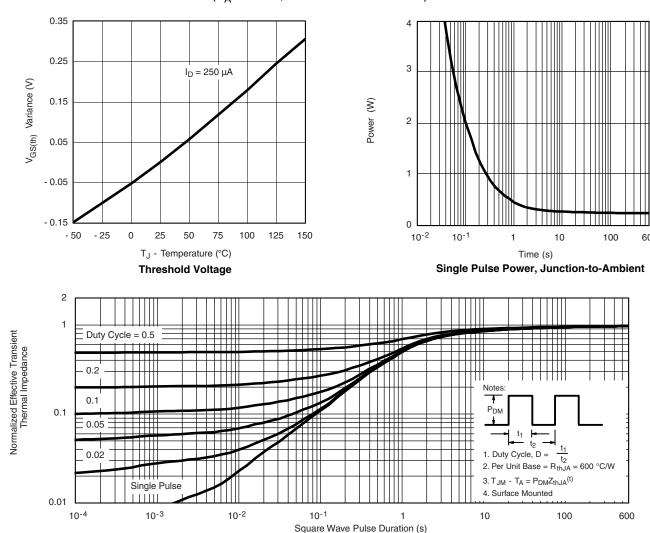
On-Resistance vs. Gate-to-Source Voltage

Is - Source Current (A)

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# **TYPICAL CHARACTERISTICS** ( $T_A = 25$ °C, unless otherwise noted)

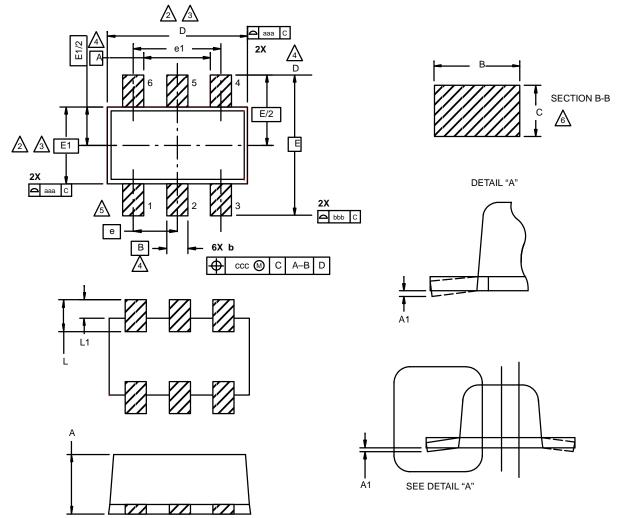


Normalized Thermal Transient Impedance, Junction-to-Ambient

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="https://www.vishay.com/ppg?70686">www.vishay.com/ppg?70686</a>.



### SC89: 6- LEADS (SOT-563F)



#### NOTES:

1. Dimensions in millimeters.



Dimension D does not include mold flash, protrusions or gate burrs. Mold flush, protrusions or gate burrs shall not exceed 0.15 mm per dimension E1 does not include interlead flash or protrusion, interlead flash or protrusion shall not exceed 0.15 mm per side.



Dimensions D and E1 are determined at the outmost extremes of the plastic body exclusive of mold flash, the bar burrs, gate burrs and interlead flash, but including any mismatch between the top and the bottom of the plastic body.



Datums A, B and D to be determined 0.10 mm from the lead tip.



Terminal numbers are shown for reference only.



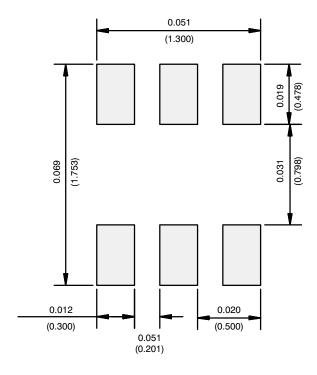
These dimensions apply to the flat section of the lead between 0.08 mm and 0.15 mm from the lead tip.

	MILLIMETERS			Tolerances Of Form And		
Dim	Min	Max	Note	Symbol	Position	
Α	0.56	0.60		aaa	0.10	
A1	0.00	0.10		bbb	0.10	
b	0.15	0.30		ccc	0.10	
С	0.10	0.18				
D	1.50	1.70	2, 3			
E	1.55	1.70				
E1	1.20 BSC		2, 3			
е	0.50 BSC					
e1	1.00 BSC					
L	0.35 BSC					
L1	0.20 BSC					

DWG: 5880



### **RECOMMENDED MINIMUM PADS FOR SC-89: 6-Lead**



Recommended Minimum Pads Dimensions in Inches/(mm)

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APPLICATION NOTE



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Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

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Revision: 02-Oct-12 Document Number: 91000