

N-Channel 30 V (D-S) MOSFET

| PRODUCT SUMMARY | | | |
|-----------------|---------------------------|-----------------|--------------|
| V_{DS} (V) | $R_{DS(on)}$ (Ω) | I_D (A) | Q_g (Typ.) |
| 30 | 0.021 at $V_{GS} = 10$ V | 12 ^a | 3.7 nC |
| | 0.033 at $V_{GS} = 4.5$ V | 6 | |

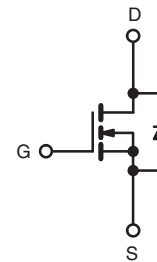
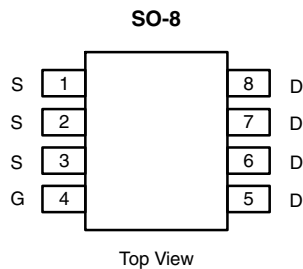
FEATURES

- TrenchFET[®] Power MOSFET
- 100 % R_g and UIS Tested
- Compliant to RoHS Directive 2002/95/EC


RoHS
COMPLIANT

APPLICATIONS

- Notebook System Power
- Low Current DC/DC


Ordering Information: Si4178DY-T1-E3 (Lead (Pb)-free)

N-Channel MOSFET

| ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted) | | | | |
|---|---------------|----------------|---------------------|------|
| Parameter | | Symbol | Limit | Unit |
| Drain-Source Voltage | | V_{DS} | 30 | V |
| Gate-Source Voltage | | V_{GS} | ± 25 | |
| Continuous Drain Current ($T_J = 150$ °C) | $T_C = 25$ °C | I_D | 12 ^a | A |
| | $T_C = 70$ °C | | 9.7 ^a | |
| | $T_A = 25$ °C | | 8.3 ^{b, c} | |
| | $T_A = 70$ °C | | 6.7 ^{b, c} | |
| Pulsed Drain Current | | I_{DM} | 40 | |
| Continuous Source-Drain Diode Current | $T_C = 25$ °C | I_S | 4.2 | |
| | $T_A = 25$ °C | | 2 ^{b, c} | |
| Single Pulse Avalanche Current | L = 0.1 mH | I_{AS} | 10 | mJ |
| Single Pulse Avalanche Energy | | E_{AS} | 5 | |
| Maximum Power Dissipation | $T_C = 25$ °C | P_D | 5 | W |
| | $T_C = 70$ °C | | 3.2 | |
| | $T_A = 25$ °C | | 2.4 ^{b, c} | |
| | $T_A = 70$ °C | | 1.5 ^{b, c} | |
| Operating Junction and Storage Temperature Range | | T_J, T_{stg} | - 55 to 150 | °C |

| THERMAL RESISTANCE RATINGS | | | | | |
|---|---------------|------------|---------|---------|------|
| Parameter | | Symbol | Typical | Maximum | Unit |
| Maximum Junction-to-Ambient ^{b, d} | $t \leq 10$ s | R_{thJA} | 42 | 53 | °C/W |
| Maximum Junction-to-Foot (Drain) | Steady State | R_{thJF} | 19 | 25 | |

Notes:

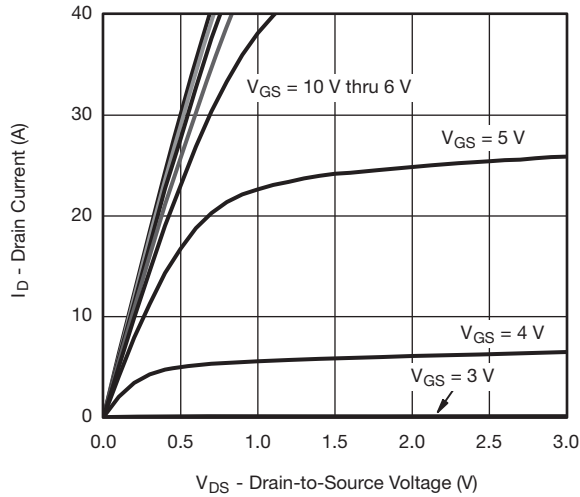
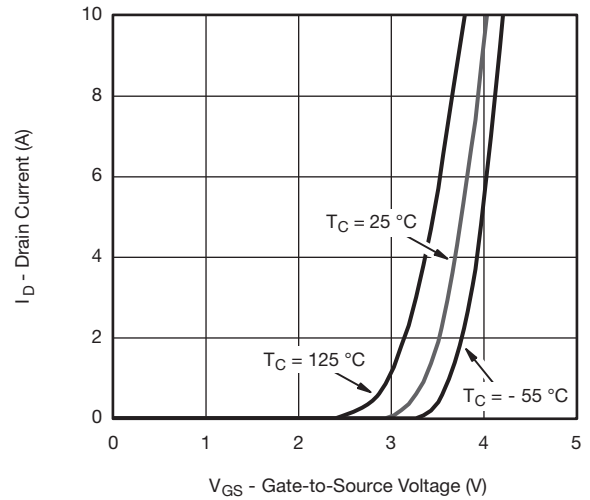
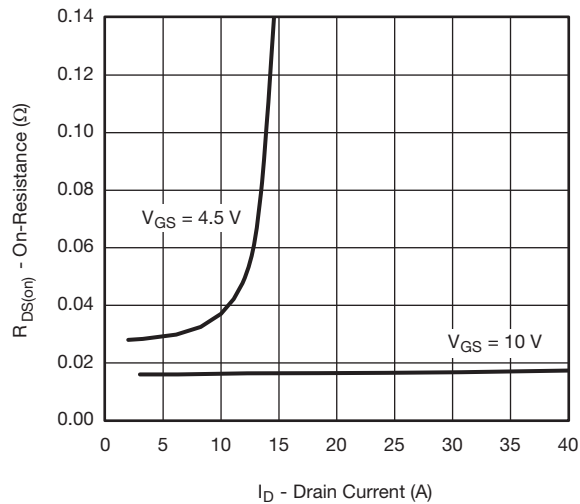
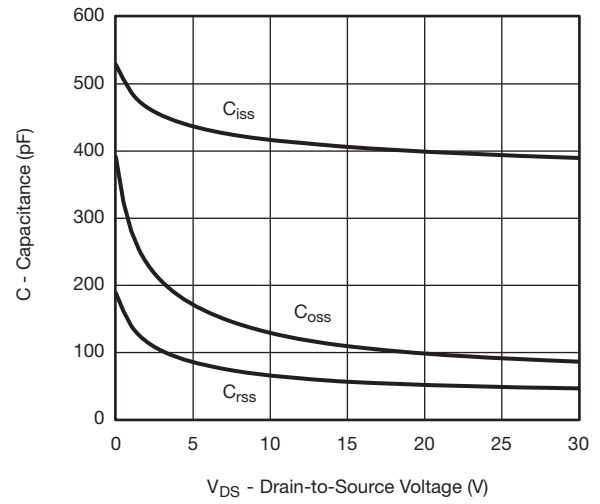
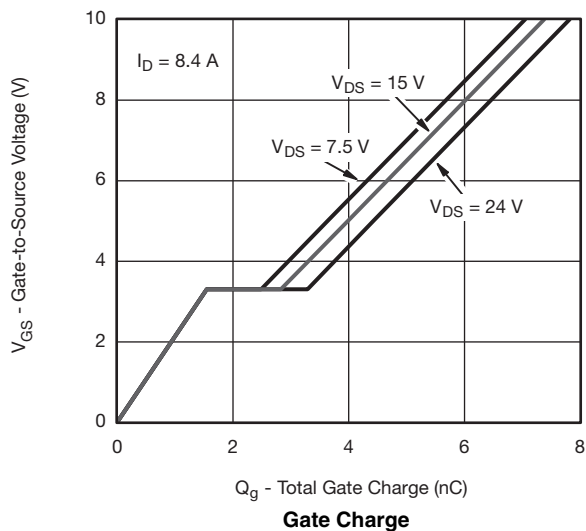
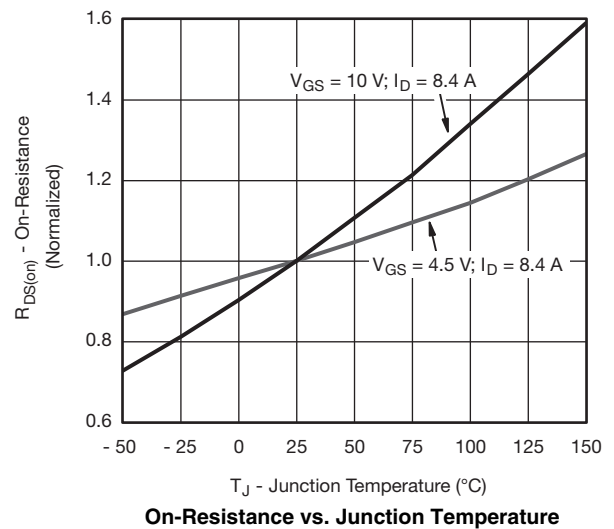
- Package limited.
- Surface mounted on 1" x 1" FR4 board.
- $t = 10$ s.
- Maximum under steady state conditions is 85 °C/W.

| SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted) | | | | | | |
|---|-------------------------|--|------|-------|-----------|----------------------|
| Parameter | Symbol | Test Conditions | Min. | Typ. | Max. | Unit |
| Static | | | | | | |
| Drain-Source Breakdown Voltage | V_{DS} | $V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$ | 30 | | | V |
| V_{DS} Temperature Coefficient | $\Delta V_{DS}/T_J$ | $I_D = 250\text{ }\mu\text{A}$ | | 25 | | mV/ $^\circ\text{C}$ |
| $V_{GS(th)}$ Temperature Coefficient | $\Delta V_{GS(th)}/T_J$ | | | -6 | | |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$ | 1.4 | | 2.8 | V |
| Gate-Source Leakage | I_{GSS} | $V_{DS} = 0\text{ V}, V_{GS} = \pm 25\text{ V}$ | | | ± 100 | nA |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$ | | | 1 | μA |
| | | $V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$ | | | 10 | |
| On-State Drain Current ^a | $I_{D(on)}$ | $V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$ | 20 | | | A |
| Drain-Source On-State Resistance ^a | $R_{DS(on)}$ | $V_{GS} = 10\text{ V}, I_D = 8.4\text{ A}$ | | 0.017 | 0.021 | Ω |
| | | $V_{GS} = 4.5\text{ V}, I_D = 2\text{ A}$ | | 0.027 | 0.033 | |
| Forward Transconductance ^a | g_{fs} | $V_{DS} = 15\text{ V}, I_D = 8.4\text{ A}$ | | 22 | | S |
| Dynamic^b | | | | | | |
| Input Capacitance | C_{iss} | $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$ | | 405 | | pF |
| Output Capacitance | C_{oss} | | | 110 | | |
| Reverse Transfer Capacitance | C_{rss} | | | 56 | | |
| Total Gate Charge | Q_g | $V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 8.4\text{ A}$ | | 7.5 | 12 | nC |
| | | | | 3.7 | 5.6 | |
| Gate-Source Charge | Q_{gs} | $V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 8.4\text{ A}$ | | 1.6 | | |
| Gate-Drain Charge | Q_{gd} | | | 1.3 | | |
| Gate Resistance | R_g | $f = 1\text{ MHz}$ | 0.5 | 2.6 | 5.2 | Ω |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD} = 15\text{ V}, R_L = 2.2\text{ }\Omega$ $I_D \cong 6.7\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$ | | 20 | 30 | ns |
| Rise Time | t_r | | | 15 | 25 | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | 11 | 20 | |
| Fall Time | t_f | | | 10 | 15 | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD} = 15\text{ V}, R_L = 2.2\text{ }\Omega$ $I_D \cong 6.7\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$ | | 7 | 15 | |
| Rise Time | t_r | | | 10 | 15 | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | 12 | 20 | |
| Fall Time | t_f | | | 10 | 15 | |
| Drain-Source Body Diode Characteristics | | | | | | |
| Continuous Source-Drain Diode Current | I_S | $T_C = 25\text{ }^\circ\text{C}$ | | | 4.2 | A |
| Pulse Diode Forward Current | I_{SM} | | | | 40 | |
| Body Diode Voltage | V_{SD} | $I_S = 6.7\text{ A}, V_{GS} = 0\text{ V}$ | | 0.85 | 1.2 | V |
| Body Diode Reverse Recovery Time | t_{rr} | $I_F = 6.7\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$ | | 15 | 30 | ns |
| Body Diode Reverse Recovery Charge | Q_{rr} | | | 8 | 16 | nC |
| Reverse Recovery Fall Time | t_a | | | 8.5 | | ns |
| Reverse Recovery Rise Time | t_b | | | 6.5 | | |

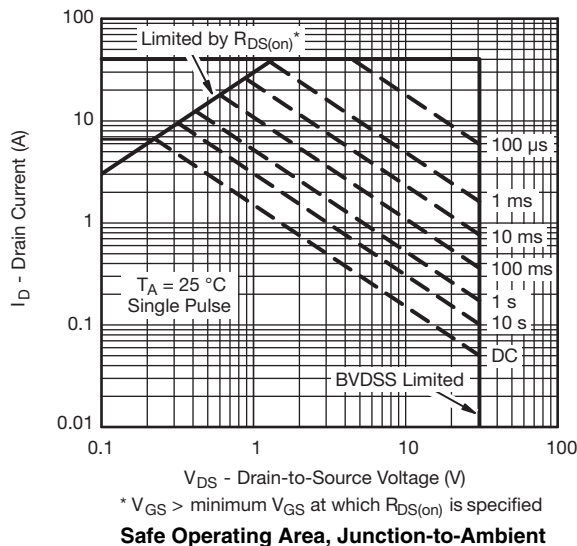
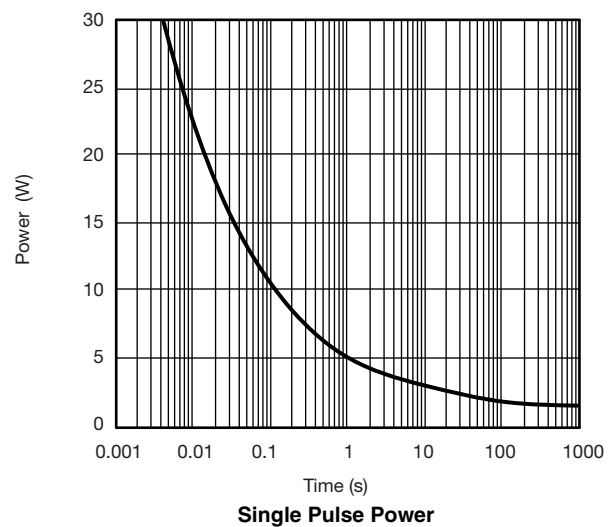
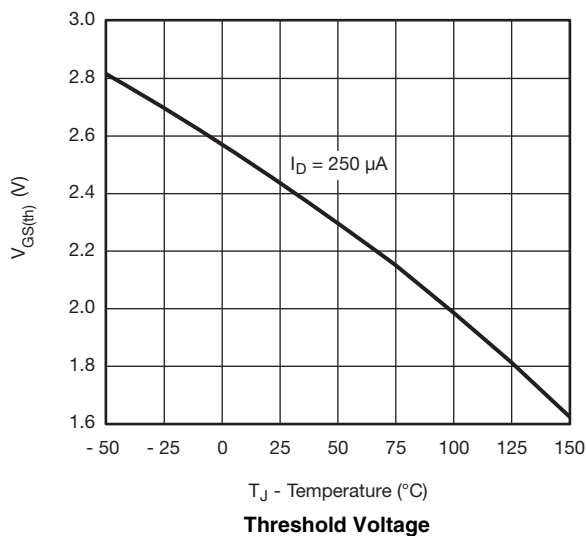
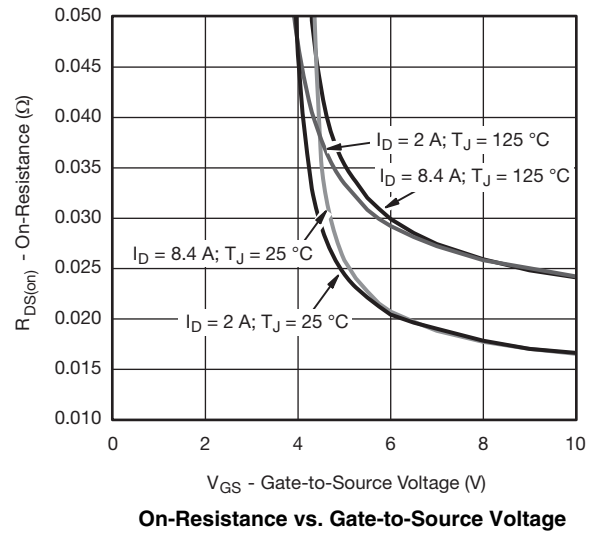
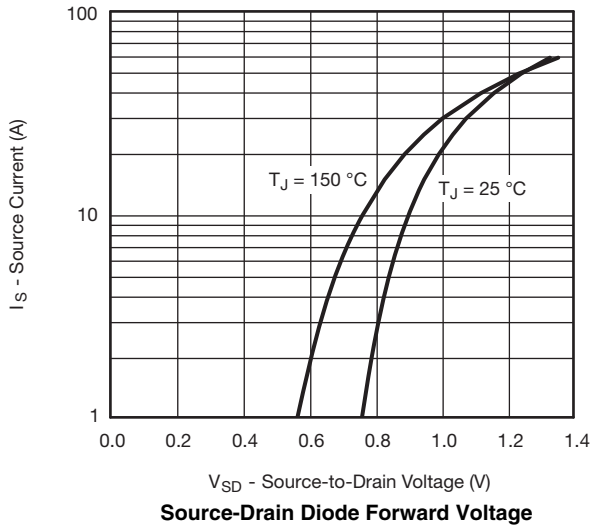
Notes:

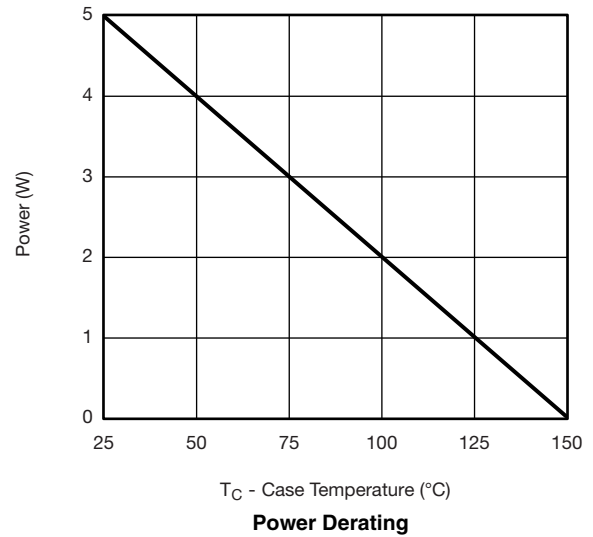
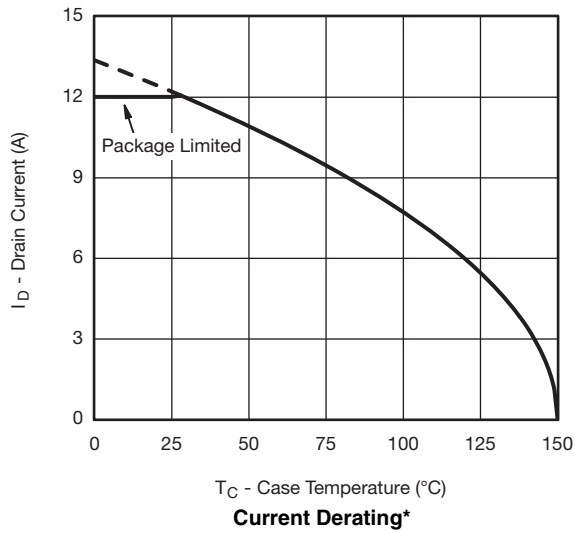
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current

Capacitance

Gate Charge

On-Resistance vs. Junction Temperature

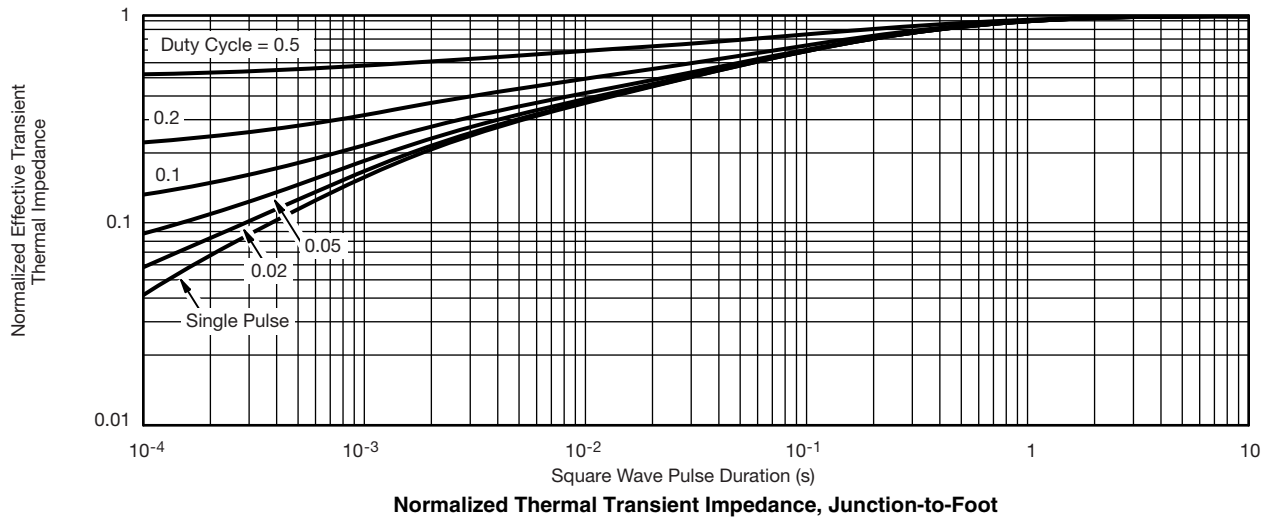
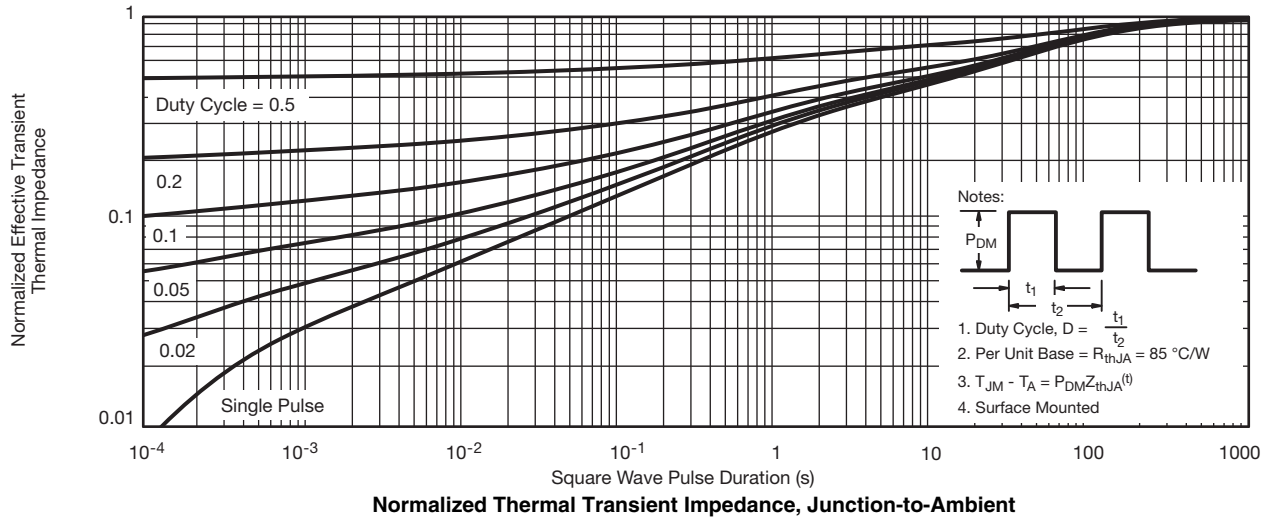
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



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* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations.



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