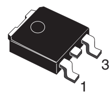
STD9NM50N

N-channel 500 V, 0.73 Ω, 5 A MDmesh™II Power MOSFET in DPAK

Features

Order code	V_{DSS}@T_{JMAX}	$R_{DS(on)}$max.	I_D
STD9NM50N	550 V	< 0.79 Ω	5 A

- 100% avalanche tested
- Low input capacitances and gate charge
- Low gate input resistance



DPAK

Applications

- Switching applications
- Automotive

Description

These N-channel Power MOSFETs are developed using STMicroelectronics' revolutionary MDmesh™ technology, which associates the multiple drain process with the company's PowerMESH™ horizontal layout. These devices offer extremely low on-resistance, high dv/dt and excellent avalanche characteristics. Utilizing ST's proprietary strip technique, these Power MOSFETs boast an overall dynamic performance which is superior to similar products on the market.

Figure 1. Internal schematic diagram

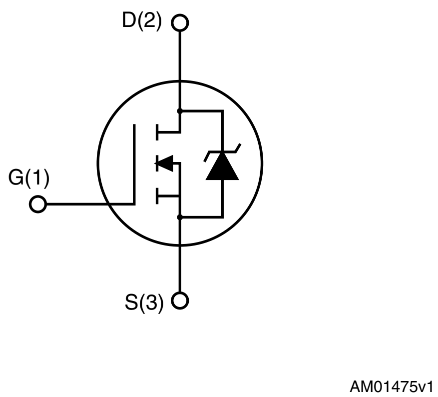


Table 1. Device summary

Order code	Marking	Packages	Packaging
STD9NM50N	9NM50N	DPAK	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at T_C = 25 °C	5	A
I_D	Drain current (continuous) at T_C = 100 °C	3	A
I_{DM} (1)	Drain current (pulsed)	20	A
P_{TOT}	Total dissipation at T_C = 25 °C	45	W
dv/dt (2)	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature	- 55 to 150	°C
T_j	Max. operating junction temperature	150	°C

1. Pulse width limited by safe operating area
2. $I_{SD} \leq 5$ A, di/dt $\leq$ 400 A/µs, $V_{Peak} < V_{(BR)DSS}$, V_{DS}=80% $V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	2.78	°C/W
$R_{thj-pcb}$	Thermal resistance junction-pcb max	50	°C/W

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	2	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25°C, $I_D = I_{AR}$, V_{DD} = 50 V)	140	mJ

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage (V_{GS} = 0)	I_D = 1 mA	500			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 500 V V_{DS} = 500 V, T_C=125 °C			1 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 25 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 2.5 A		0.73	0.79	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0	-	364 33 1.2	-	pF pF pF
$C_{oss(eq)}$ (1)	Equivalent output capacitance time related	V_{DS} = 0 to 50 V, V_{GS} = 0	-	147.5	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	5.4	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 400 V, I_D = 5 A, V_{GS} = 10 V (see *Figure 13*)	-	14 3 7	-	nC nC nC

1. Coss eq. is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off-delay time Fall time	V_{DD} = 250 V, I_D = 5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 12*)	-	7 4.4 25 8.8	-	ns ns ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)		-		5 20	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 5 A, V_{GS} = 0	-		1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 5 A, di/dt = 100 A/µs V_{DD} = 60 V (see *Figure 17*)	-	187 1.3 14		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 5 A, di/dt = 100 A/µs V_{DD} = 60 V, T_j = 150 °C (see *Figure 17*)	-	224 1.5 13		ns µC A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

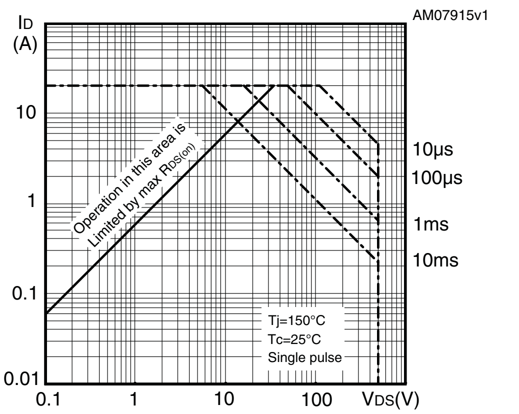


Figure 3. Thermal impedance

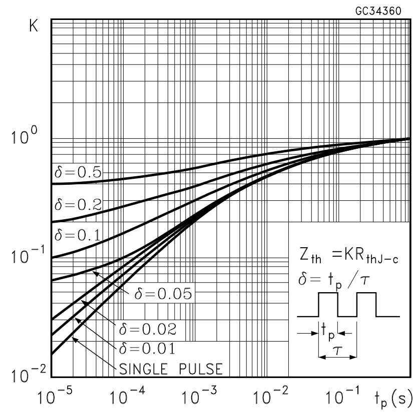


Figure 4. Output characteristics

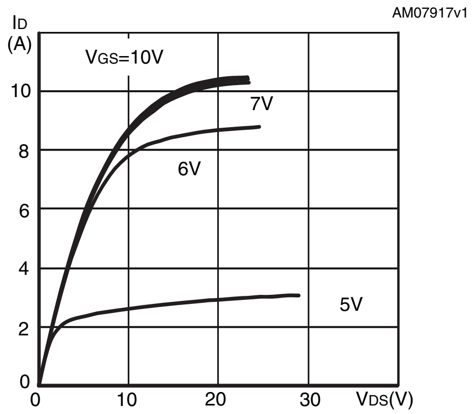


Figure 5. Transfer characteristics

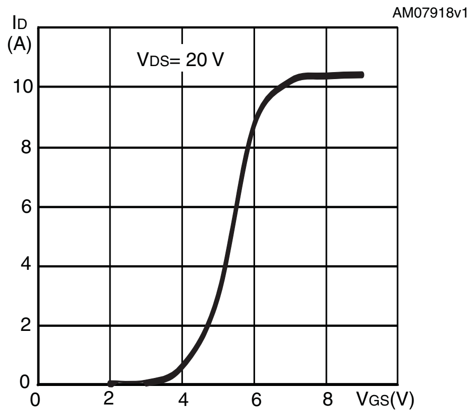


Figure 6. Static drain-source on resistance

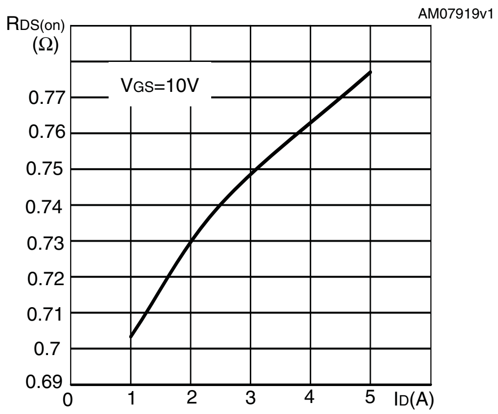


Figure 7. Gate charge vs gate-source voltage

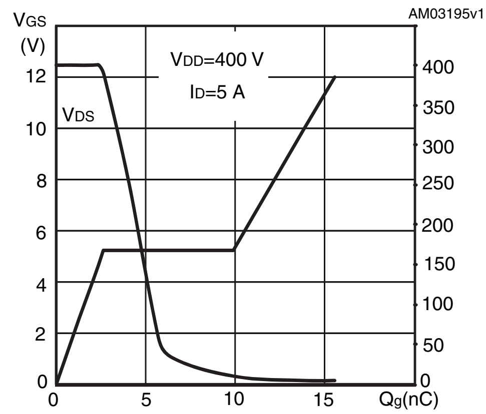


Figure 8. Capacitance variations

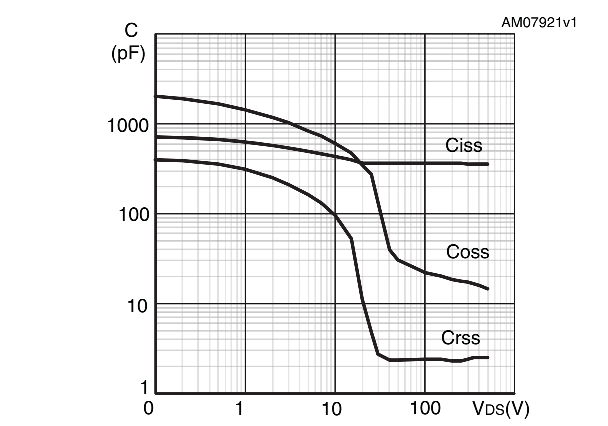


Figure 9. Normalized BVdss vs temperature

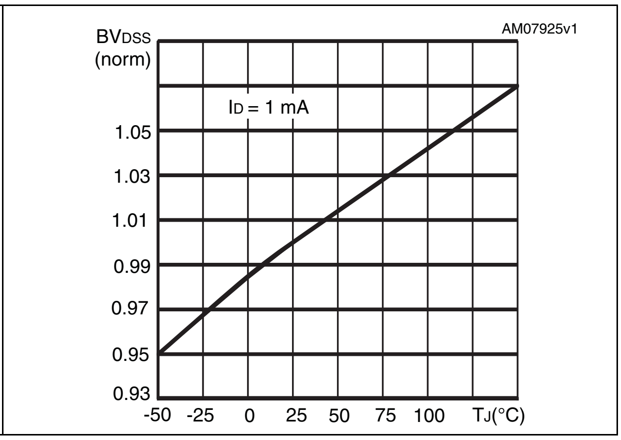


Figure 10. Normalized gate threshold voltage vs temperature

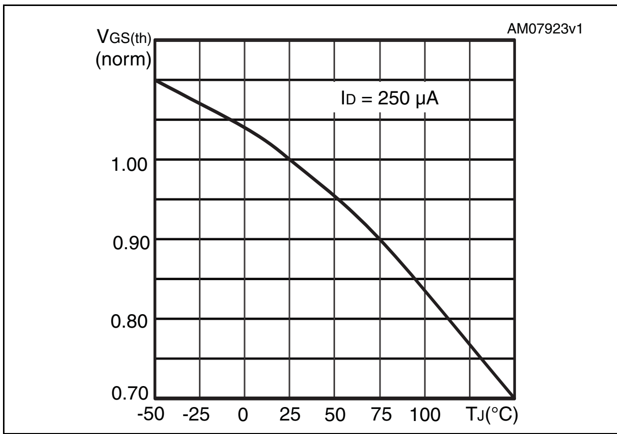
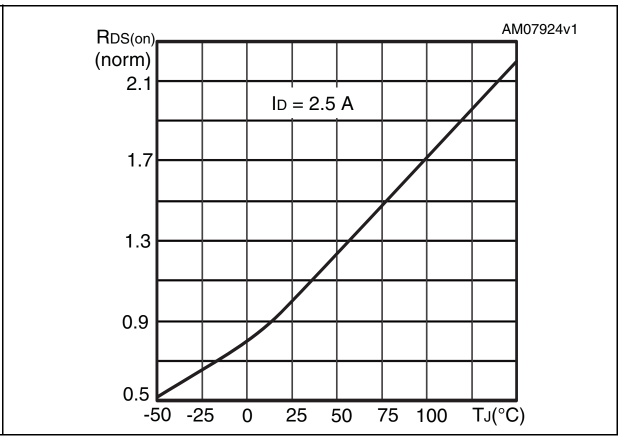


Figure 11. Normalized on resistance vs temperature



3 Test circuits

Figure 12. Switching times test circuit for resistive load

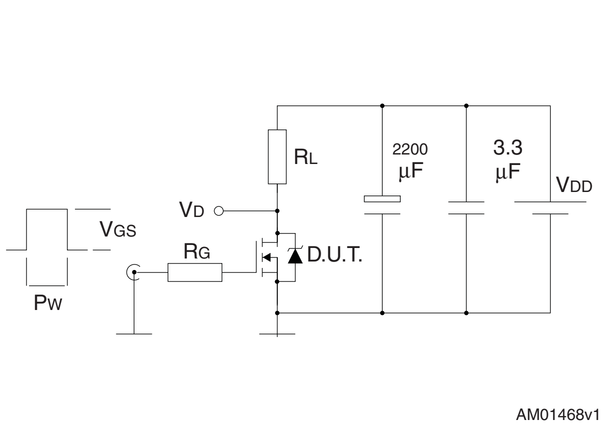


Figure 13. Gate charge test circuit

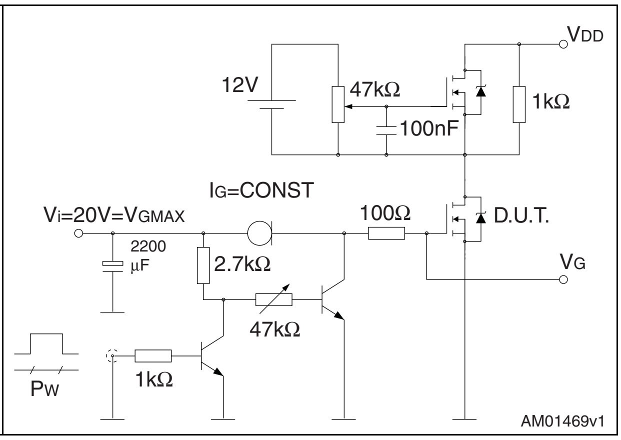


Figure 14. Test circuit for inductive load switching and diode recovery times

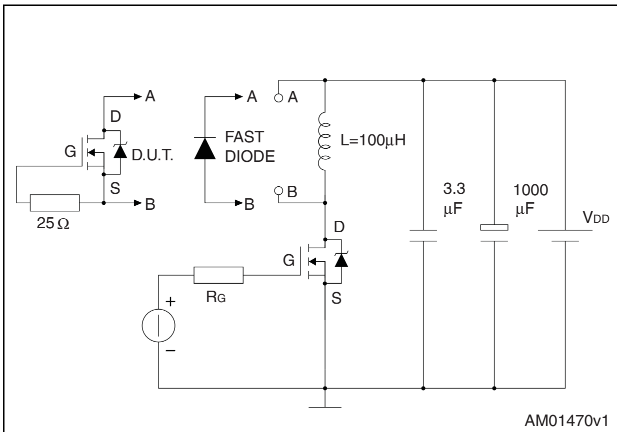


Figure 15. Unclamped inductive load test circuit

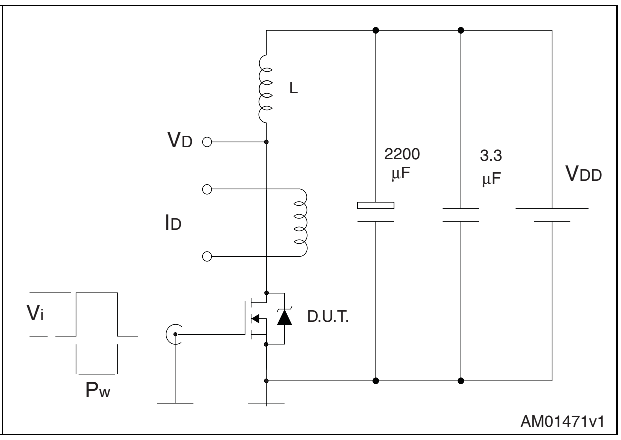


Figure 16. Unclamped inductive waveform

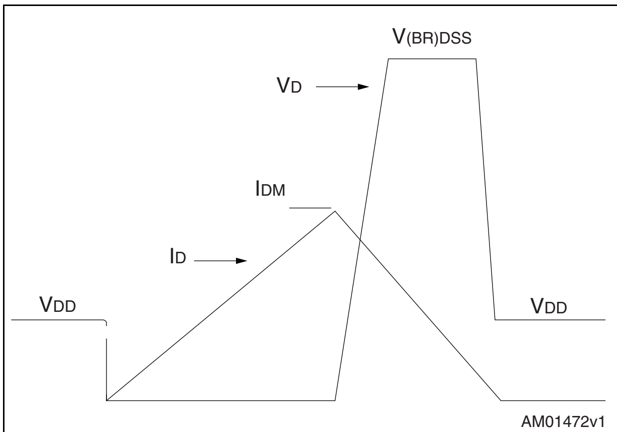
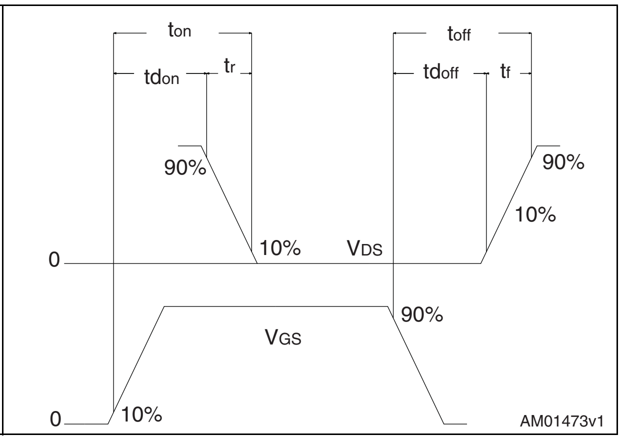


Figure 17. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 9. DPAK (TO-252) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		1.50
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°

Figure 18. DPAK (TO-252) drawing

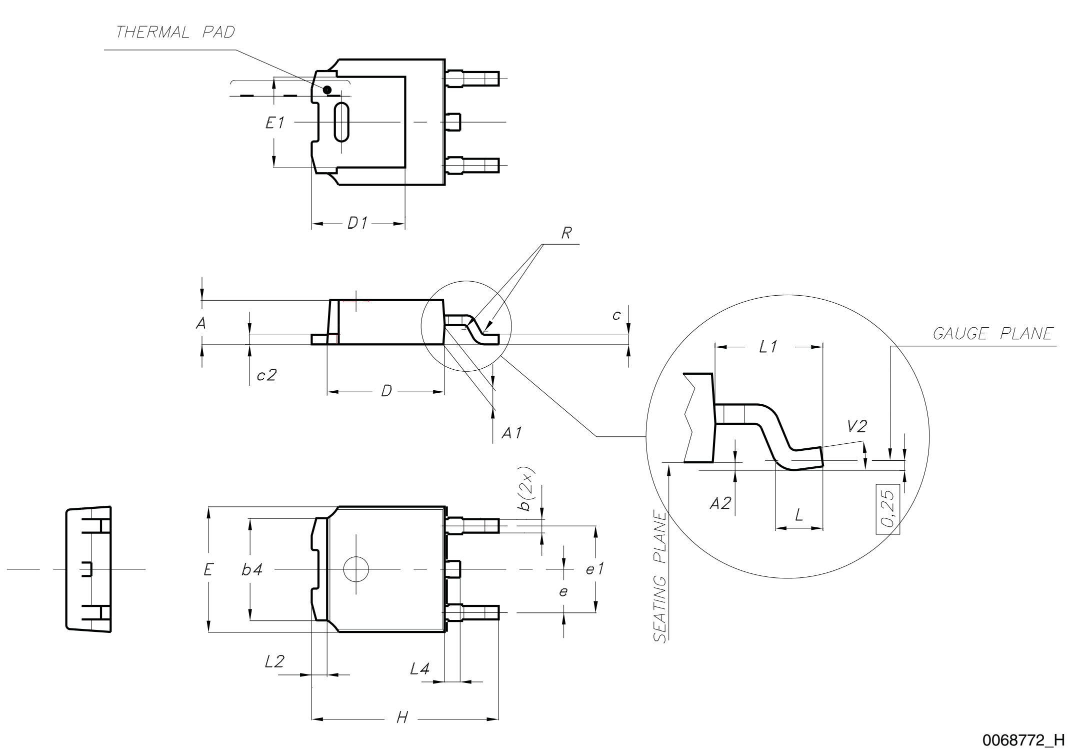
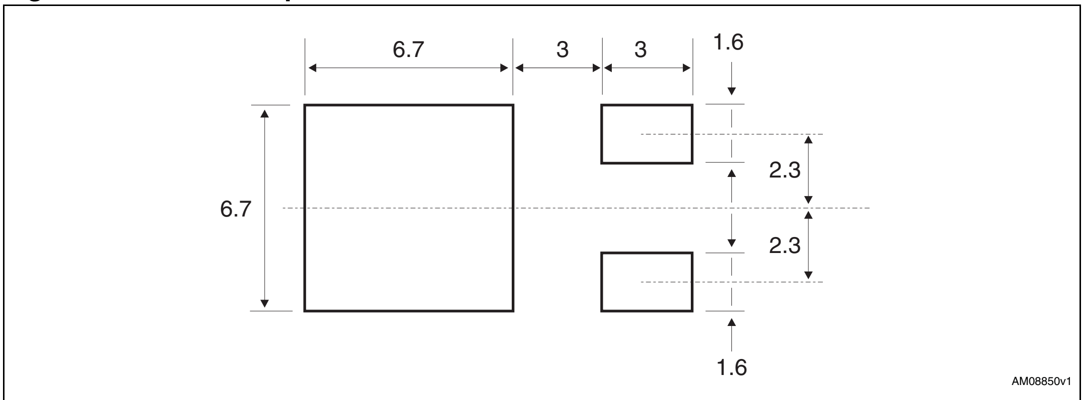


Figure 19. DPAK footprint[(a)]



a. All dimension are in millimeters

5 Packaging mechanical data

Table 10. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Figure 20. Tape for DPAK (TO-252)

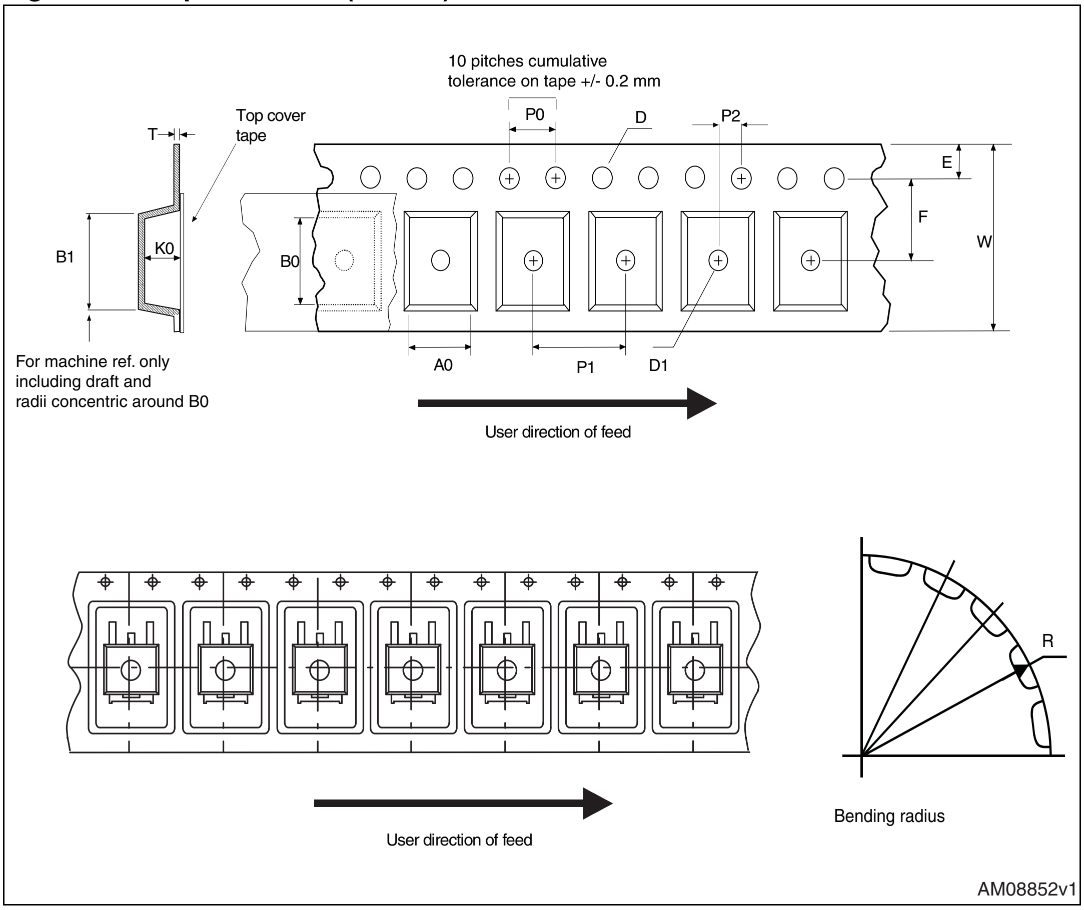
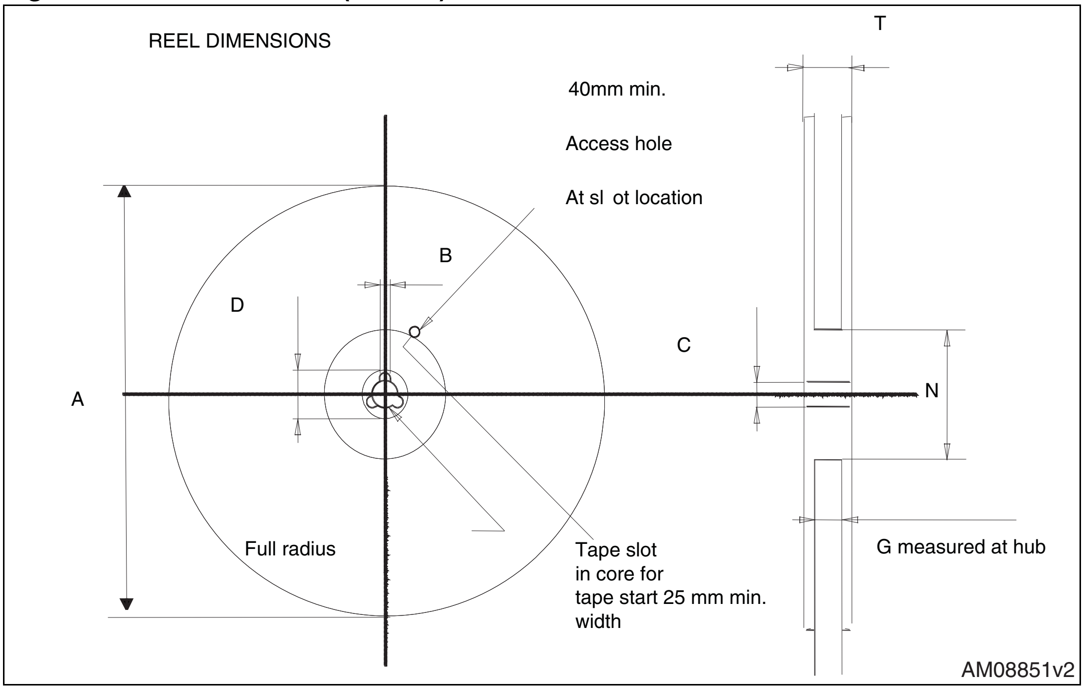


Figure 21. Reel for DPAK (TO-252)



6 Revision history

Table 11. Document revision history

Date	Revision	Changes
21-Sep-2011	1	First release.