



STF13NK50Z STP13NK50Z, STW13NK50Z

N-channel 500 V, 0.40 Ω , 11 A TO-220, TO-220FP, TO-247
Zener-protected SuperMESH™ Power MOSFET

Features

Type	V _{DSS}	R _{DS(on) max}	I _D	P _w
STF13NK50Z	500 V	<0.48 Ω	11 A	30 W
STP13NK50Z	500 V	<0.48 Ω	11 A	140 W
STW13NK50Z	500 V	<0.48 Ω	11 A	140 W

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeatability

Applications

- Switching application

Description

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs.

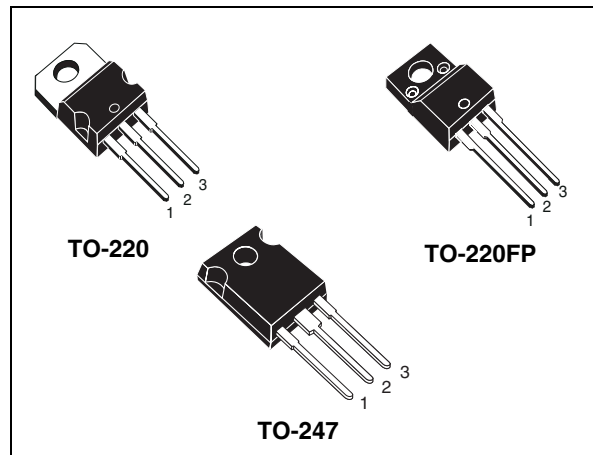


Figure 1. Internal schematic diagram

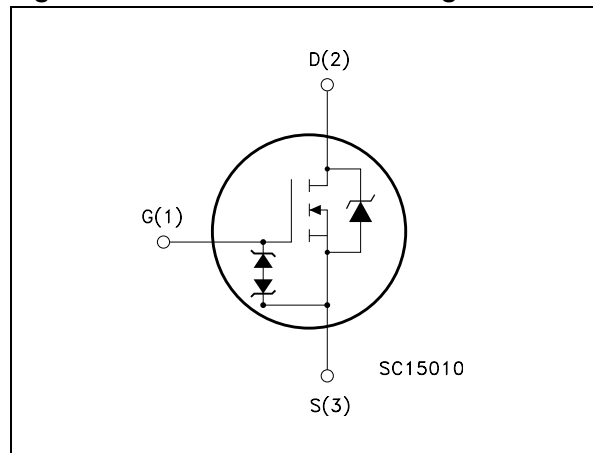


Table 1. Device summary

Order code	Marking	Package	Packaging
STF13NK50Z	F13NK50Z	TO-220FP	Tube
STP13NK50Z	P13NK50Z	TO-220	Tube
STW13NK50Z	W13NK50Z	TO-247	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220, TO-247	TO-220FP	
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	500		V
V_{GS}	Gate-source voltage	± 30		V
I_D	Drain current (continuous) at $T_C = 25\text{ °C}$	11	11 ⁽¹⁾	A
I_D	Drain current (continuous) at $T_C = 100\text{ °C}$	6.93	6.93 ⁽¹⁾	A
$I_{DM}^{(2)}$	Drain current (pulsed)	44	44 ⁽¹⁾	A
P_{TOT}	Total dissipation at $T_C = 25\text{ °C}$	140	30	W
	Derating factor	1.12	0.24	W/°C
$dv/dt^{(3)}$	Peak diode recovery voltage slope	4.5		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sin ($t=1\text{ s}; T_C=25\text{ °C}$)		2500	V
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150		°C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 11\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} \leq 80\% V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value			Unit
		TO-220	TO-247	TO-220FP	
$R_{thj-case}$	Thermal resistance junction-case max	0.89		4.17	°C/W
R_{thj-a}	Thermal resistance junction-ambient max	62.5	50	62.5	°C/W
T_I	Maximum lead temperature for soldering purpose	300			°C

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_J \text{ Max}$)	11	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ °C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	240	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 1 mA, V _{GS} = 0	500			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = Max rating, V _{DS} = Max rating, T _C = 125 °C			1 50	μA μA
I _{GSS}	Gate body leakage current (V _{DS} = 0)	V _{GS} = ± 20 V			±10	μA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 100 μA	3	3.75	4.5	V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10 V, I _D = 6.5 A		0.4	0.48	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g _{fs} ⁽¹⁾	Forward transconductance	V _{DS} = 15 V, I _D = 6.5 A		8.5		S
C _{iss} C _{oss} C _{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V _{DS} = 25 V, f = 1 MHz, V _{GS} = 0		1600 200 45		pF pF pF
C _{oss eq} ⁽²⁾	Equivalent output capacitance	V _{GS} = 0, V _{DS} = 0 V to 400 V		50		pF
Q _g Q _{gs} Q _{gd}	Total gate charge Gate-source charge Gate-drain charge	V _{DD} = 400 V, I _D = 13 A V _{GS} = 10 V <i>Figure 20</i>		47 9 28		nC nC nC
R _g	Intrinsic gate resistance	f = 1 MHz open drain		2.3		Ω

1. Pulsed: pulse duration = 300 μs, duty cycle 1.5%

2. C_{oss eq} is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)} t _r	Turn-on delay time Rise time	V _{DD} = 400 V, I _D = 6.5 A, R _G = 4.7 Ω, V _{GS} = 10 V <i>Figure 19</i>		18 23		ns ns
t _{d(off)} t _f	Turn-off delay time Fall time			61 24		ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				11	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				44	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=11\text{ A}$, $V_{GS}=0$			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=6.5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD}=40\text{ V}$, $T_j=25\text{ }^\circ\text{C}$ <i>Figure 21</i>		380 3.4 18		ns μC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=6.5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD}=40\text{ V}$, $T_j=150\text{ }^\circ\text{C}$ <i>Figure 21</i>		425 3.9 18.5		ns μC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

Table 9. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$BV_{GSO}^{(1)}$	Gate-source breakdown voltage	$I_{GS}=\pm 1\text{ mA}$ (open drain)	30			V

1. The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220

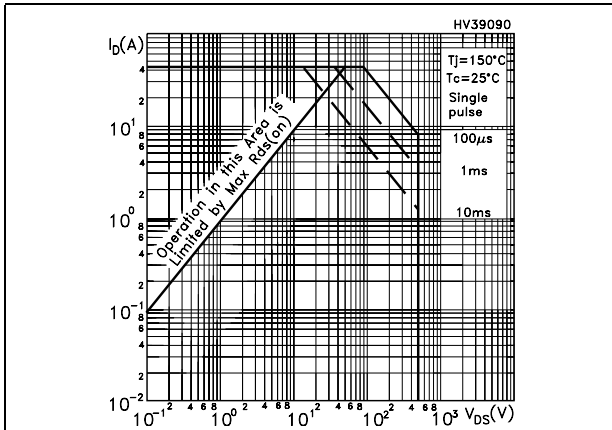


Figure 3. Thermal impedance for TO-220

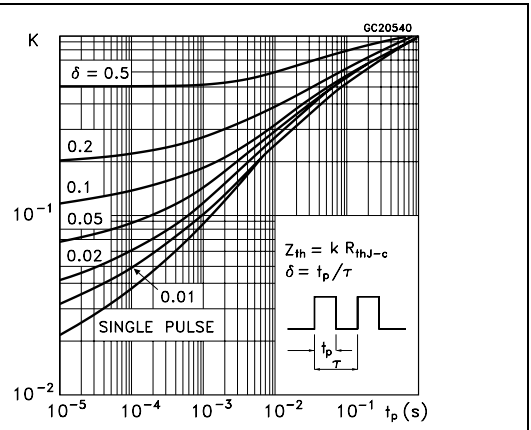


Figure 4. Safe operating area for TO-220FP

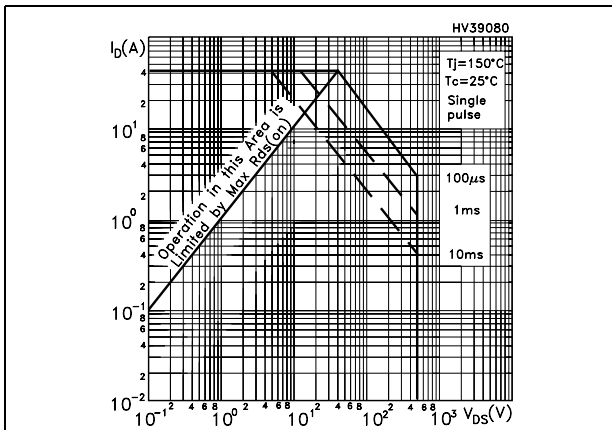


Figure 5. Thermal impedance for TO-220FP

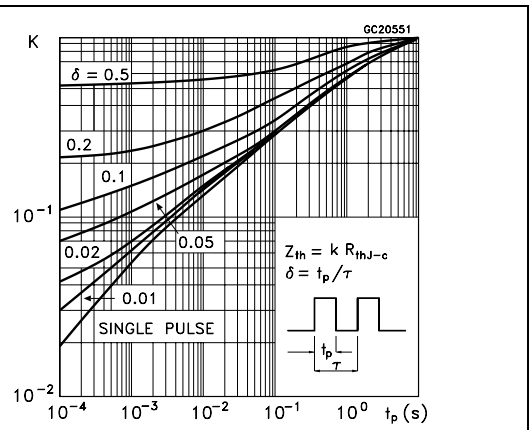


Figure 6. Safe operating area for TO-247

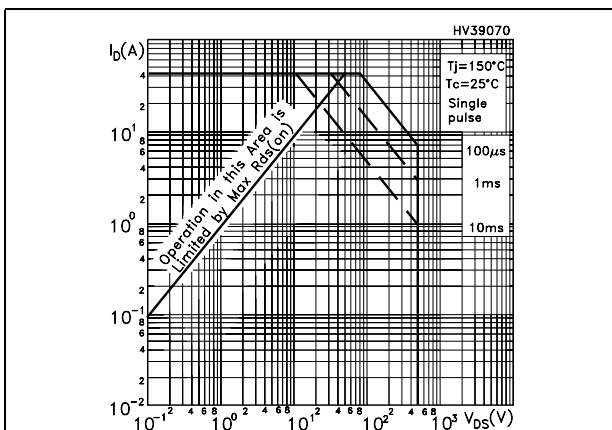


Figure 7. Thermal impedance for TO-247

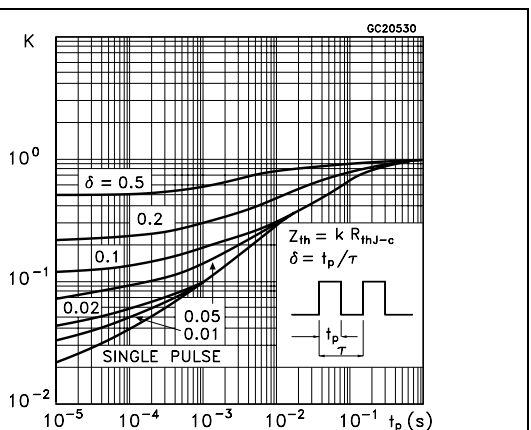


Figure 8. Output characteristics

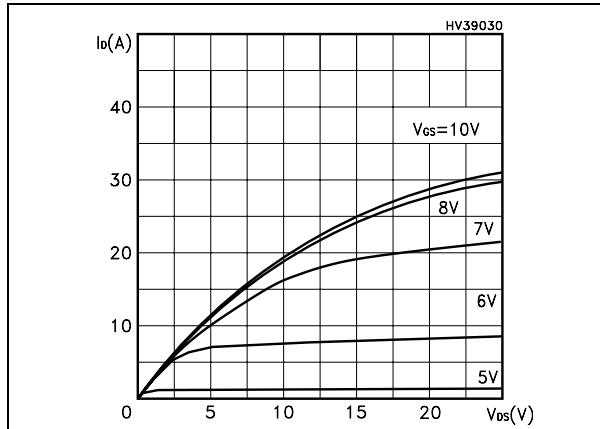


Figure 9. Transfer characteristics

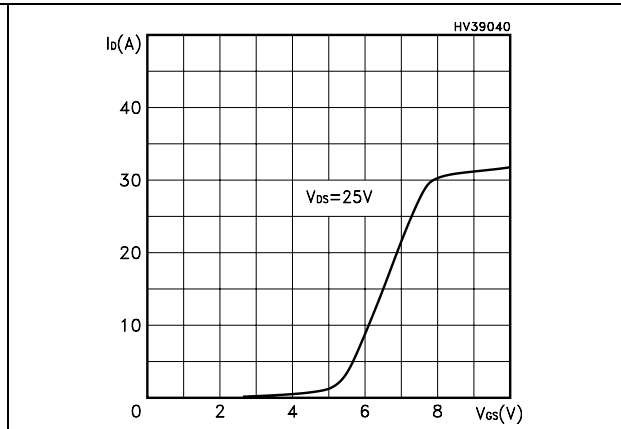


Figure 10. Transconductance

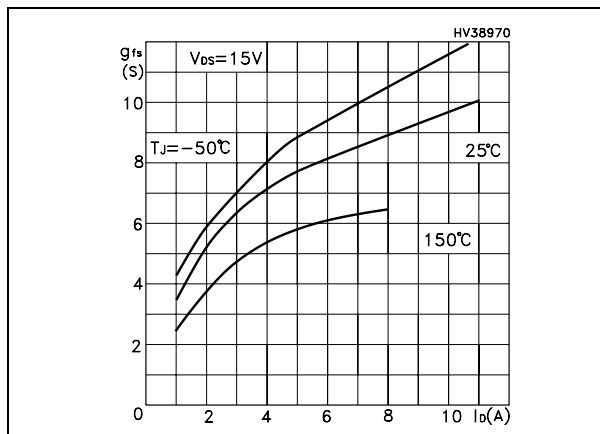


Figure 11. Static drain-source on resistance

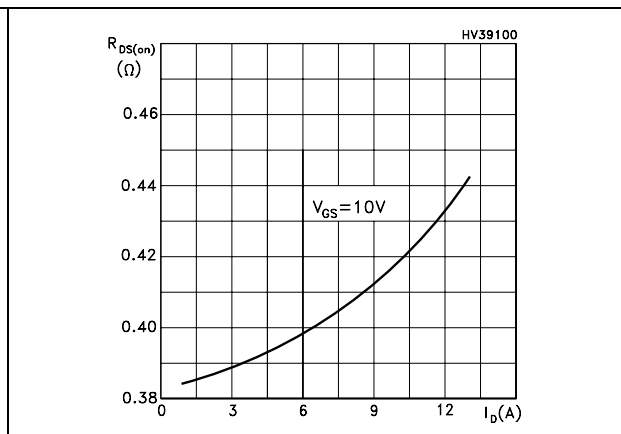


Figure 12. Gate charge vs gate-source voltage

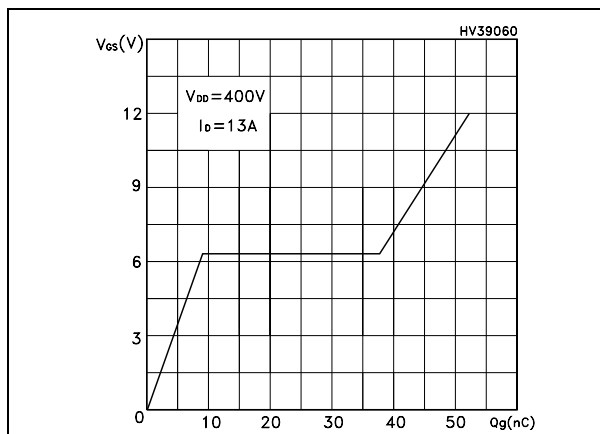


Figure 13. Capacitance variations

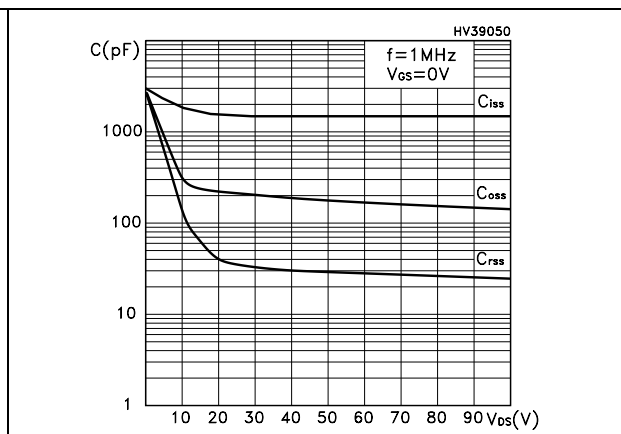


Figure 14. Normalized gate threshold voltage vs temperature

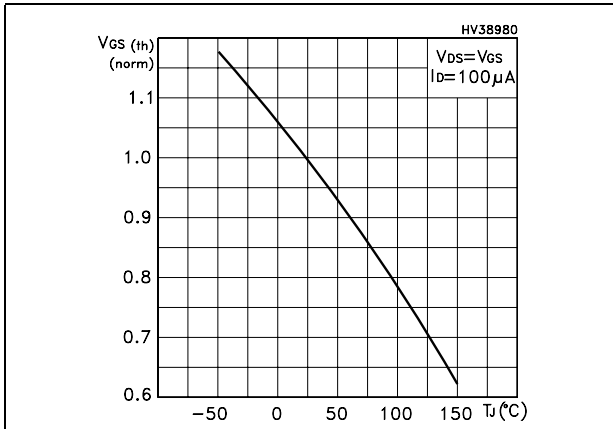


Figure 15. Normalized on resistance vs temperature

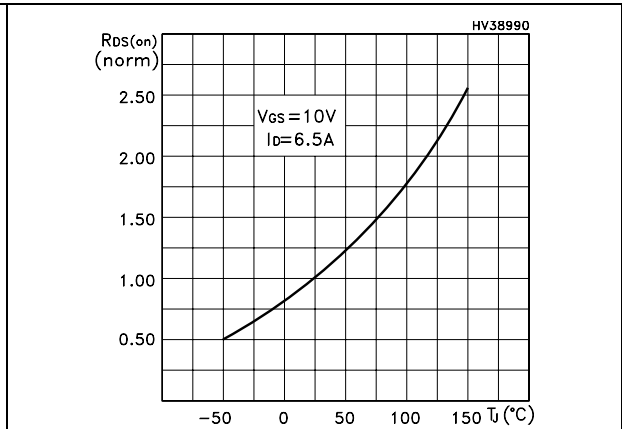


Figure 16. Source-drain diode forward characteristics

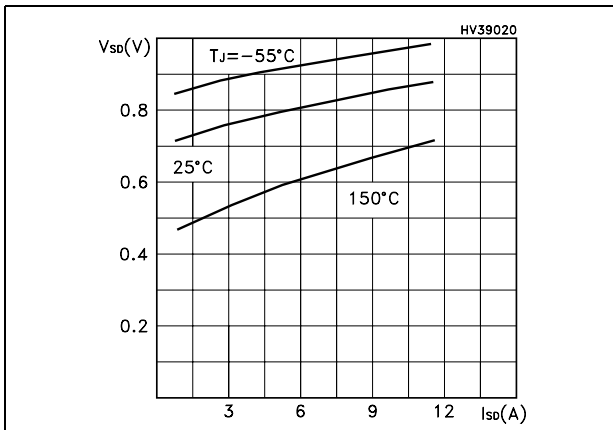


Figure 17. Normalized BV_{DSS} vs temperature

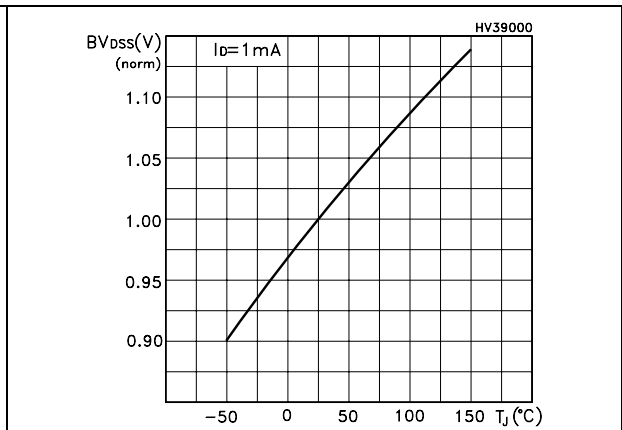
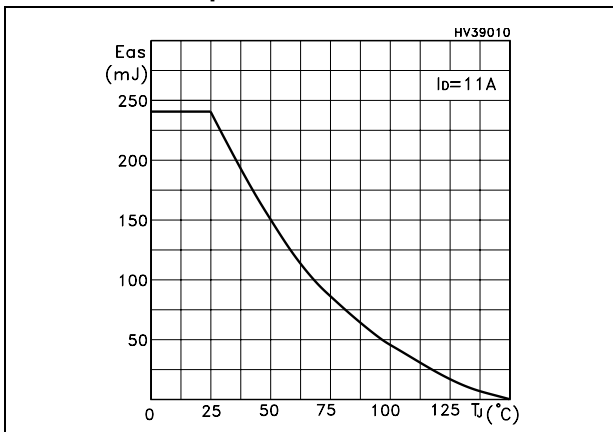


Figure 18. Maximum avalanche energy vs temperature



3 Test circuit

Figure 19. Switching times test circuit for resistive load

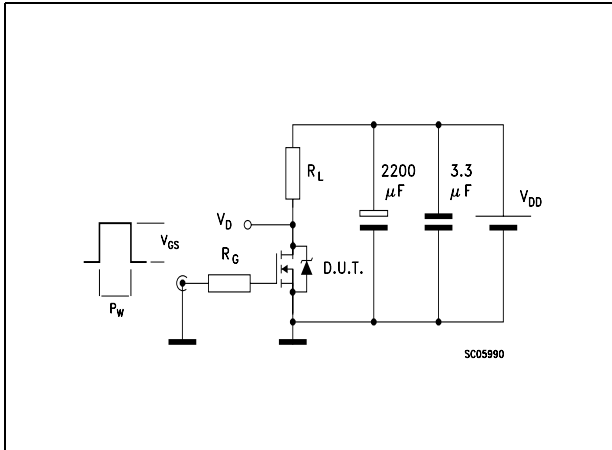


Figure 20. Gate charge test circuit

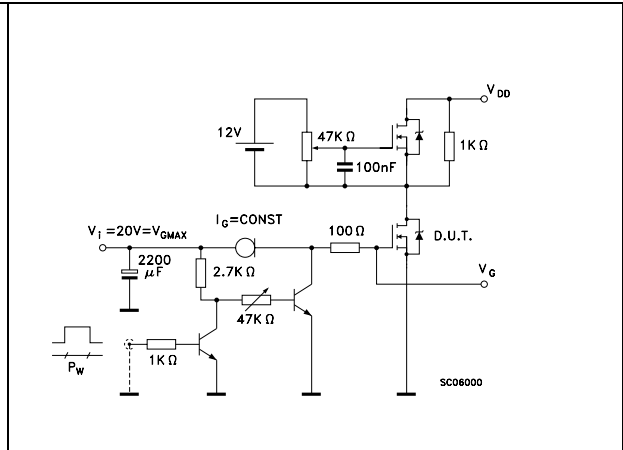


Figure 21. Test circuit for inductive load switching and diode recovery times

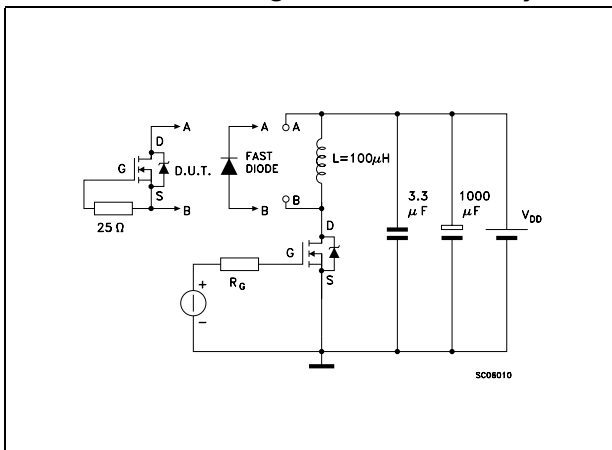


Figure 22. Unclamped inductive load test circuit

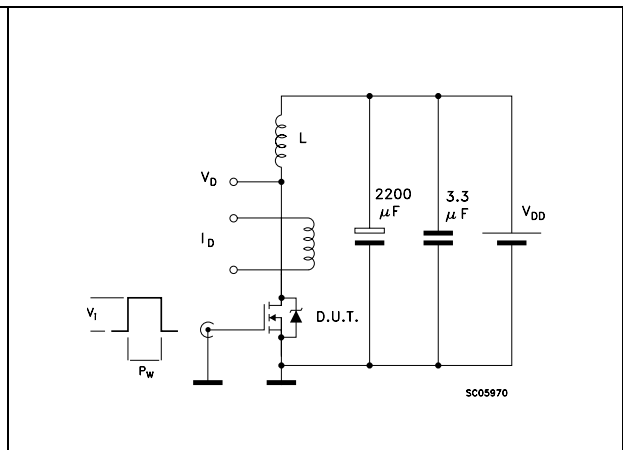


Figure 23. Unclamped inductive waveform

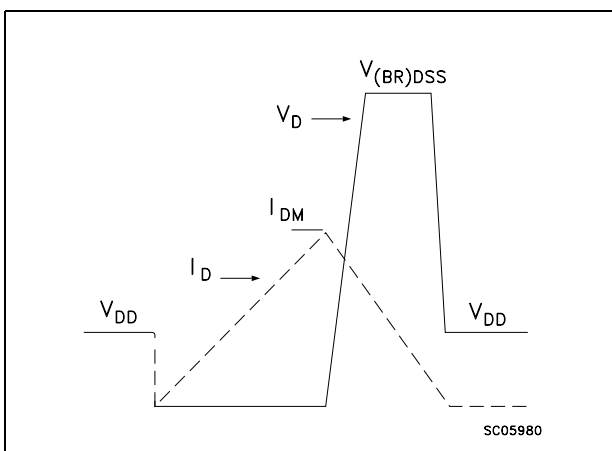
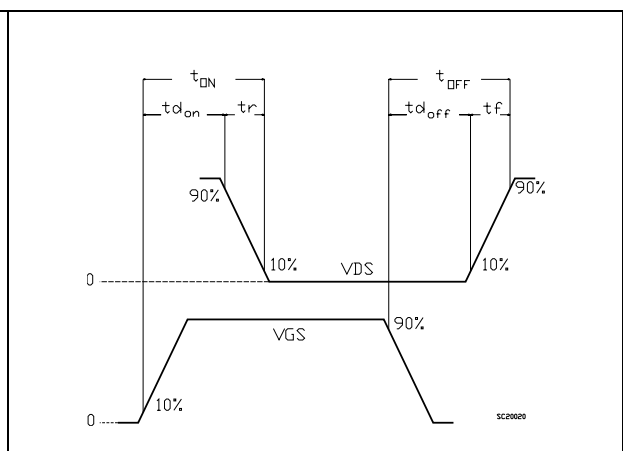


Figure 24. Switching time waveform

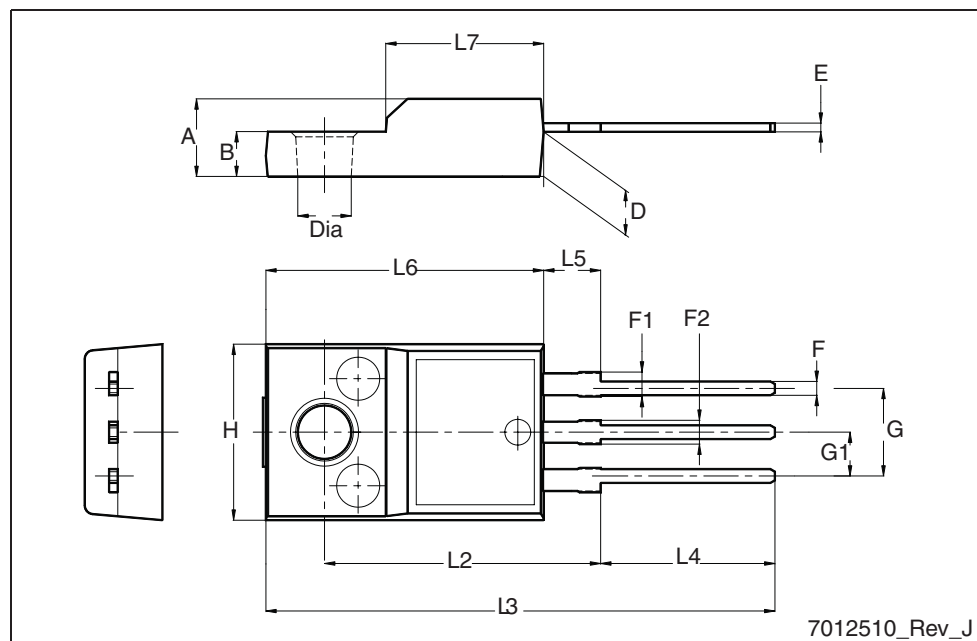


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

TO-220FP mechanical data

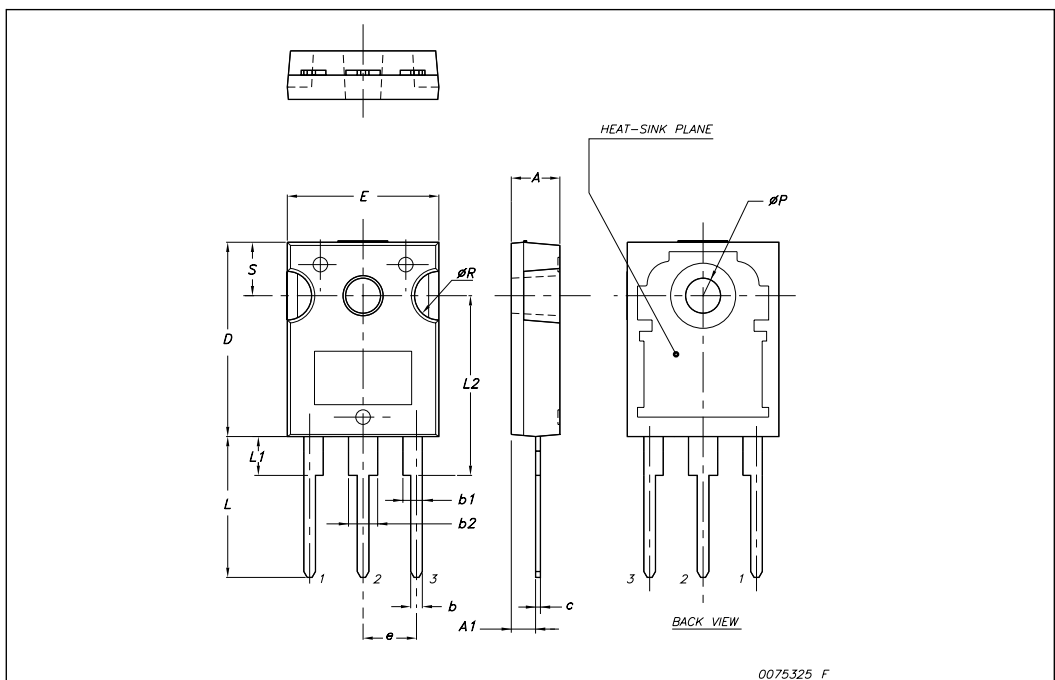
Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.5
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2



7012510_Rev_J

TO-247 Mechanical data

Dim.	mm.		
	Min.	Typ	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e		5.45	
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
øP	3.55		3.65
øR	4.50		5.50
S		5.50	



5 Revision history

Table 10. Revision history

Date	Revision	Changes
07-Aug-2007	1	First version
19-Mar-2009	2	Update I_D value test condition in Table 6 .

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