



STF6N65K3

N-channel 650 V, 1.1 Ω , 5.4 A, TO-220FP
SuperMESH3™ Power MOSFET

Preliminary data

Features

| Order code | V _{DSS} | R _{DS(on)} max | I _D | P _w |
|------------|------------------|-------------------------|----------------------|----------------|
| STF6N65K3 | 650 V | < 1.3 Ω | 5.4 A ⁽¹⁾ | 30 W |

1. Limited by package

- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitances
- Improved diode reverse recovery characteristics
- Zener-protected

Application

Switching applications

Description

This device is made using the SuperMESH3™ Power MOSFET technology that is obtained via improvements applied to STMicroelectronics' SuperMESH™ technology combined with a new optimized vertical structure. The resulting product has an extremely low on resistance, superior dynamic performance and high avalanche capability, making it especially suitable for the most demanding applications.

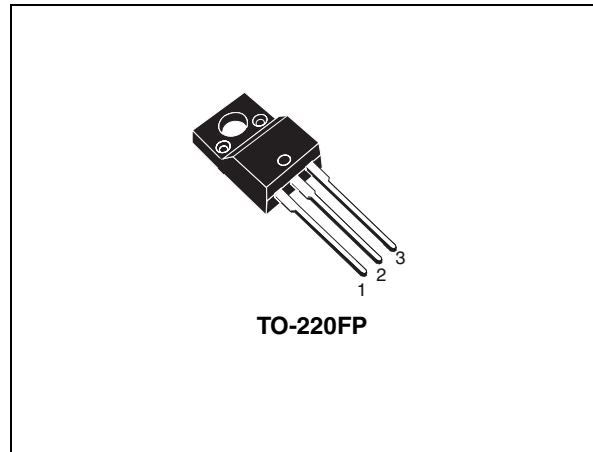


Figure 1. Internal schematic diagram

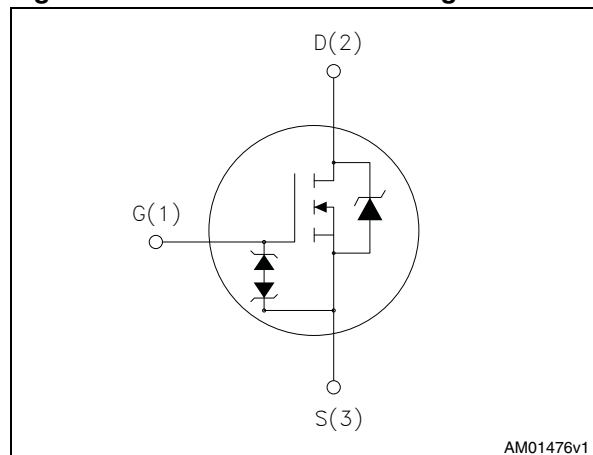


Table 1. Device summary

| Order code | Marking | Package | Packaging |
|------------|---------|----------|-----------|
| STF6N65K3 | 6N65K3 | TO-220FP | Tube |

Contents

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1 Electrical ratings

Table 2. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|----------------------|--|---------------------|------------------|
| V_{DS} | Drain-source voltage ($V_{GS} = 0$) | 650 | V |
| V_{GS} | Gate- source voltage | ± 30 | V |
| I_D | Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$ | 5.4 ⁽¹⁾ | A |
| I_D | Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$ | 3.4 ⁽¹⁾ | A |
| $I_{DM}^{(2)}$ | Drain current (pulsed) | 21.6 ⁽¹⁾ | A |
| P_{TOT} | Total dissipation at $T_C = 25\text{ }^\circ\text{C}$ | 30 | W |
| $V_{ESD(G-S)}$ | Gate source ESD(HBM-C = 100 pF, R = 1.5 k Ω) | 2500 | V |
| dv/dt ⁽³⁾ | Peak diode recovery voltage slope | 12 | V/ns |
| V_{ISO} | Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; $T_C = 25\text{ }^\circ\text{C}$) | 2500 | V |
| T_{stg} | Storage temperature | -55 to 150 | $^\circ\text{C}$ |
| T_j | Max. operating junction temperature | 150 | $^\circ\text{C}$ |

1. Limited by package

2. Pulse width limited by safe operating area

3. $I_{SD} \leq 5.4\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DD} = 80\% V_{(BR)DSS}$

Table 3. Thermal data

| Symbol | Parameter | Value | Unit |
|----------------|--|-------|---------------------------|
| $R_{thj-case}$ | Thermal resistance junction-case max | 4.17 | $^\circ\text{C}/\text{W}$ |
| $R_{thj-amb}$ | Thermal resistance junction-ambient max | 62.5 | $^\circ\text{C}/\text{W}$ |
| T_l | Maximum lead temperature for soldering purpose | 300 | $^\circ\text{C}$ |

Table 4. Avalanche characteristics

| Symbol | Parameter | Max value | Unit |
|----------|--|-----------|------|
| I_{AR} | Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max) | 5.4 | A |
| E_{AS} | Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$) | 125 | mJ |

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 5. On /off states

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|--|--|------|------|-----------|--------------------------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $I_D = 1\text{ mA}$, $V_{GS} = 0$ | 650 | | | V |
| I_{DSS} | Zero gate voltage drain current ($V_{GS} = 0$) | $V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating}$, $T_C = 125\text{ °C}$ | | | 0.8 50 | μA μA |
| I_{GSS} | Gate-body leakage current ($V_{DS} = 0$) | $V_{GS} = \pm 20\text{ V}$ | | | ± 9 | μA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS} = V_{GS}$, $I_D = 50\text{ }\mu\text{A}$ | 3 | 3.75 | 4.5 | V |
| $R_{DS(on)}$ | Static drain-source on resistance | $V_{GS} = 10\text{ V}$, $I_D = 2.8\text{ A}$ | | 1.1 | 1.3 | Ω |

Table 6. Dynamic

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-------------------|--------------------------------|--|------|------|------|----------|
| C_{iss} | Input capacitance | $V_{DS} = 50\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$ | - | 880 | - | pF |
| C_{oss} | Output capacitance | | | 100 | | pF |
| C_{rss} | Reverse transfer capacitance | | | 17 | | pF |
| $C_{o(tr)}^{(1)}$ | Eq. capacitance time related | $V_{GS} = 0$, $V_{DS} = 0\text{ to }480\text{ V}$ | - | 64 | - | pF |
| $C_{o(er)}^{(2)}$ | Eq. capacitance energy related | | | 30 | | pF |
| R_G | Intrinsic gate resistance | $f = 1\text{ MHz}$ open drain | - | 4 | - | Ω |
| Q_g | Total gate charge | $V_{DD} = 520\text{ V}$, $I_D = 5.4\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 16) | - | 35 | - | nC |
| Q_{gs} | Gate-source charge | | | 5 | | nC |
| Q_{gd} | Gate-drain charge | | | 24 | | nC |

- $C_{oss\text{ eq}}$: time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
- $C_{oss\text{ eq}}$: energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--------------|---------------------|--|------|------|------|------|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD} = 325\text{ V}$, $I_D = 2.7\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 15) | - | 25 | - | ns |
| t_r | Rise time | | - | 15 | - | ns |
| $t_{d(off)}$ | Turn-off-delay time | | - | 54 | - | ns |
| t_f | Fall time | | - | 22 | - | ns |

Table 8. Source drain diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit | |
|-----------------|-------------------------------|--|------|------|------|------|----|
| I_{SD} | Source-drain current | | - | | 5.4 | A | |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) | | | | 21.6 | A | |
| $V_{SD}^{(2)}$ | Forward on voltage | $I_{SD} = 5.4\text{ A}$, $V_{GS} = 0$ | - | | 1.5 | V | |
| t_{rr} | Reverse recovery time | $I_{SD} = 5.4\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see Figure 20) | - | 300 | | ns | |
| Q_{rr} | Reverse recovery charge | | | | 2000 | | nC |
| I_{RRM} | Reverse recovery current | | | | 14 | | A |
| t_{rr} | Reverse recovery time | $I_{SD} = 5.4\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 20) | - | 350 | | ns | |
| Q_{rr} | Reverse recovery charge | | | | 2500 | | nC |
| I_{RRM} | Reverse recovery current | | | | 15 | | A |

1. Pulse width limited by safe operating area

2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

Table 9. Gate-source Zener diode

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|------------|-------------------------------|---|-----|-----|-----|------|
| BV_{GSO} | Gate-source breakdown voltage | $I_{gs} = \pm 1\text{ mA}$ (open drain) | 30 | - | - | V |

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

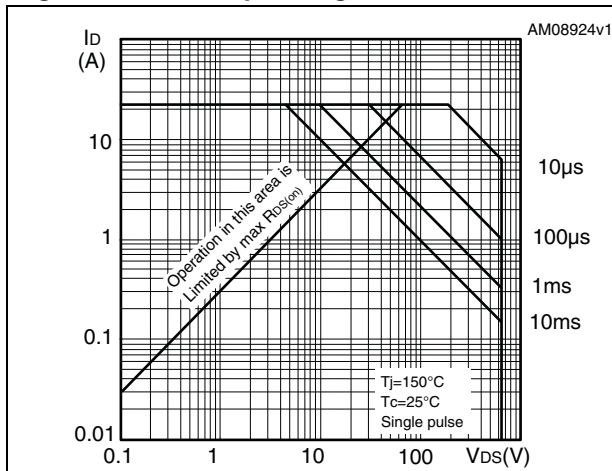


Figure 3. Thermal impedance

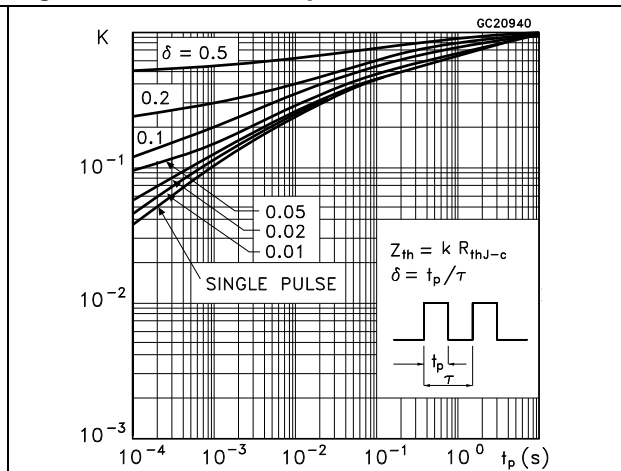


Figure 4. Output characteristics

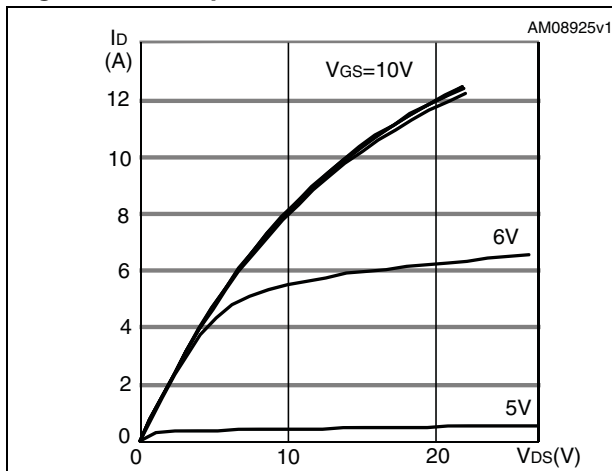


Figure 5. Transfer characteristics

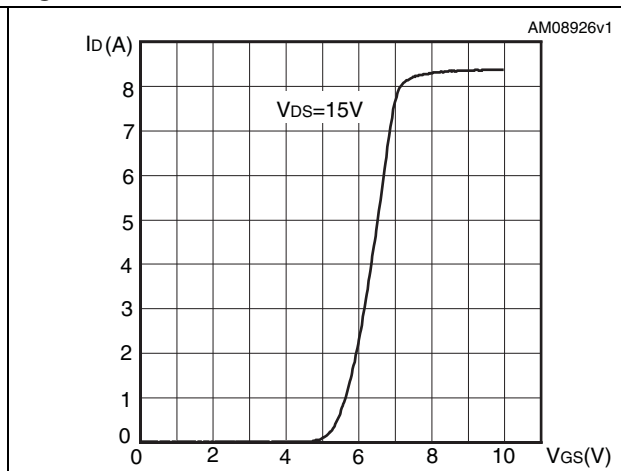


Figure 6. Gate charge vs gate-source voltage

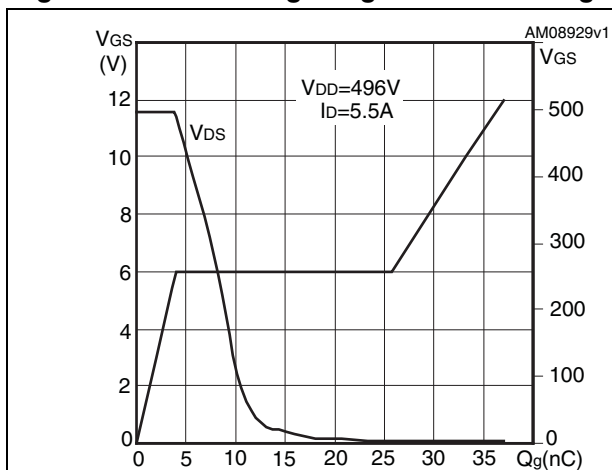


Figure 7. Static drain-source on resistance

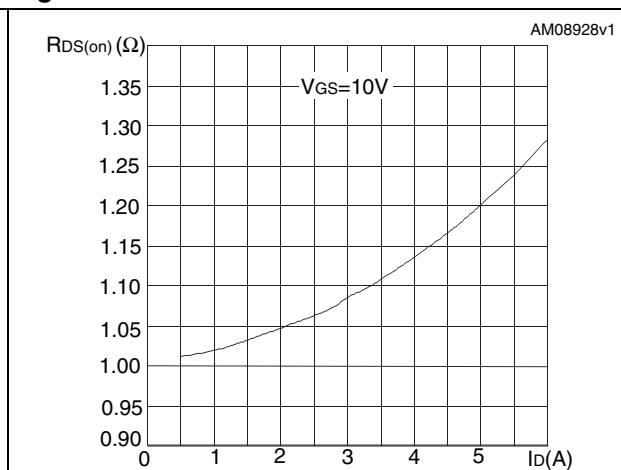


Figure 8. Capacitance variations

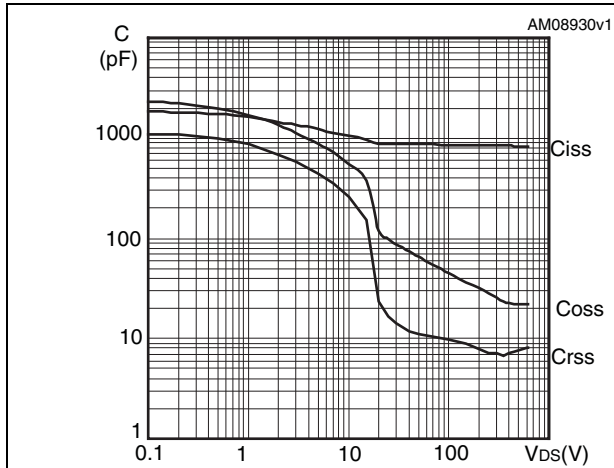


Figure 9. Output capacitance stored energy

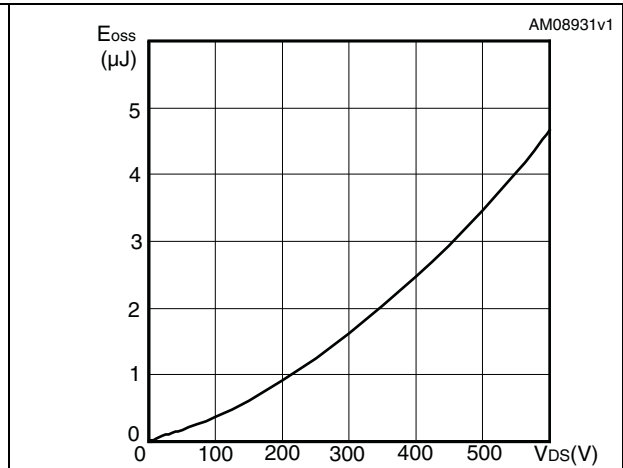


Figure 10. Normalized gate threshold voltage vs temperature

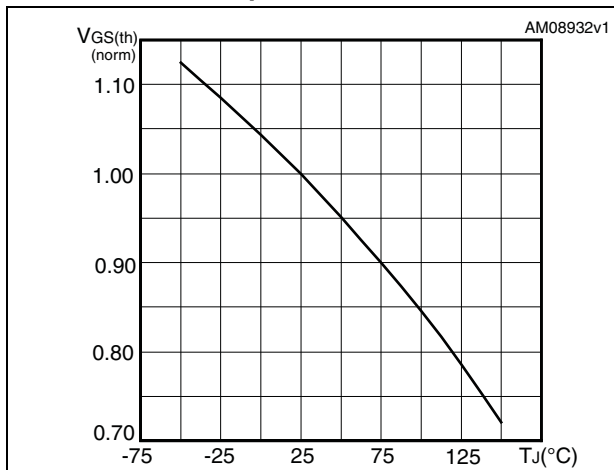


Figure 11. Normalized on resistance vs temperature

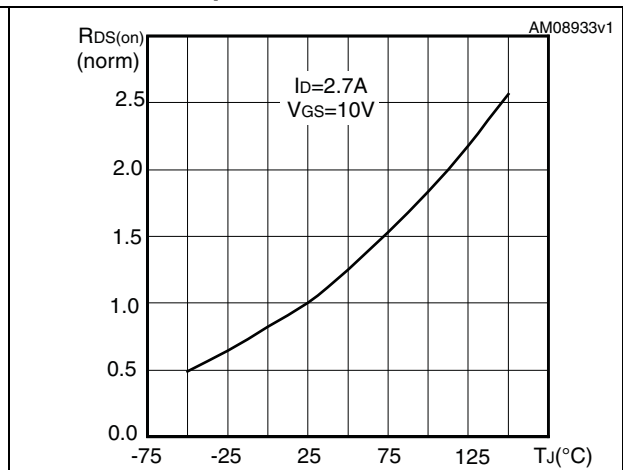


Figure 12. Normalized BV_{DSS} vs temperature

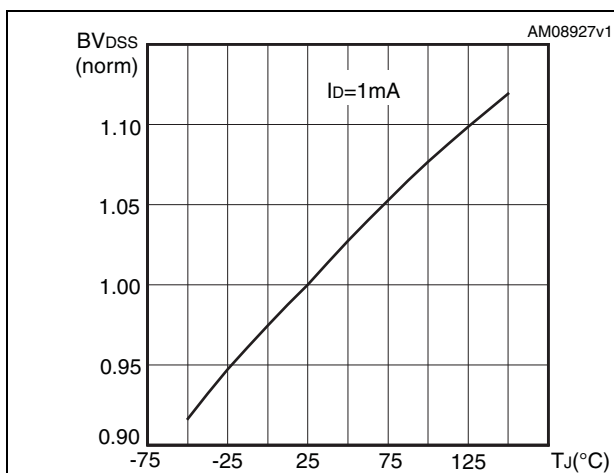


Figure 13. Source-drain diode forward characteristics

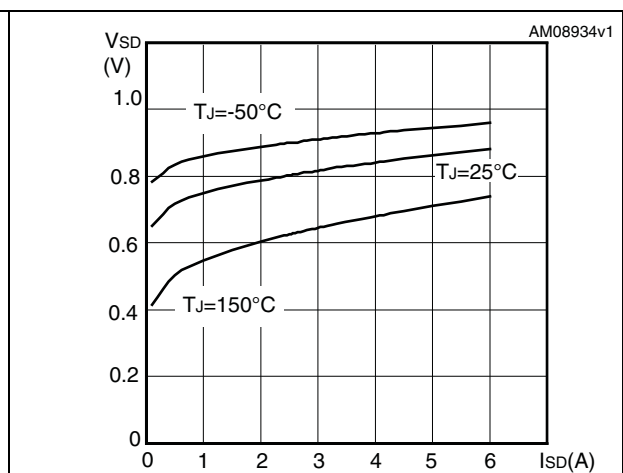
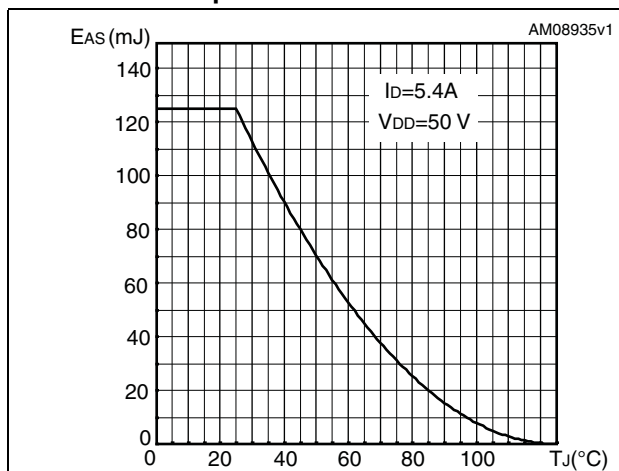


Figure 14. Maximum avalanche energy vs temperature



3 Test circuits

Figure 15. Switching times test circuit for resistive load

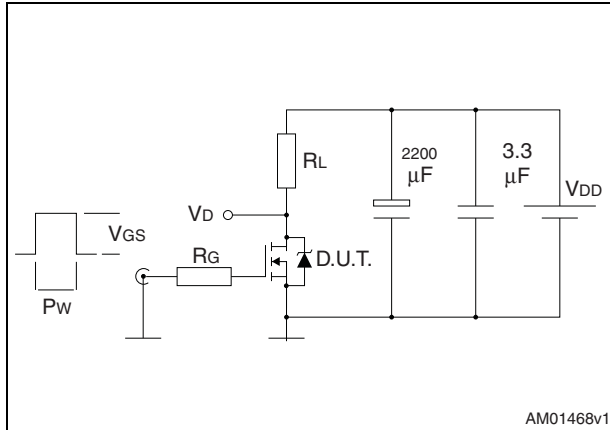


Figure 16. Gate charge test circuit

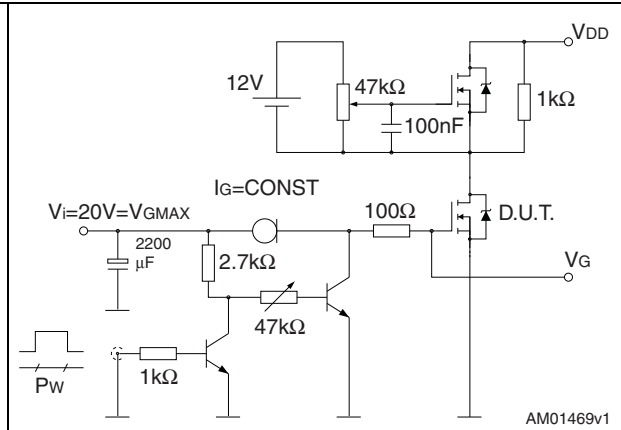


Figure 17. Test circuit for inductive load switching and diode recovery times

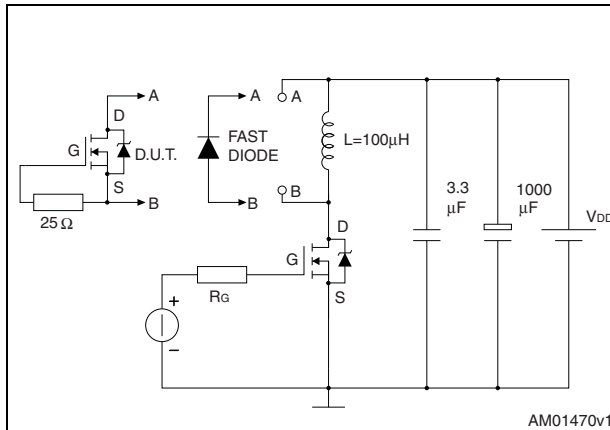


Figure 18. Unclamped inductive load test circuit

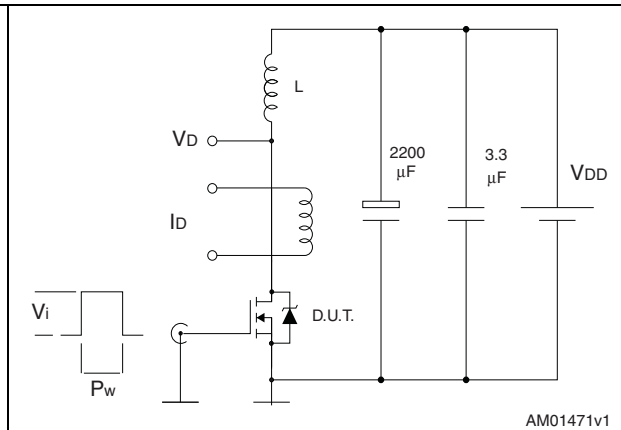


Figure 19. Unclamped inductive waveform

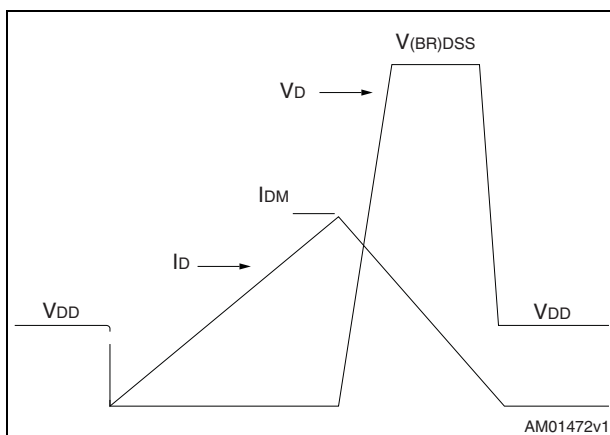
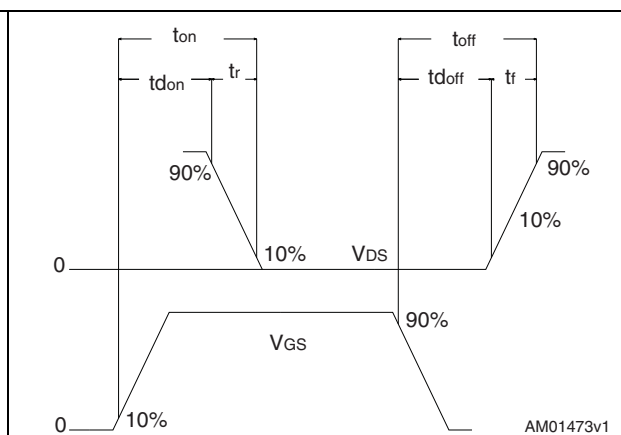


Figure 20. Switching time waveform



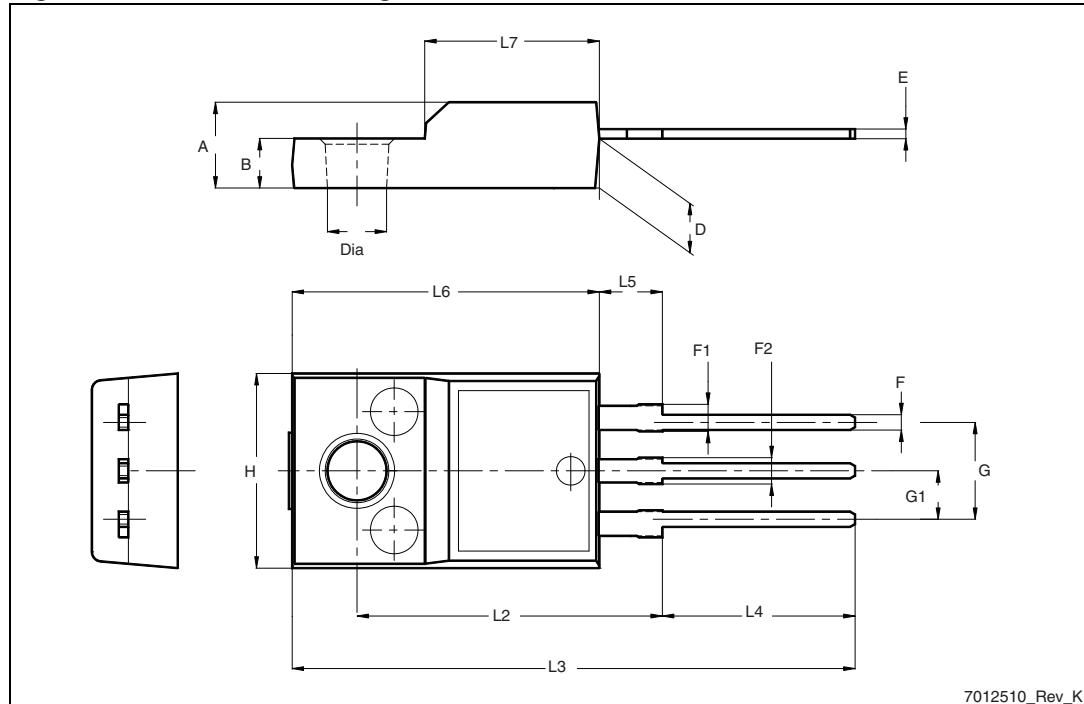
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 10. TO-220FP mechanical data

| Dim. | mm | | |
|------|------|------|------|
| | Min. | Typ. | Max. |
| A | 4.4 | | 4.6 |
| B | 2.5 | | 2.7 |
| D | 2.5 | | 2.75 |
| E | 0.45 | | 0.7 |
| F | 0.75 | | 1 |
| F1 | 1.15 | | 1.70 |
| F2 | 1.15 | | 1.70 |
| G | 4.95 | | 5.2 |
| G1 | 2.4 | | 2.7 |
| H | 10 | | 10.4 |
| L2 | | 16 | |
| L3 | 28.6 | | 30.6 |
| L4 | 9.8 | | 10.6 |
| L5 | 2.9 | | 3.6 |
| L6 | 15.9 | | 16.4 |
| L7 | 9 | | 9.3 |
| Dia | 3 | | 3.2 |

Figure 21. TO-220FP drawing



7012510_Rev_K

5 Revision history

Table 11. Document revision history

| Date | Revision | Changes |
|-------------|----------|---------------|
| 05-Apr-2011 | 1 | First release |

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