



STL23NM60ND

N-channel 600 V, 0.150 Ω , 19.5 A, FDmesh™ II Power MOSFET
(with fast diode) PowerFLAT™ (8x8) HV

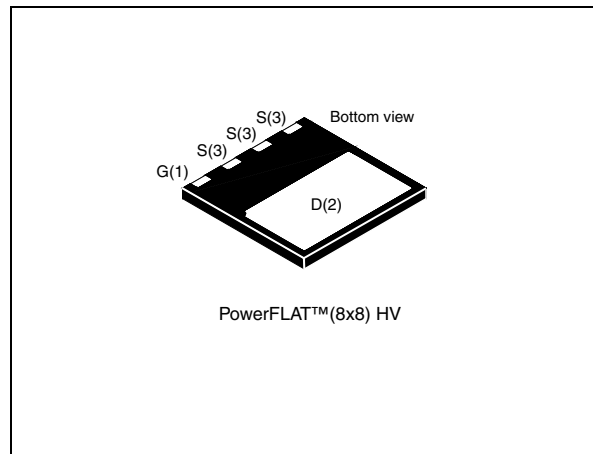
Preliminary data

Features

Type	V _{DSS} (@T _{Jmax})	R _{DS(on)} max	I _D
STL23NM60ND	650 V	< 0.180 Ω	19.5 A ⁽¹⁾

1. This value is rated according to R_{thj-case}.

- The worldwide best R_{DS(on)} * area amongst the fast recovery diode devices
- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance
- High dv/dt and avalanche capabilities



Application

- Switching applications

Description

The FDmesh™ II series belongs to the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a new vertical structure to the company's strip layout and associates all advantages of reduced on-resistance and fast switching with an intrinsic fast-recovery body diode. It is therefore strongly recommended for bridge topologies, in particular ZVS phase-shift converters.

Figure 1. Internal schematic diagram

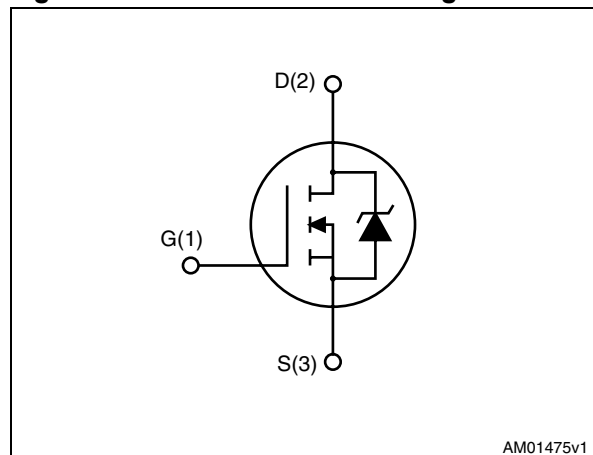


Table 1. Device summary

Order code	Marking	Package	Packaging
STL23NM60ND	23NM60ND	PowerFLAT™ 8x8 HV	Tape and reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	600	V
V_{GS}	Gate-source voltage	± 25	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	19.5	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	11.7	A
$I_{DM}^{(1),(2)}$	Drain current (pulsed)	78	A
$I_D^{(3)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	2.75	A
$I_D^{(3)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	1.75	A
$I_{DM}^{(2),(3)}$	Drain current (pulsed)	11	A
$P_{TOT}^{(3)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$ (steady state)	150	W
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$ (steady state)	3	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	9	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	700	mJ
$dv/dt^{(4)}$	Peak diode recovery voltage slope	40	V/ns
T_{stg}	Storage temperature	- 55 to 150	$^\circ\text{C}$
T_j	Max. operating junction temperature	150	$^\circ\text{C}$

1. The value is rated according to $R_{thj-case}$
2. Pulse width limited by safe operating area
3. When mounted on FR-4 board of 1 inch^2 , 2oz Cu
4. $I_{SD} \leq 19.5\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{Peak} < V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.83	$^\circ\text{C}/\text{W}$
$R_{thj-amb}^{(1)}$	Thermal resistance junction-amb max	45	$^\circ\text{C}/\text{W}$
T_l	Maximum lead temperature for soldering purposes	300	$^\circ\text{C}$

1. When mounted on 1 inch^2 FR-4 board, 2 oz Cu

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	600			V
$dv/dt^{(1)}$	Drain-source voltage slope	$V_{DD} = 480\text{ V}$, $I_D = 19.5\text{ A}$, $V_{GS} = 10\text{ V}$	48			V/ns
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$, $V_{DS} = \text{Max rating}$, @ 125 °C			1 100	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 10\text{ A}$		0.150	0.180	Ω

1. Characteristic value at turn off on inductive load

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 50\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	2050	-	pF
C_{oss}	Output capacitance			80		pF
C_{rss}	Reverse transfer capacitance			8		pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0$, $V_{DS} = 0\text{ to }480\text{ V}$	-	318	-	pF
R_g	Gate input resistance	$f = 1\text{ MHz}$ Gate DC Bias=0 Test signal level=20 mV open drain	-	4	-	Ω
Q_g	Total gate charge	$V_{DD} = 480\text{ V}$, $I_D = 19.5\text{ A}$ $V_{GS} = 10\text{ V}$ (see Figure 3)	-	70	-	nC
Q_{gs}	Gate-source charge			10		nC
Q_{gd}	Gate-drain charge			30		nC

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 10\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 2)	-	25	-	ns
t_r	Rise time		-	45	-	ns
$t_{d(off)}$	Turn-off delay time		-	90	-	ns
t_f	Fall time		-	40	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		19.5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				78	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 19.5\text{ A}$, $V_{GS}=0$	-		1.3	V
t_{rr}	Reverse recovery time	$I_{SD} = 19.5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 100\text{ V}$ (see Figure 4)	-	190		ns
Q_{rr}	Reverse recovery charge		-	1.2		μC
I_{RRM}	Reverse recovery current		-	13		A
t_{rr}	Reverse recovery time	$V_{DD} = 100\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$, $I_{SD} = 19.5\text{ A}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 4)	-	260		ns
Q_{rr}	Reverse recovery charge		-	2.0		μC
I_{RRM}	Reverse recovery current		-	15		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

3 Test circuits

Figure 2. Switching times test circuit for resistive load

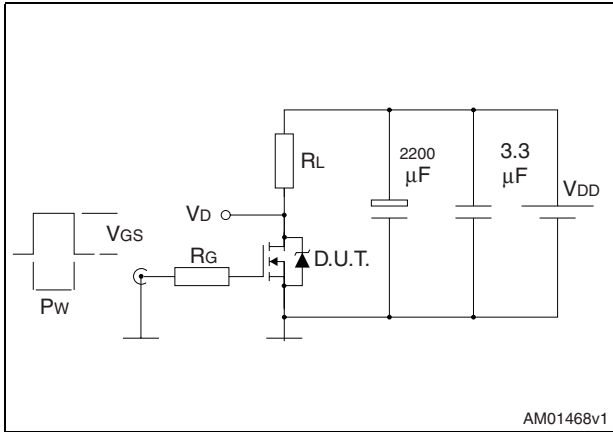


Figure 3. Gate charge test circuit

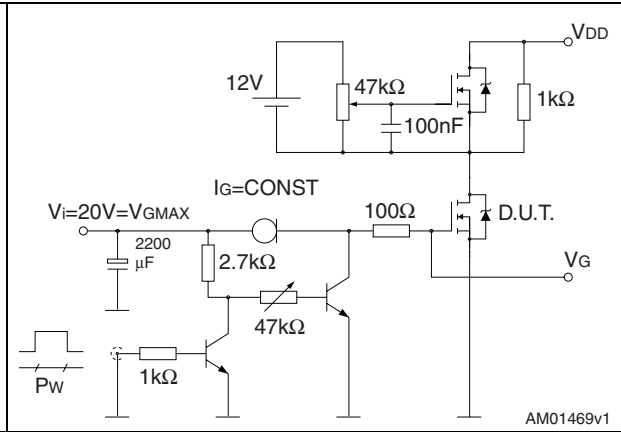


Figure 4. Test circuit for inductive load switching and diode recovery times

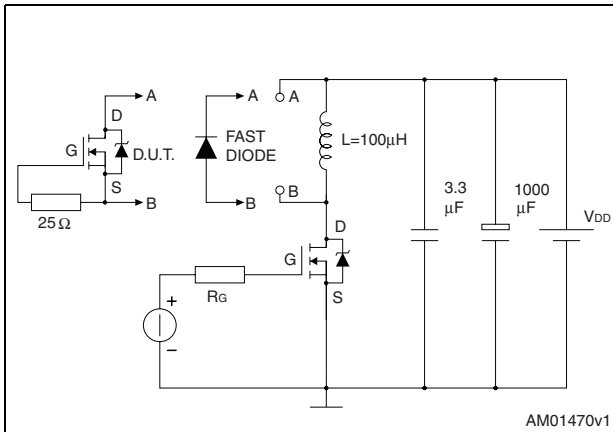


Figure 5. Unclamped inductive load test circuit

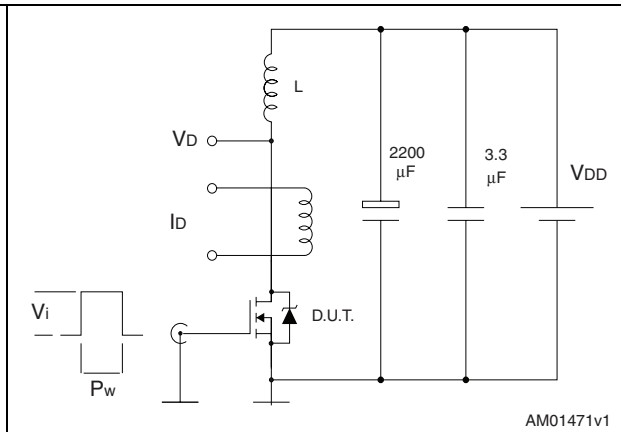


Figure 6. Unclamped inductive waveform

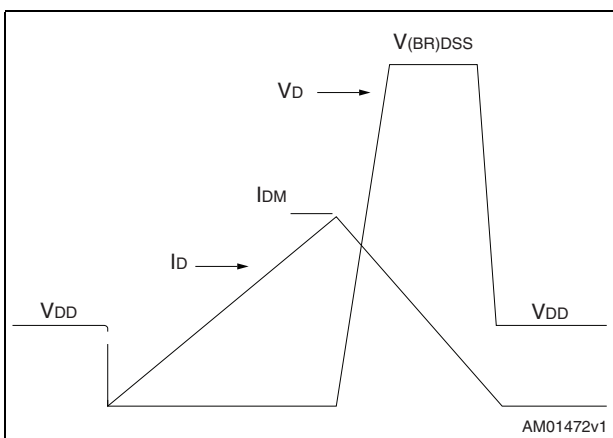
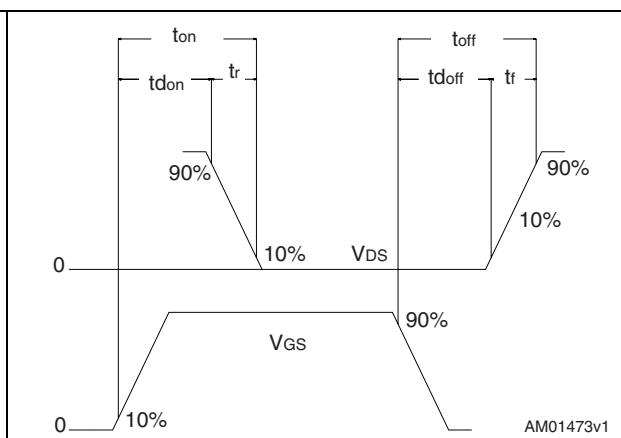


Figure 7. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. PowerFLAT™ 8x8 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1		0.02	0.05
b	0.95	1.00	1.05
c		0.10	
D		8.00	
E		8.00	
D2	7.05	7.20	7.30
E2	4.15	4.30	4.40
e		2.00	
L	0.40	0.50	0.60

Figure 8. PowerFLAT™ 8x8 HV drawing mechanical data

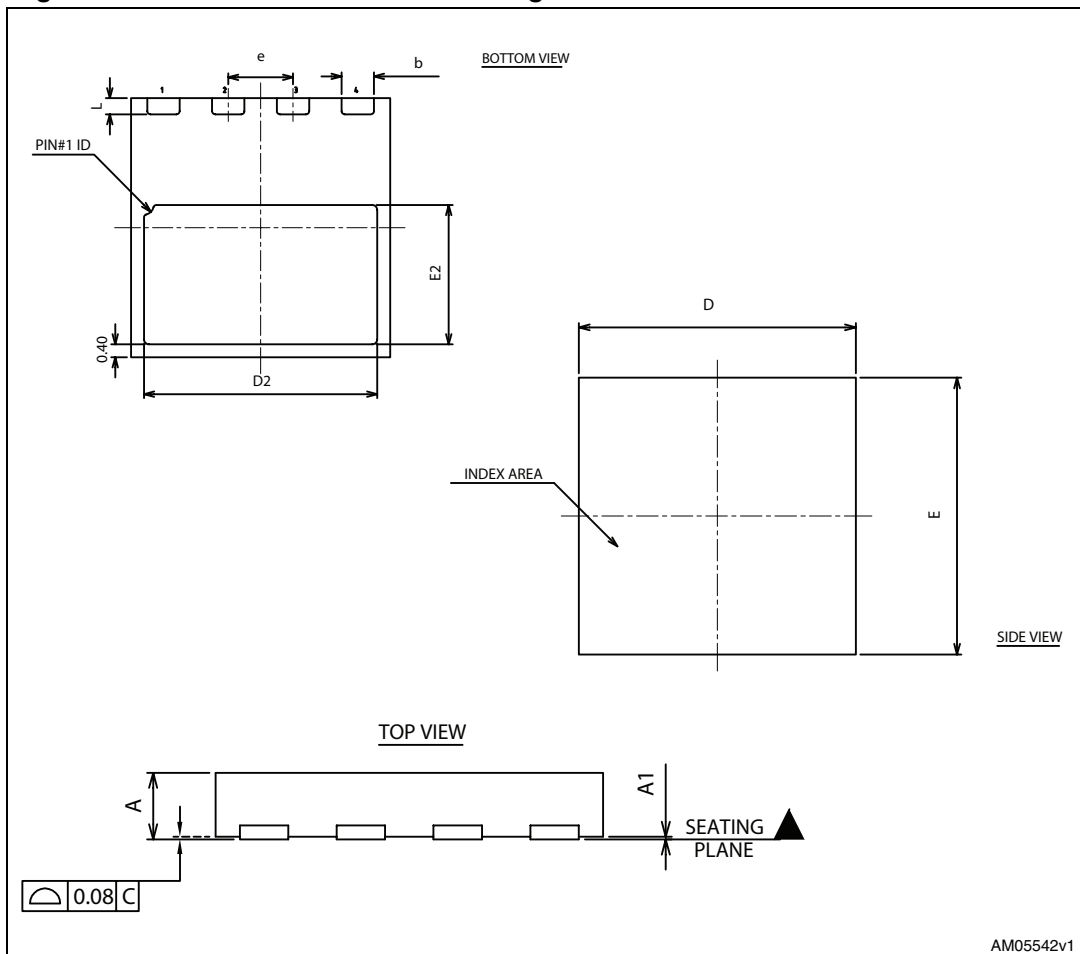
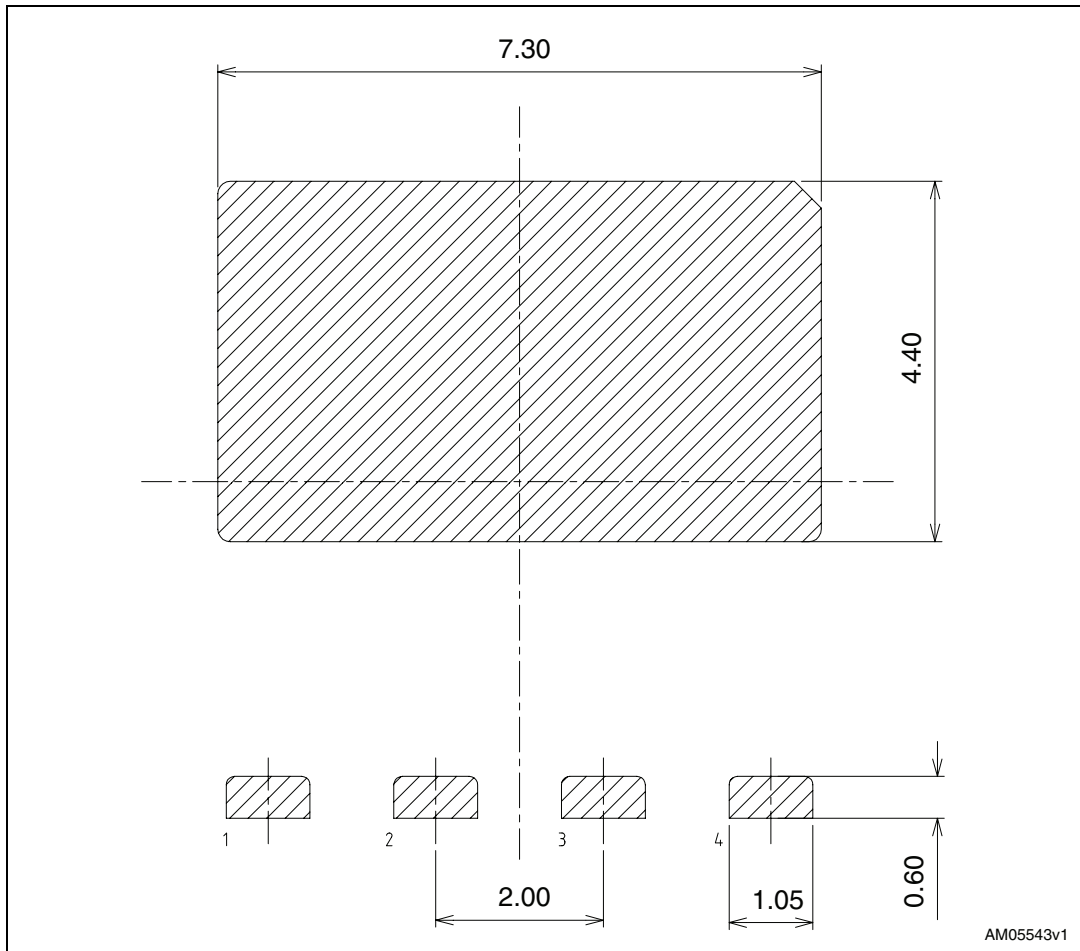


Figure 9. PowerFLAT™ 8x8 HV recommended footprint



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
28-Apr-2010	1	First release

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