



# STD50N03L STD50N03L-1

N-CHANNEL 30V - 9.2mΩ - 40A - DPAK/IPAK  
STripFET™ III Power MOSFET

## General features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STD50N03L	30V	10.5mΩ	40A
STD50N03L-1	30V	10.5mΩ	40A

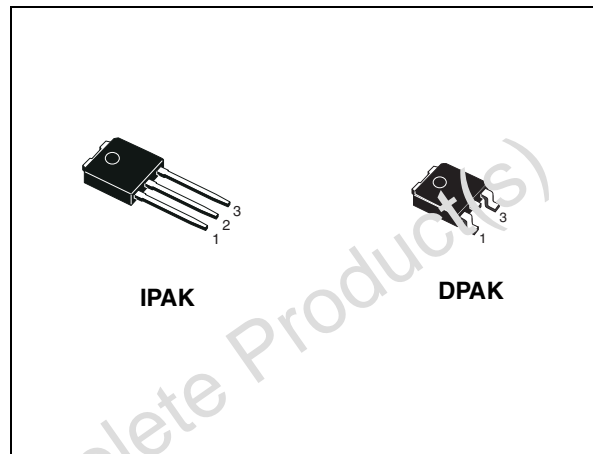
- R<sub>DS(on)</sub>\*Q<sub>g</sub> industry's benchmark
- Conduction losses reduced
- Switching losses reduced
- Low threshold device

## Description

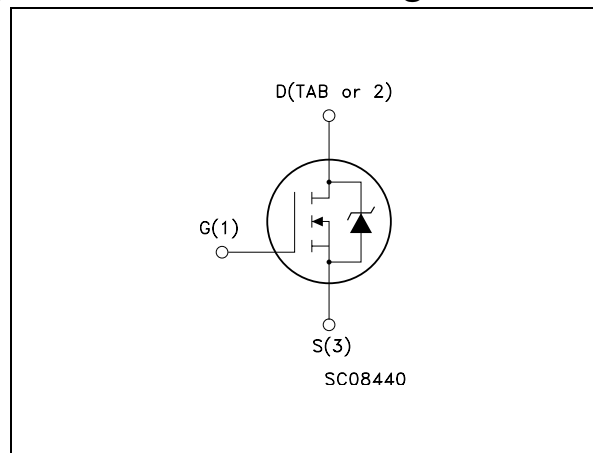
This product utilizes the latest advanced design rules of ST's proprietary STripFET™ technology. This is suitable for the most demanding DC-DC converter application where high efficiency is to be achieved.

## Applications

- Switching applications



## Internal schematic diagram



## Order codes

Part number	Marking	Package	Packaging
STD50N03L	D50N03L	DPAK	Tape & reel
STD50N03L-1	D50N03L	IPAK	Tube

# Contents

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# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	30	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	40	A
$I_D$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	36	A
$I_{DM}^{(2)}$	Drain current (pulsed)	160	A
$P_{TOT}$	Total dissipation at $T_C = 25^\circ\text{C}$	60	W
	Derating factor	0.4	W/ $^\circ\text{C}$
$E_{AS}^{(3)}$	Single pulse avalanche energy	230	mJ
$T_J$ $T_{stg}$	Operating junction temperature Storage temperature	-55 to 175	$^\circ\text{C}$

1. Limited by wire bonding
2. Pulse width limited by safe operating area
3. Starting  $T_J = 25^\circ\text{C}$ ,  $I_D = 20\text{A}$ ,  $V_{DD} = 15\text{V}$

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJ-Case}$	Thermal resistance junction-case max	2.5	$^\circ\text{C}/\text{W}$
$R_{thJ-Amb}$	Thermal resistance junction-ambient max	100	$^\circ\text{C}/\text{W}$
	Maximum lead temperature for soldering purpose	275	$^\circ\text{C}$

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}C$  unless otherwise specified)

**Table 3. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\mu A, V_{GS} = 0$	30			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 30V$ $V_{DS} = 30V, T_C=125^{\circ}C$			1 10	$\mu A$ $\mu A$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20V$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	1			V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 20A$ $V_{GS} = 5V, I_D = 20A$		9.2 0.012	10.5 0.019	$m\Omega$ $\Omega$

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25V, f = 1MHz,$ $V_{GS} = 0$		1434		pF
$C_{oss}$	Output capacitance			294		pF
$C_{rss}$	Reverse transfer capacitance			48		pF
$Q_g$	Total gate charge	$V_{DD} = 15V, I_D = 40A$		10.4	14	nC
$Q_{gs}$	Gate-source charge	$V_{GS} = 5V$		5.1		nC
$Q_{gd}$	Gate-drain charge	(see Figure 13)		3.7		nC
$Q_{OSS}^{(1)}$	Output charge	$V_{DS} = 24V ; V_{GS} = 0$		12.6		nC
$R_G$	Gate input resistance	f=1MHz Gate Bias Bias=0 Test signal Level=20mV open drain		1.1		$\Omega$

1.  $Q_{OSS} = C_{OSS} \cdot D \cdot V_{in}$ ;  $C_{OSS} = C_{gd} + C_{gd}$ . See [Appendix A](#)

**Table 5. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on delay time Rise time	$V_{DD}=15V, I_D=25A,$ $R_G=4.7\Omega, V_{GS}=4.5V$ (see Figure 12)		15 125		ns ns
$t_{d(off)}$ $t_f$	Turn-off delay time Fall time	$V_{DD}=15V, I_D=25A,$ $R_G=4.7\Omega, V_{GS}=4.5V$ (see Figure 12)		14 45		ns ns

**Table 6. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM}^{(1)}$	Source-drain current Source-drain current (pulsed)				40 160	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=20A, V_{GS}=0$			1.3	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=40A, di/dt = 100A/\mu s,$ $V_{DD}=10V, T_J = 25^\circ C$ (see Figure 17)		26 15.6 1.2		ns nC A
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=40A, di/dt = 100A/\mu s,$ $V_{DD}=10V, T_J = 150^\circ C$ (see Figure 17)		26.4 18.1 1.4		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 $\mu s$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

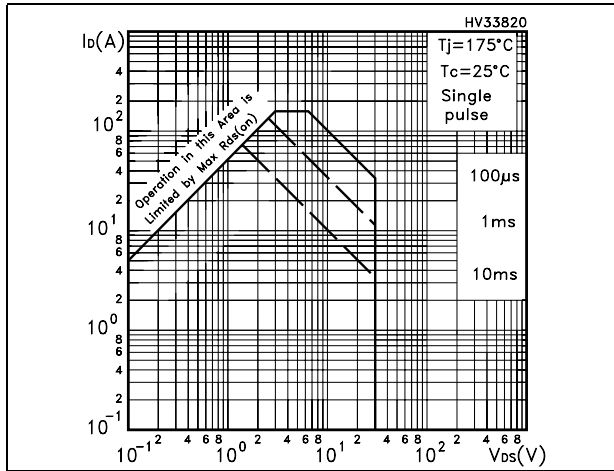


Figure 2. Thermal impedance

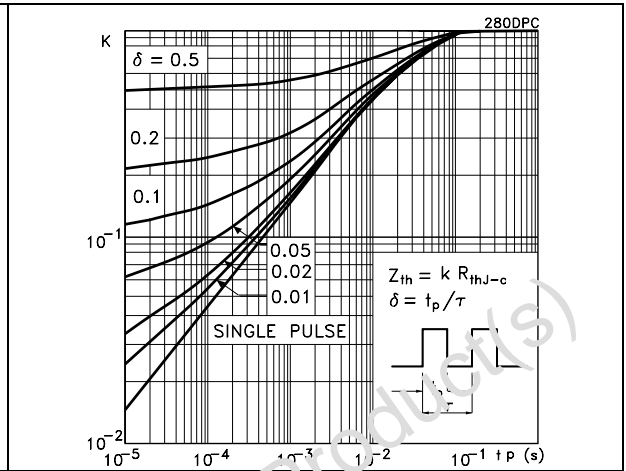


Figure 3. Output characteristics

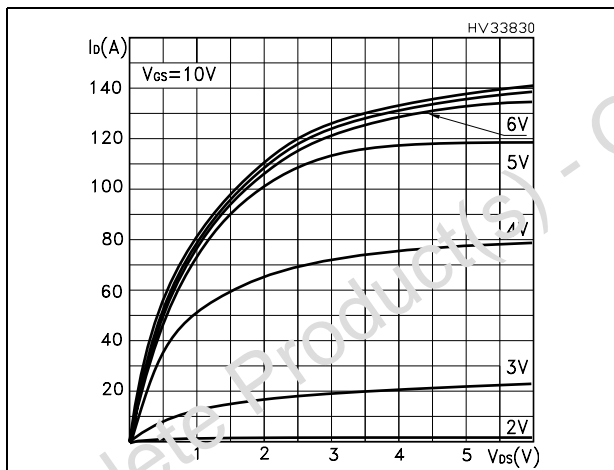


Figure 4. Transfer characteristics

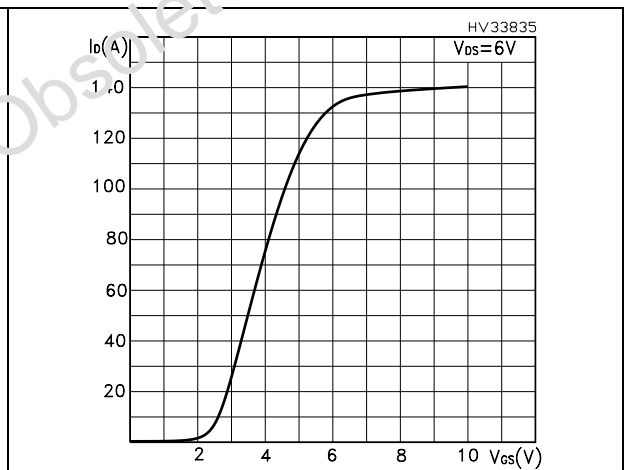


Figure 5. Normalized  $B_{V_{DS}}$  vs temperature

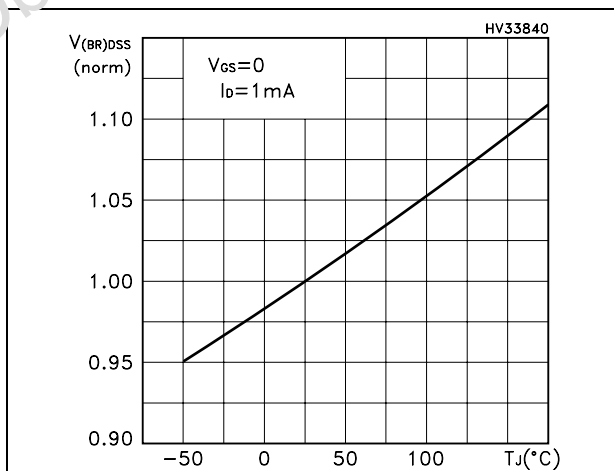


Figure 6. Static drain-source on resistance

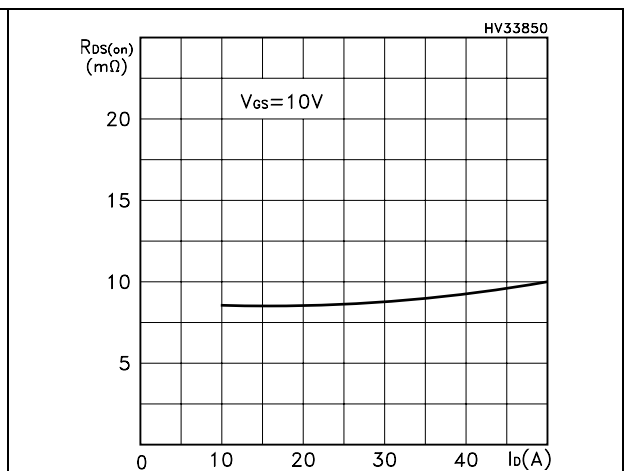


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

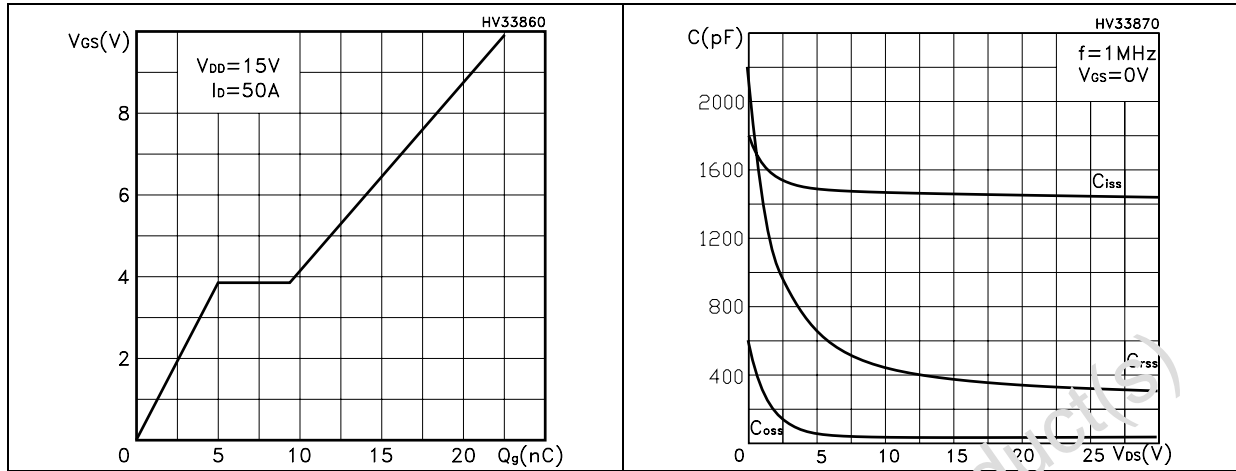


Figure 9. Normalized gate threshold voltage vs temperature Figure 10. Normalized on resistance vs temperature

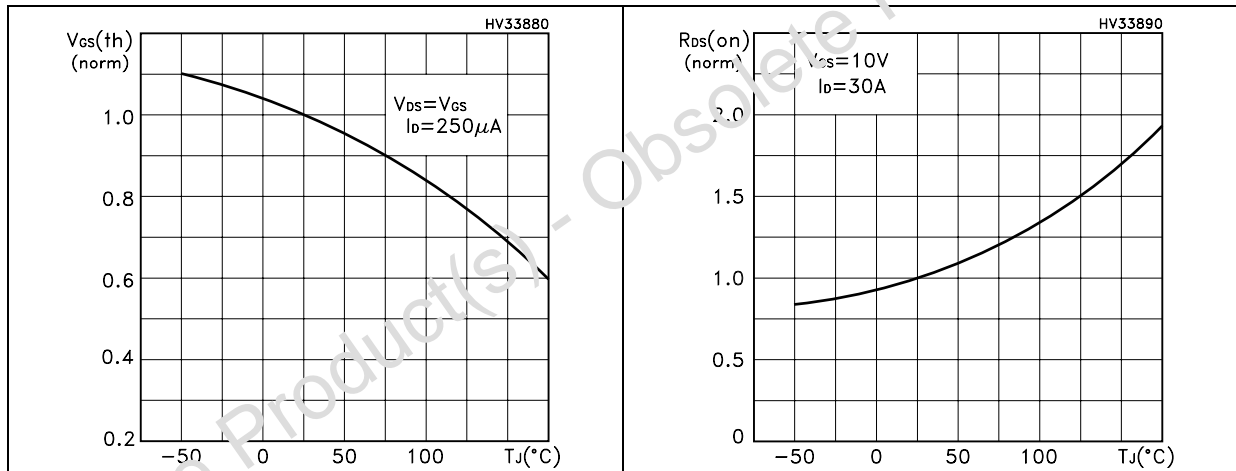
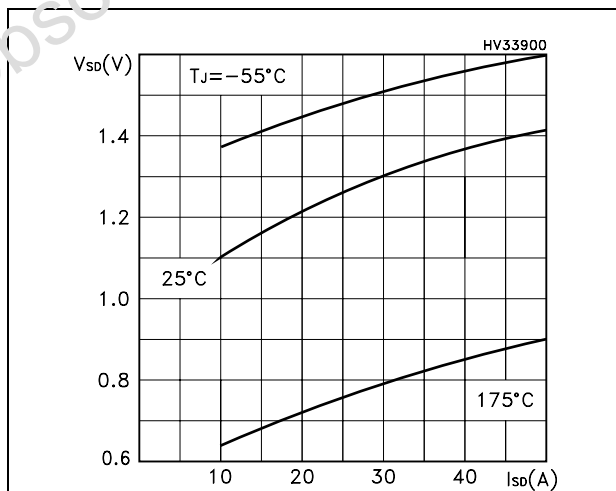


Figure 11. Source-drain diode forward characteristics



### 3 Test circuit

Figure 12. Switching times test circuit for resistive load

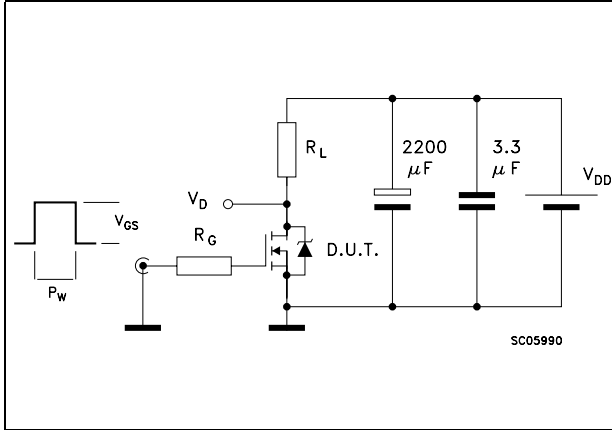


Figure 13. Gate charge test circuit

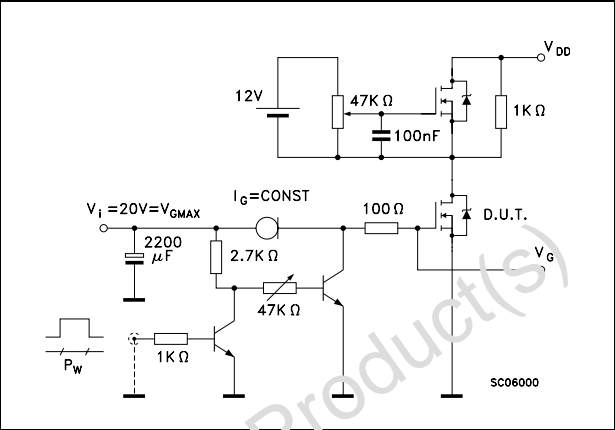


Figure 14. Test circuit for inductive load switching and diode recovery times

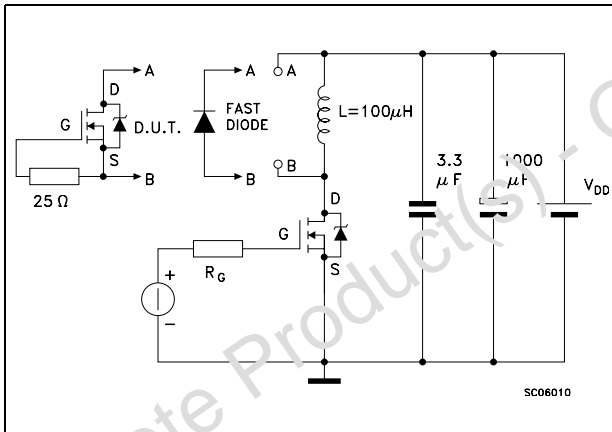


Figure 15. Unclamped Inductive load test circuit

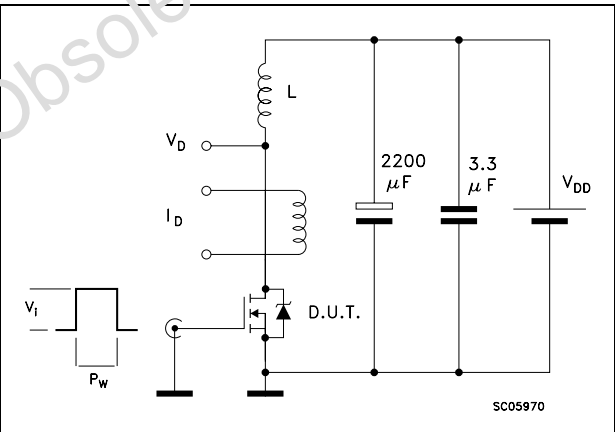


Figure 16. Unclamped inductive waveform

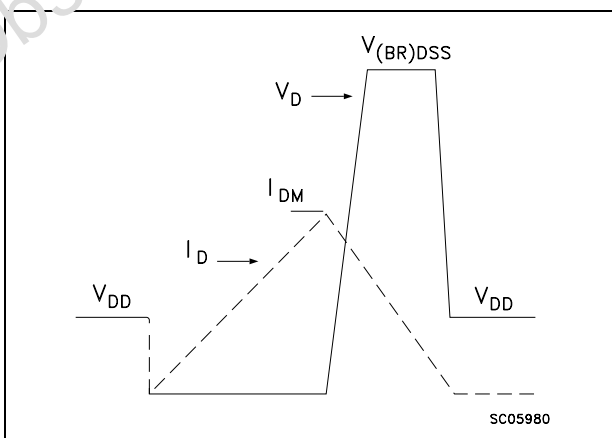
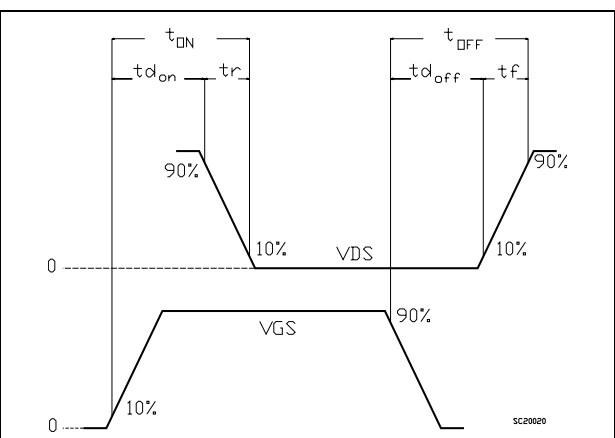


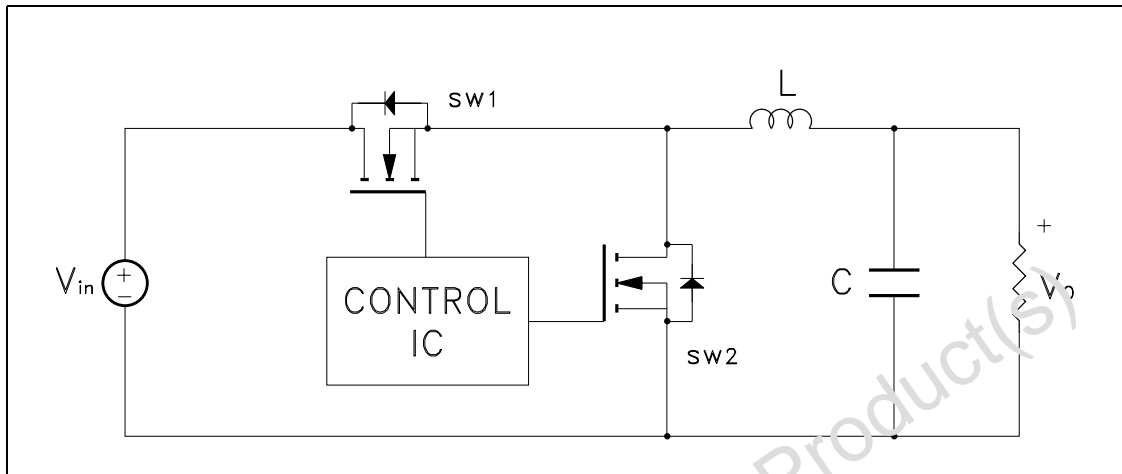
Figure 17. Switching time waveform





## Appendix A Buck converter

Figure 18. Power losses estimation



The power losses associated with the FETs in a Synchronous Buck converter can be estimated using the equations shown in the table below. The formulas give a good approximation, for the sake of performance comparison, of how different pairs of devices affect the converter efficiency. However a very important parameter, the working temperature, is not considered. The real device behavior is really dependent on how the heat generated inside the devices is removed to allow for a safer working junction temperature.

The low side (SW2) device requires:

- Very low  $R_{DS(on)}$  to reduce conduction losses
- Small  $Q_{gl}$  to reduce the gate charge losses
- Small  $C_{oss}$  to reduce losses due to output capacitance
- Small  $Q_{rr}$  to reduce losses on SW1 during its turn-on
- The  $C_{gd}/C_{gs}$  ratio lower than  $V_{th}/V_{gg}$  ratio especially with low drain to source
- $V_{gs}$  voltage to avoid the cross conduction phenomenon;

The high side (SW1) device requires:

- Small  $R_g$  and  $L_s$  to allow higher gate current peak and to limit the voltage feedback on the gate
- Small  $Q_g$  to have a faster commutation and to reduce gate charge losses

Low  $R_{DS(on)}$  to reduce the conduction losses.

**Table 7. Power losses**

		High side switching (SW1)	Low side switch (SW2)
$P_{conduction}$		$R_{DS(on)SW1} * I_L^2 * \delta$	$R_{DS(on)SW2} * I_L^2 * (1 - \delta)$
$P_{switching}$		$V_{in} * (Q_{gsth(SW1)} + Q_{gd(SW1)}) * f * \frac{I_L}{I_g}$	Zero Voltage Switching
$P_{diode}$	Recovery (1)	Not applicable	$V_{in} * Q_{rr(SW2)} * f$
	Conduction	Not applicable	$V_{f(SW2)} * I_L * t_{deadtime} * f$
$P_{gate(Q_G)}$		$Q_{g(SW1)} * V_{gg} * f$	$Q_{gls(SW2)} * V_{gg} * f$
$P_{Qoss}$		$\frac{V_{in} * Q_{oss(SW1)} * f}{2}$	$\frac{V_{in} * Q_{oss(SW2)} * f}{2}$

1. Dissipated by SW1 during turn-on

**Table 8. Paramiters meaning**

Parameter	Meaning
d	Duty-cycle
$Q_{post}$	Post threshold gate charge
$Q_{g3}$	Third quadrant gate charge
$P_{conduction}$	On state losses
$P_{switching}$	On-off transition losses
$P_{diode}$	Conduction and reverse recovery diode losses
$P_{gate}$	Gate drive losses
$P_{Qoss}$	Output capacitance losses

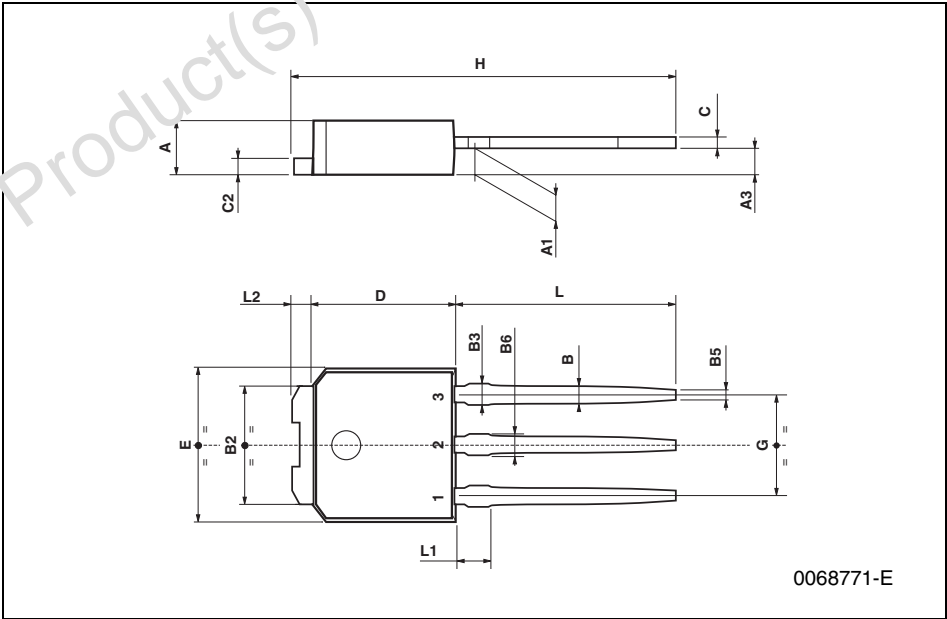
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at : [www.st.com](http://www.st.com)

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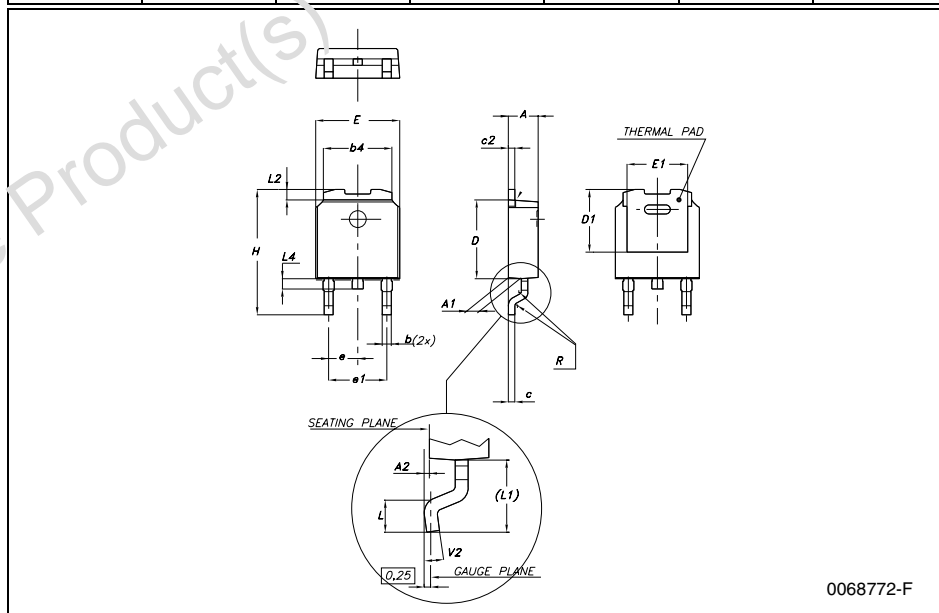
**TO-251 (IPAK) MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.7	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039



**DPAK MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
b4	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1		0.201		
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
e		2.28			0.090	
e1	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L	1			0.039		
(L1)		2.8			0.110	
L2		0.8			0.031	
L4	0.6		1	0.023		0.039
R		0.2			0.008	
V2	0°		8°	0°		8°



## 5 Packaging mechanical data

### DPAK FOOTPRINT



### TAPE AND REEL SHIPMENT

**REEL MECHANICAL DATA**

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

**TAPE MECHANICAL DATA**

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A <sub>0</sub>	6.8	7	0.267	0.275
B <sub>0</sub>	10.4	10.6	0.409	0.417
B <sub>1</sub>		12.1		0.476
D	1.5	1.6	0.059	0.063
D <sub>1</sub>	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K <sub>0</sub>	2.55	2.75	0.100	0.108
P <sub>0</sub>	3.9	4.1	0.153	0.161
P <sub>1</sub>	7.9	8.1	0.311	0.319
P <sub>2</sub>	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641

## 6 Revision history

Table 9. Revision history

Date	Revision	Changes
31-Jul-2006	1	Initial release.
27-Oct-2006	2	Modified <i>Figure 1.: Safe operating area on page 6</i>

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