Never stop thinking

n-Channel Power MOSFET

OptiMOS™
BSC0902NSI

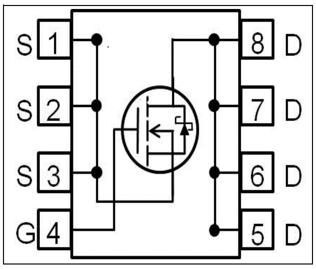
Data Sheet

2.1, 2011-09-08
Final

Industrial & Multimarket

1 Description

OptiMOS™30V products are class leading power MOSFETs for highest power density and energy efficient solutions. Ultra low gate and output charges together with lowest on state resistance in small footprint packages make OptiMOS™ 30V the best choice for the demanding requirements of voltage regulator solutions in Servers, Datacom and Telecom applications. Super fast switching Control FETs together with low EMI Sync FETs provide solutions that are easy to design in. OptiMOS™ products are available in high performance packages to tackle your most challenging applications giving full flexibility in optimizing space, efficiency and cost. OptiMOS™ products are designed to meet and exceed the energy efficiency and power density requirements of the sharpened next generation voltage regulation standards in computing applications.



Features

- Optimized SyncFET for high performance buck converter
- 100% avalanche tested
- Very low on-resistance $R_{DS(on)}$ @ V_{GS}=4.5 V
- N-channel
- Qualified according to JEDEC[1)] for target applications
- Superior thermal resistance
- Pb-free plating; RoHS compliant
- Halogen-free according to IEC61249-2-21
- Integrated monolithic Schottky-like diode

Applications

- On board power for server
- Power managment for high performance computing
- Synchronous rectification
- High power density point of load converters

Table 1 Key Performance Parameters

Parameter	Value	Unit		Related Links
V_{DS}	30	V		IFX OptiMOS webpage
$R_{DS(on),max}$	2.8	mΩ		IFX OptiMOS product brief
I_D	100	A		IFX OptiMOS spice models
Q_{OSS}	17	nC		IFX Design tools
$Q_{g\cdot typ}$	24			

Type	Package	Marking
BSC0902NSI	PG-TDSON-8	0902NSI

1) J-STD20 and JESD22

2 Maximum ratings

at T_j = 25 °C, unless otherwise specified.

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	-	-	100	A	V_{GS}=10 V, T_C=25 °C
		-	-	65		V_{GS}=10 V, T_C=100 °C
		-	-	89		V_{GS}=4.5 V, T_C=25 °C
		-	-	56		V_{GS}=4.5 V, T_C=100 °C
		-	-	23		V_{GS}=10 V, T_A=25 °C, R_{thJA}=50 K/W[1)])
Pulsed drain current[2)]	$I_{D,pulse}$	-	-	400		T_C=25 °C
Avalanche current, single pulse[3)]	I_{AS}	-	-	50		
Avalanche energy, single pulse	E_{AS}	-	-	20	mJ	I_D=40 A,R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	
Power dissipation	P_{tot}	-	-	48	W	T_C=25 °C
		-	-	2.5		T_A=25 °C, R_{thJA}=50 K/W[1)])
Operating and storage temperature	T_j,T_{stg}	-55	-	150	°C	
IEC climatic category; DIN IEC 68-1		55/150/56				

1) Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

2) See figure 3 for more detailed information

3) See figure 13 for more detailed information

3 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	2.6	K/W	
		-	-	20		top
Device on PCB	R_{thJA}	-	-	50		6 cm^2 cooling area[1)]

1) Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air

4 Electrical characteristics

Electrical characteristics, at T_j=25 °C, unless otherwise specified.

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	30	-	-	V	V_{GS}=0 V, I_D=10mA
Breakdown voltage temperature coefficient	$dV_{(BR)DSS}/dT_j$	-	15	-	mV/k	I_D=10 mA, reference to 25°C
Gate threshold voltage	$V_{GS(th)}$	1.2	-	2		V_{DS}=V_{GS}, I_D=10 mA
Zero gate voltage drain current	I_{DSS}	-	-	0.5	mA	V_{DS}=24 V, V_{GS}=0 V, T_j=25 °C
		-	2	-		V_{DS}=24 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	3	3.7	mΩ	V_{GS}=4.5 V, I_D=30 A,
		-	2.3	2.8		V_{GS}=10 V, I_D=30 A,
Gate resistance	R_G	-	0.9	-	Ω	
Transconductance	g_{fs}	50	100	-	S	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=30 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	1500	-	pF	V_{GS}=0 V, V_{DS}=15 V, f=1 MHz
Output capacitance	C_{oss}	-	630	-		
Reverse transfer capacitance	C_{rss}	-	88	-		
Turn-on delay time	$t_{d(on)}$	-	3.9	-	ns	V_{DD}=15 V, V_{GS}=10 V, I_D=30 A, R_G= 1.6 Ω
Rise time	t_r	-	5.4	-		
Turn-off delay time	$t_{d(off)}$	-	20	-		
Fall time	t_f	-	3.8	-		

Table 6 Gate charge characteristics[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	4	-	nC	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 4.5 V
Gate charge at threshold	$Q_{g(th)}$	-	2.4	-		
Gate to drain charge	Q_{gd}	-	4	-		
Switching charge	Q_{sw}	-	5.6	-		
Gate charge total	Q_g	-	12.2	-		
Gate plateau voltage	$V_{plateau}$	-	2.6	-	V	
Gate charge total	Q_g	-	24	-	nC	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 10V
Gate charge total, sync. FET	$Q_{g(sync)}$	-	9.8	-		V_{DS}=0.1 V, V_{GS}=0 to 4.5 V
Output charge	Q_{oss}	-	17	-		V_{DD}=15 V, V_{GS}=0 V

1) See figure 16 for gate charge parameter definition

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	48	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	192		
Diode forward voltage	V_{SD}	-	0.54	0.7	V	V_{GS}=0 V, I_F=4 A, T_j=25 °C
Reverse recovery charge	Q_{rr}	-	5	-	nC	V_R=15V, I_F=4A, di_F/dt=400 A/µs

5 Electrical characteristics diagrams

Table 8

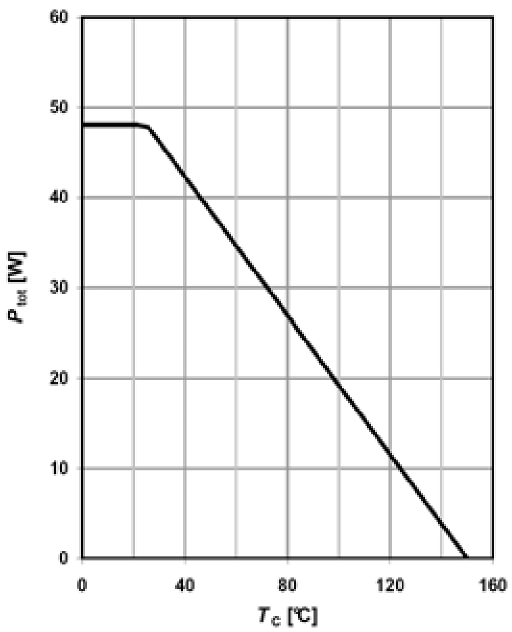
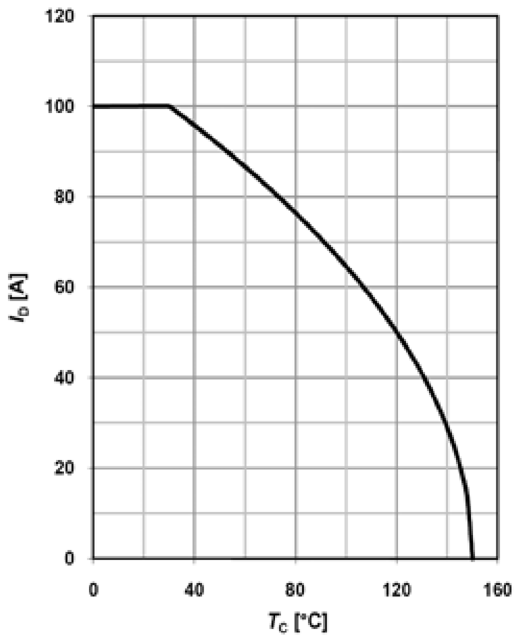
1 Power dissipation	**2 Drain current**
	
P_{tot} = f(T_C)	I_D=f(T_C); parameter:V_{GS}

Table 9

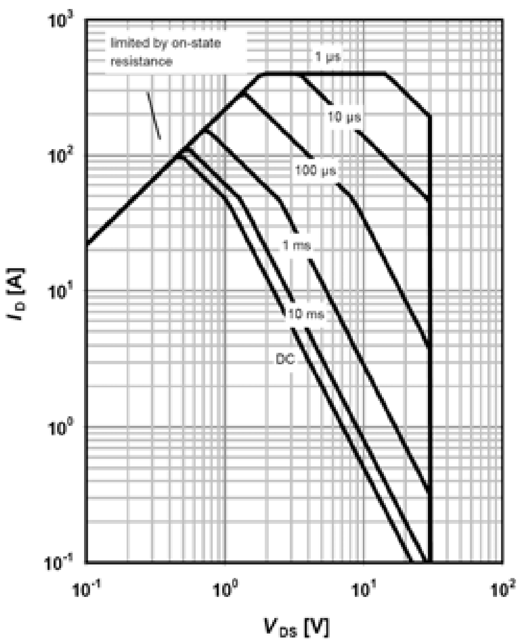
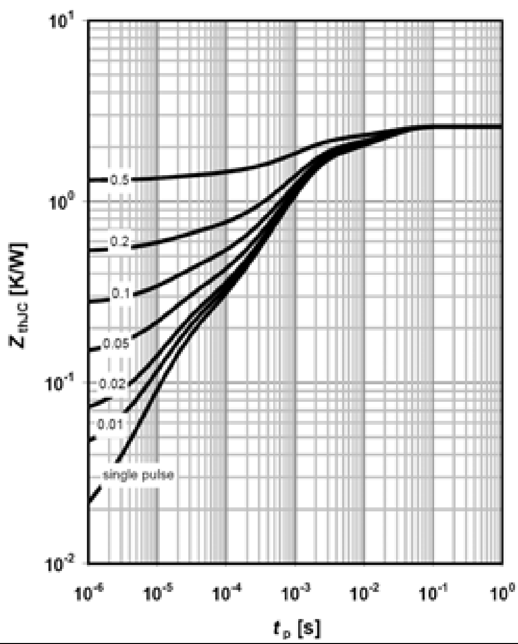
3 Safe operating area T_C=25 °C	**4 Max. transient thermal impedance**
	
I_D=f(V_{DS}); T_j=25 °C; D=0; parameter: T_p	$Z_{(thJC)}$=f(t_p); parameter: D=t_p/T

Table 10

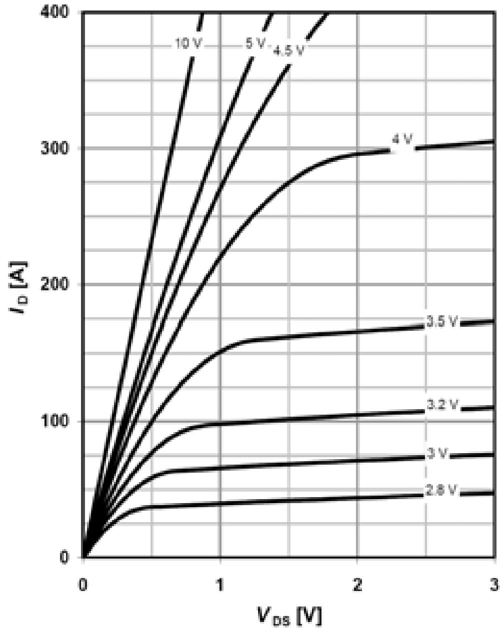
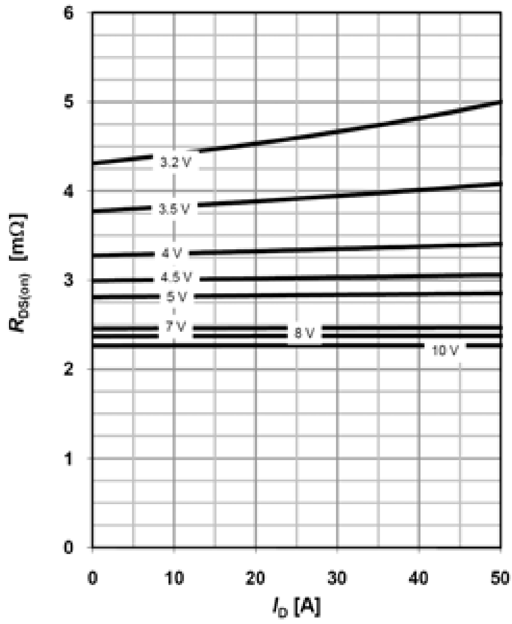
5 Typ. output characteristics T_C=25 °C	6 Typ. drain-source on-state resistance
	
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}	$R_{DS(on)}$=f(I_D); T_j=25 °C; parameter: V_{GS}

Table 11

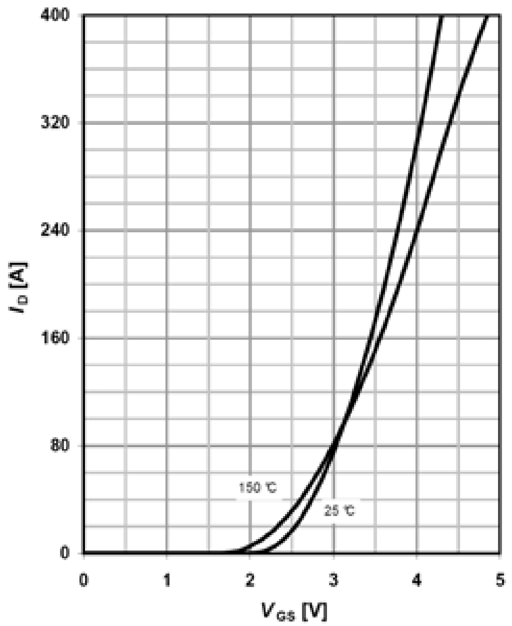
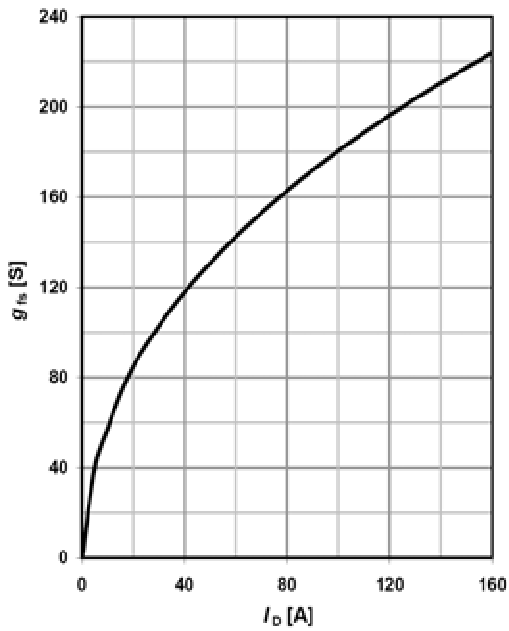
7 Typ. transfer characteristics	8 Typ. forward transconductance
	
I_D=f(V_{GS}); $\|V_{DS}\|$>2$\|I_D\|R_{DS(on)max}$	g_{fs}=f(I_D); T_j=25 °C

Table 12

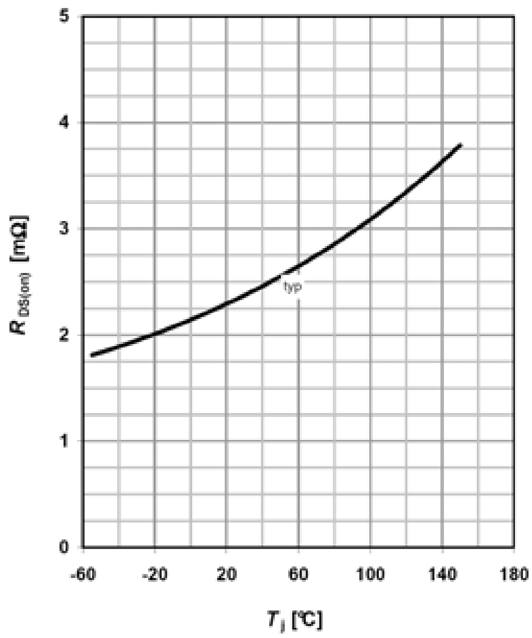
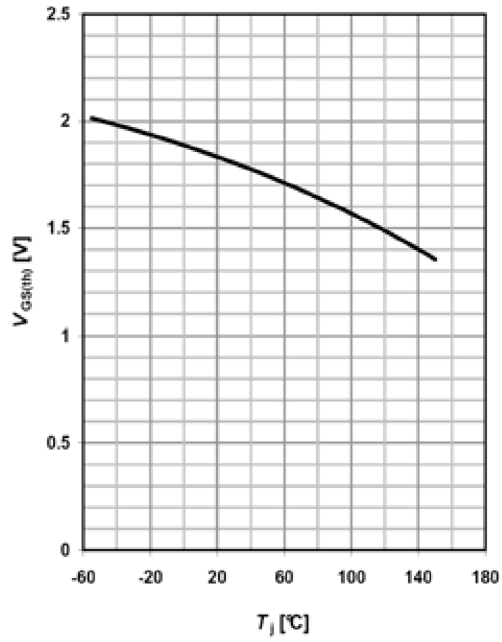
9 Drain-source on-state resistance	10 Typ. gate threshold voltage
	
$R_{DS(on)}$=f(T_j); I_D=30 A; V_{GS}=10 V	$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}; I_D=10 mA

Table 13

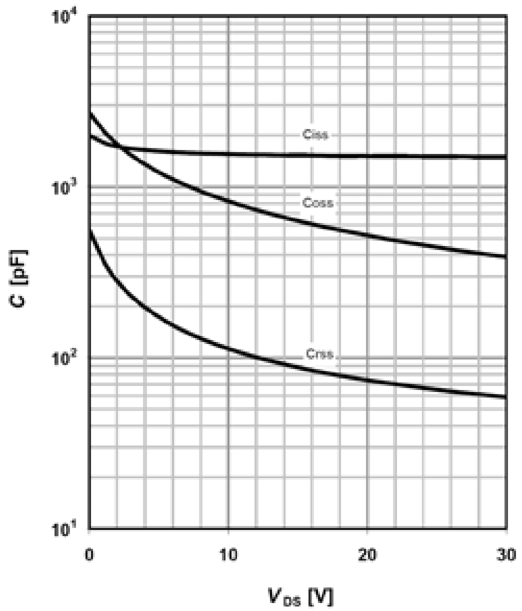
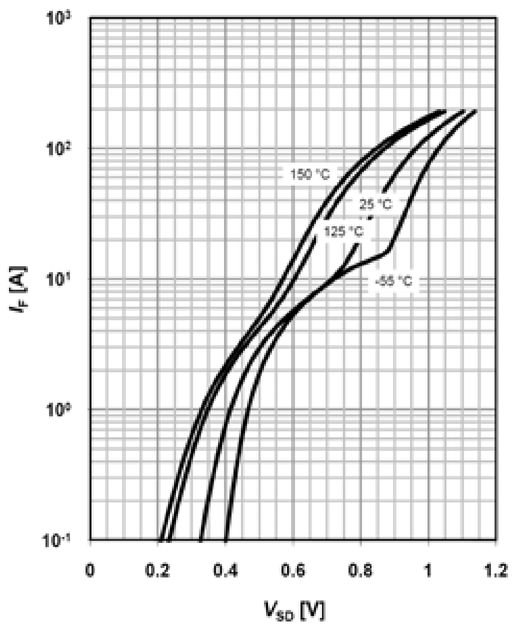
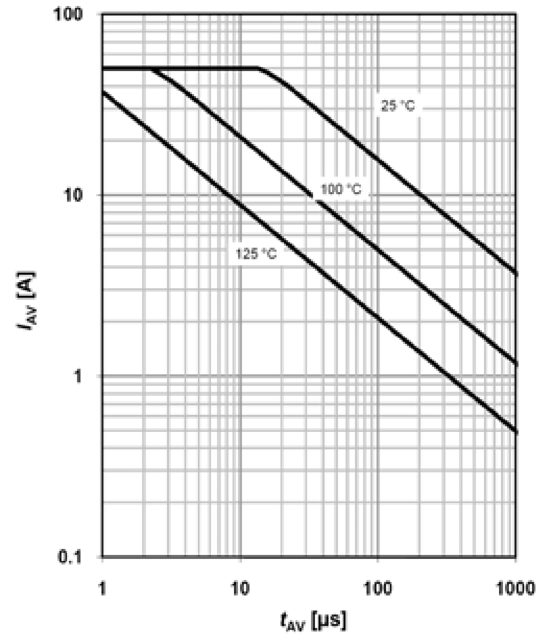
11 Typ. capacitances	12 Forward characteristics of reverse diode
	
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz	I_F=f(V_{SD}); parameter: T_j

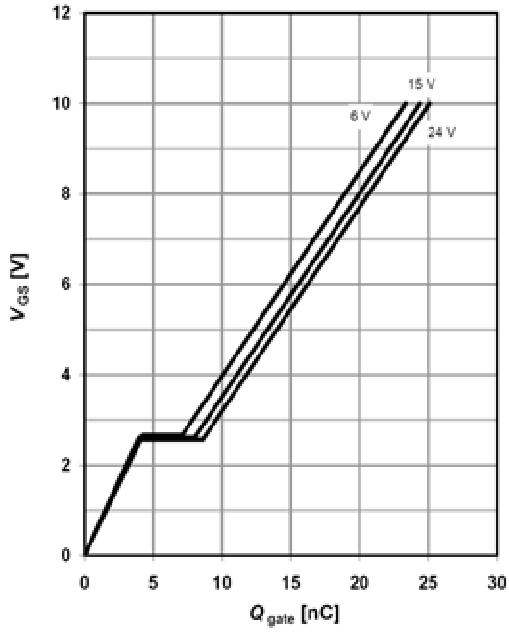
Table 14

13 Avalanche characteristics



I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j(start)}$

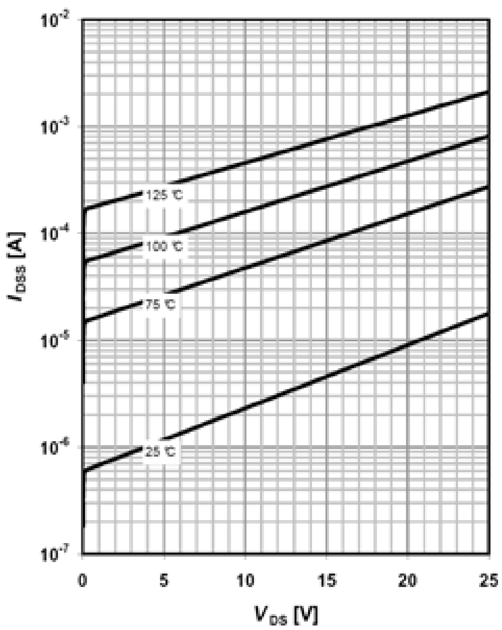
14 Typ. gate charge



V_{GS}=f(Q_{gate}); I_D=30 A pulsed; parameter: V_{DD}

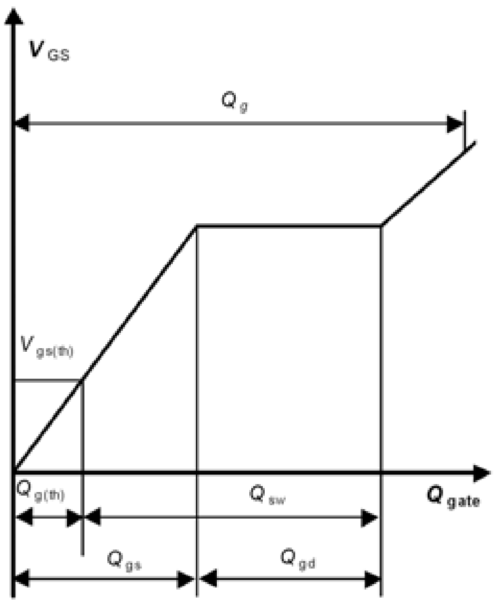
Table 15

15 Typ. drain-source leakage current

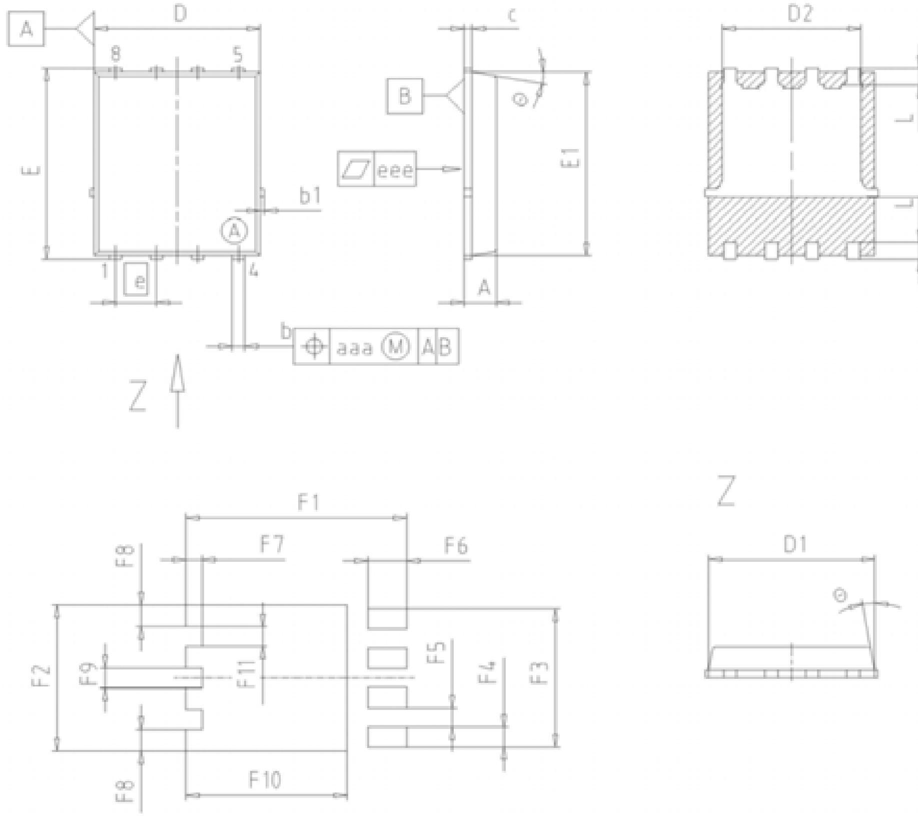


I_{DSS}=f(V_{DS}); V_{GS}=0 V

16 Gate charge waveforms



6 Package outline



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.90	1.10	0.035	0.043
b	0.34	0.54	0.013	0.021
b1	0.02	0.22	0.001	0.008
c	0.15	0.35	0.006	0.014
D=D1	4.95	5.35	0.195	0.211
D2	4.20	4.40	0.165	0.173
E	5.95	6.35	0.234	0.250
E1	5.70	6.10	0.224	0.240
E2	3.40	3.80	0.134	0.150
e	1.27		0.050	
N	8		8	
L	0.45	0.65	0.018	0.026
□	8.5°	11.5°	8.5°	11.5°
aaa	0.25		0.010	
eee	0.05		0.002	
F1	6.75	6.95	0.266	0.274
F2	4.60	4.80	0.181	0.189
F3	4.36	4.56	0.172	0.180
F4	0.55	0.75	0.022	0.030
F5	0.52	0.72	0.020	0.028
F6	1.10	1.30	0.043	0.051
F7	0.40	0.60	0.016	0.024
F8	0.60	0.80	0.024	0.031
F9	0.53	0.73	0.021	0.029
F10	4.90	5.10	0.193	0.201
F11	0.53	0.73	0.021	0.029

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SCALE

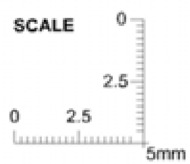

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Figure 1 Outlines PG-TDSON-8, dimensions in mm/inches

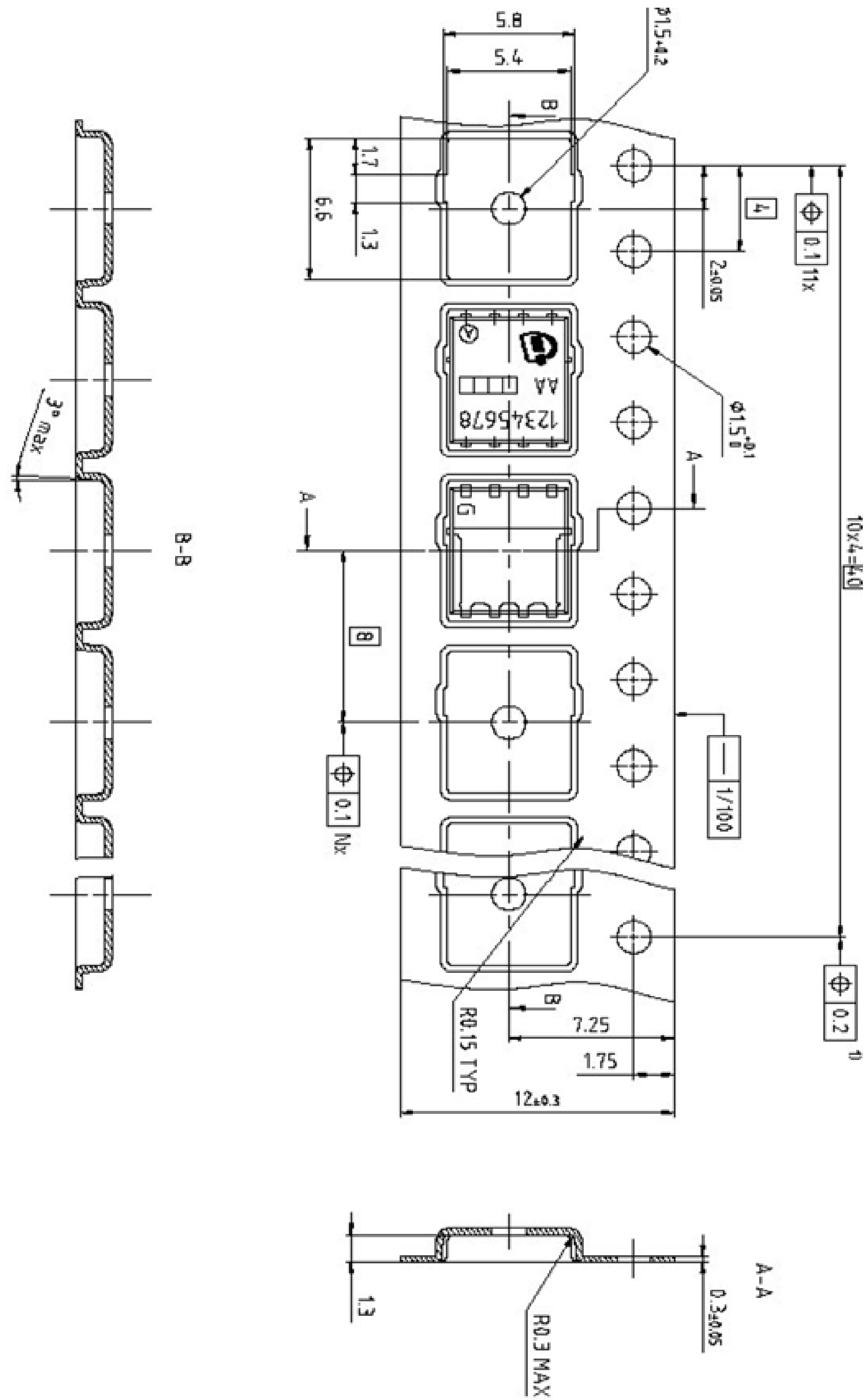

Figure 2 **Outlines PG-TDSON-8 tape, dimension in mm/inches**

7 Revision History

Revision History: 2011-06-10, 2.1

Previous Revision:	
Revision	**Subjects (major changes since last revision)**
0.1	Release of target data sheet
2.0	Release of Final data sheet
2.1	Update schematic

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