TOSHIBA Field-Effect Transistor Silicon P-Channel MOS Type

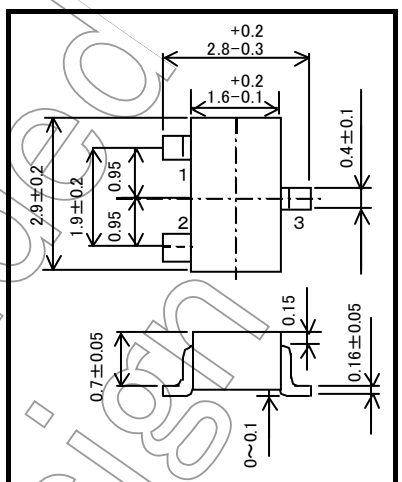
SSM3J317T

○ Power Management Switch Applications

○ High-Speed Switching Applications

- 1.8-V drive
- Low ON-resistance: R_{on} = 306 mΩ (max) (@V_{GS} = -1.8 V)
  : R_{on} = 144 mΩ (max) (@V_{GS} = -2.8 V)
  : R_{on} = 107 mΩ (max) (@V_{GS} = -4.5 V)

Unit: mm



JEDEC	—
JEITA	—
TOSHIBA	2-3S1A

Weight: 10 mg (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-Source voltage		V_{DSS}	-20	V
Gate-Source voltage		V_{GSS}	±8	V
Drain current	DC	I_D (Note 1)	-3.6	A
	Pulse	I_{DP} (Note 1)	-7.2	
Drain power dissipation		P_D (Note 2)	700	mW
		t = 5s	1400	
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: The junction temperature should not exceed 150°C during use.

Note 2: Mounted on an FR4 board. (25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 645 mm^2)

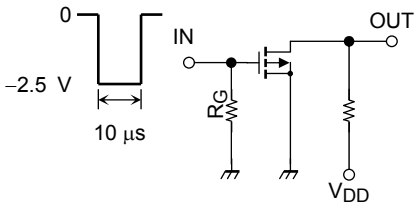
Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Conditions	Min	Typ.	Max	Unit
Drain-Source breakdown voltage		$V_{(BR)\ DSS}$	I_D = -1 mA, V_{GS} = 0 V	-20	—	—	V
		$V_{(BR)\ DSX}$	I_D = -1 mA, V_{GS} = 8 V	-12	—	—	
Drain cut-off current		I_{DSS}	V_{DS} = -20 V, V_{GS} = 0 V	—	—	-10	μA
Gate leakage current		I_{GSS}	V_{GS} = ±8 V, V_{DS} = 0 V	—	—	±1	μA
Gate threshold voltage		V_{th}	V_{DS} = -3 V, I_D = -1 mA	-0.3	—	-1.0	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = -3 V, I_D = -1.0 A (Note 3)	2.2	4.4	—	S
Drain–source ON-resistance		$R_{DS\ (ON)}$	I_D = -1.0 A, V_{GS} = -4.5 V (Note 3)	—	83	107	mΩ
			I_D = -0.75 A, V_{GS} = -2.8 V (Note 3)	—	107	144	
			I_D = -0.5 A, V_{GS} = -1.8 V (Note 3)	—	170	306	
Input capacitance		C_{iss}	V_{DS} = -10 V, V_{GS} = -0 V, f = 1 MHz	—	390	—	pF
Output capacitance		C_{oss}		—	67	—	
Reverse transfer capacitance		C_{rss}		—	55	—	
Total Gate Charge		Q_g	V_{DS} = -10 V, I_{DS}= -3.6 A V_{GS} = -4 V	—	9.6	—	nC
Gate-Source Charge		Q_{gs}		—	6.6	—	
Gate-Drain Charge		Q_{gd}		—	3.0	—	
Switching time	Turn-on time	t_{on}	V_{DD} = -10 V, I_D = -1.0 A V_{GS} = 0 to -2.5 V, R_G = 4.7 Ω	—	17	—	ns
	Turn-off time	t_{off}		—	19.5	—	
Drain-Source forward voltage		V_{DSF}	I_D = 3.6 A, V_{GS} = 0 V (Note 3)	—	0.9	1.2	V

Note3: Pulse test

Switching Time Test Circuit

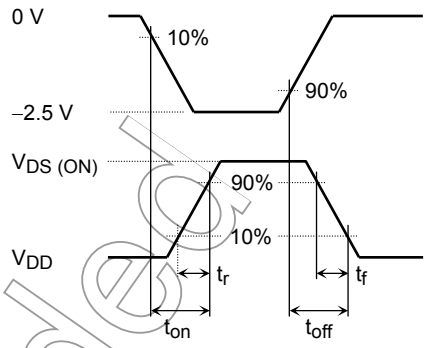
(a) Test Circuit



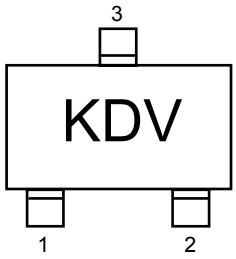
V_{DD} = −10 V
R_G = 4.7Ω
D.U. ≤ 1%
V_{IN}: t_r, t_f < 5 ns
Common Source
Ta = 25°C

(b) V_{IN}

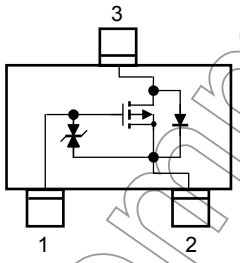
(c) V_{OUT}



Marking



Equivalent Circuit (top view)



Usage Considerations

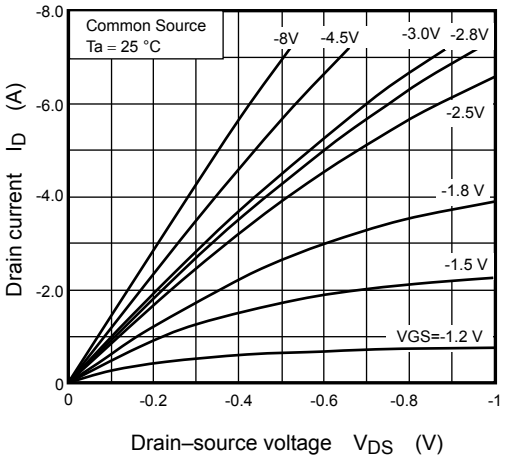
Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to below (−1 mA for the Q2 of the SSM3J317T). Then, for normal switching operation, $V_{GS(on)}$ must be higher than V_{th}, and $V_{GS(off)}$ must be lower than V_{th}. This relationship can be expressed as: $V_{GS(off)} < V_{th} < V_{GS(on)}$.

Take this into consideration when using the device.

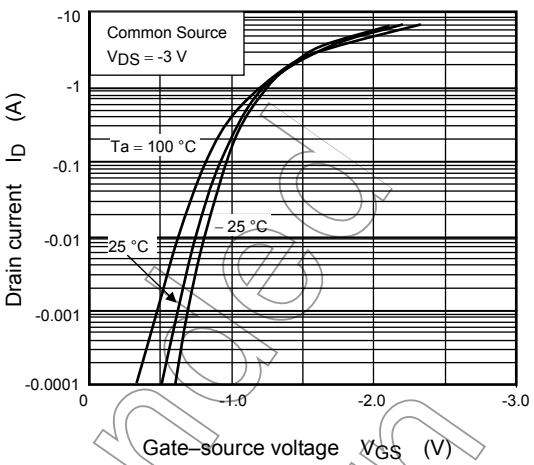
Handling Precaution

When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

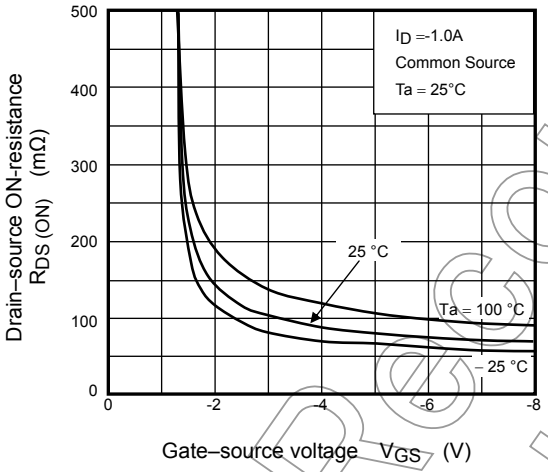
$I_D - V_{DS}$



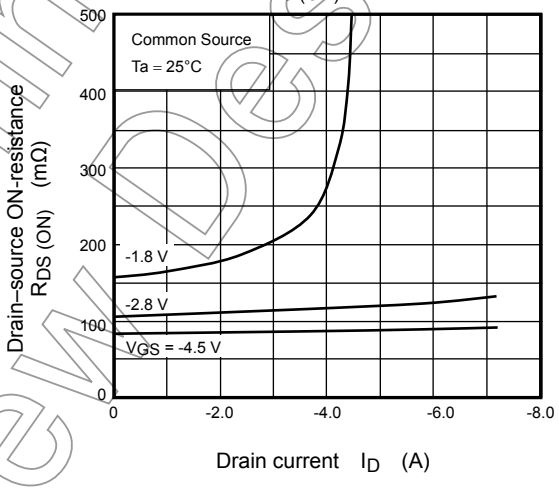
$I_D - V_{GS}$



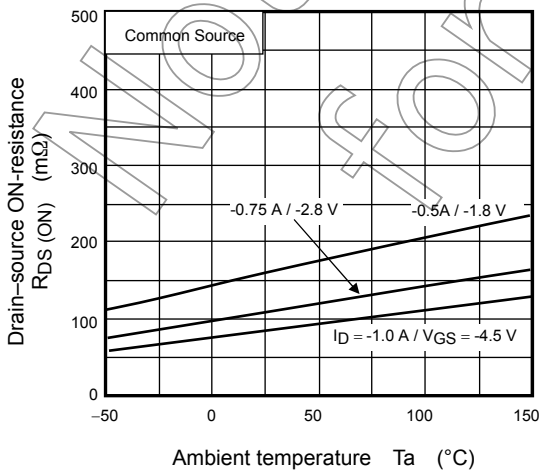
$R_{DS\ (ON)} - V_{GS}$



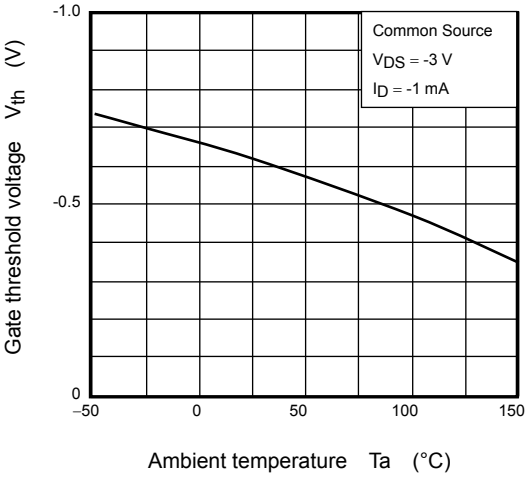
$R_{DS\ (ON)} - I_D$

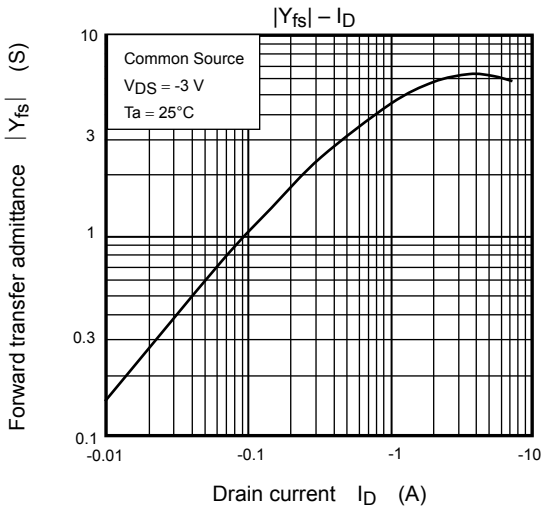


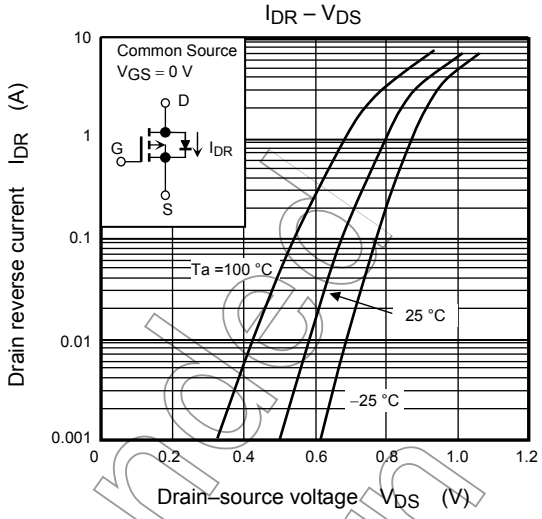
$R_{DS\ (ON)} - Ta$

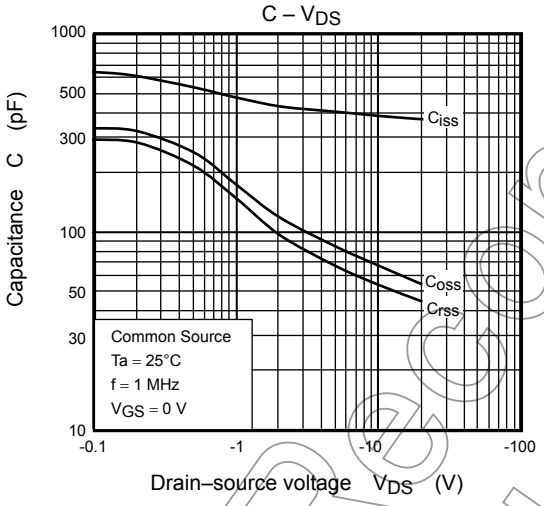


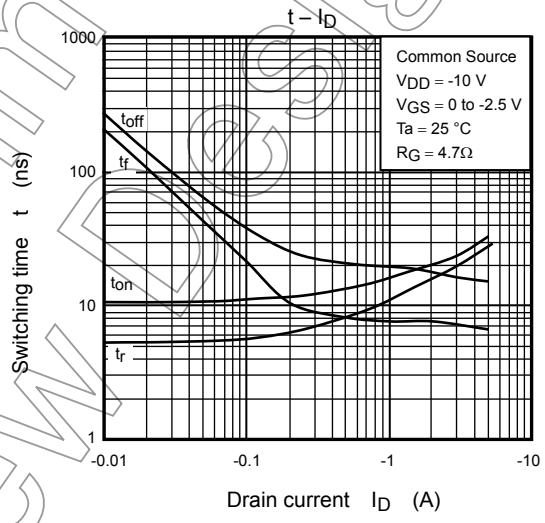
$V_{th} - Ta$

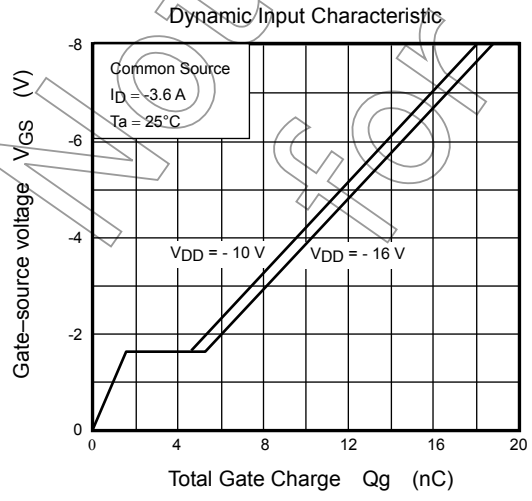




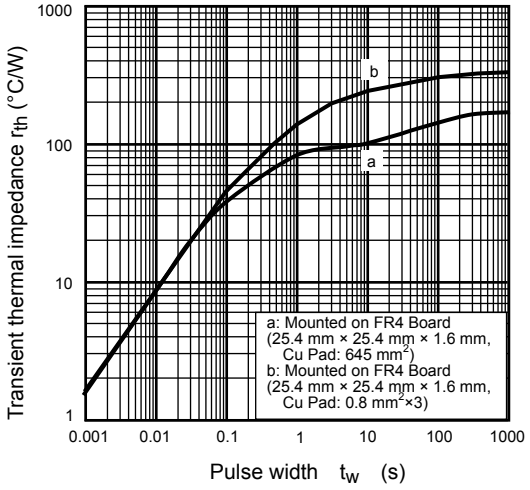




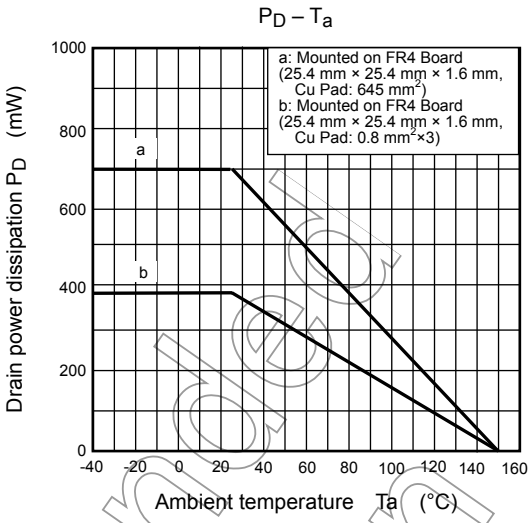




$r_{th} - t_w$



$P_D - T_a$



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