STH250N55F3-6

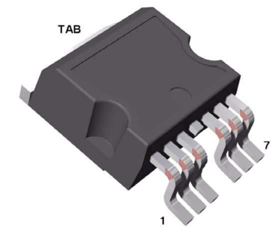
N-channel 55 V, 2.2 mΩ, 180 A, H²PAK STripFET™ III Power MOSFET

Features

Order code	V_{DSS}	$R_{DS(on)}$ max.	I_D	Pw
STH250N55F3-6	55 V	2.6 mΩ	180 A(1)	300 W

1. Value limited by package

- Ultra low on-resistance
- 100% avalanche tested



H²PAK-6I

Application

Switching applications

Description

This N-channel STripFET™ III Power MOSFET technology is among the latest improvements, which have been especially tailored to minimize on-state resistance providing superior switching performance.

Figure 1. Internal schematic diagram

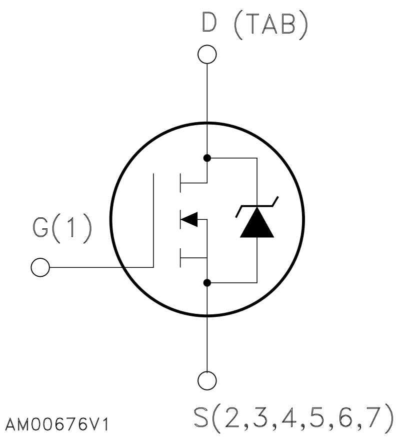


Table 1. Device summary

Order code	Marking	Package	Packaging
STH250N55F3-6	250N55F3	H²PAK	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS}=0)	55	V
V_{GS}	Gate-source voltage	± 20	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	180	A
I_D (1)	Drain current (continuous) at T_C=100 °C	160	A
I_{DM} (2)	Drain current (pulsed)	720	A
P_{TOT}	Total dissipation at T_C = 25 °C	300	W
	Derating factor	2.0	W/°C
dv/dt (3)	Peak diode recovery voltage slope	11	V/ns
E_{AS} (4)	Single pulse avalanche energy	1000	mJ
T_j T_{stg}	Operating junction temperature storage temperature	- 55 to 175	°C

1. Current limited by package.
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq 120$ A, di/dt ≤ 900 A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq T_{JMAX}$
4. Starting Tj = 25 °C, I_D = 60 A, V_{DD} = 40 V *(see Figure 16 and Figure 17)*

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.5	°C/W
$R_{thj-pcb}$ (1)	Thermal resistance junction-ambient max	35	°C/W

1. When mounted on FR-4 board, on 1inch², 2oz Cu.

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS}= 0	55			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS}= max rating, V_{DS}= max rating, @125°C			10 100	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±200	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10 , I_D= 60 A		2.2	2.6	mΩ

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0	-	6800 1450 15	-	pF pF pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 27.5 V, I_D = 60 A R_G = 4.7 Ω V_{GS} = 10 V (see *Figure 13*, *Figure 18*)	-	25 150 110 50	-	ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 44 V, I_D = 120 A, V_{GS} = 10 V, (see *Figure 14*)	-	100 30 26	-	nC nC nC

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}[1]	Source-drain current Source-drain current (pulsed)		-		180 720	A A
V_{SD}[2]	Forward on voltage	I_{SD}=120 A, V_{GS}=0	-		1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}=120 A, di/dt = 100 A/µs, V_{DD} = 35 V, Tj=150 °C (see *Figure 15*)	-	60 0.11 3.5		ns µC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

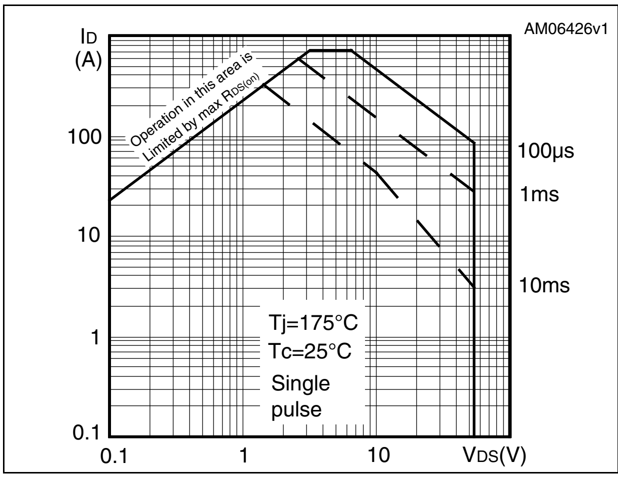


Figure 3. Thermal impedance

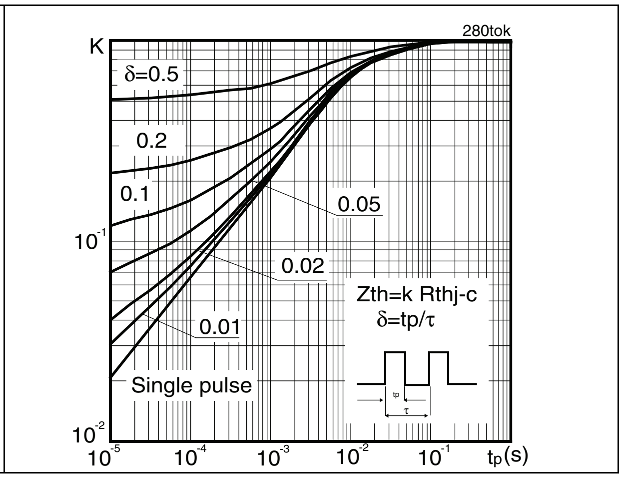


Figure 4. Output characteristics

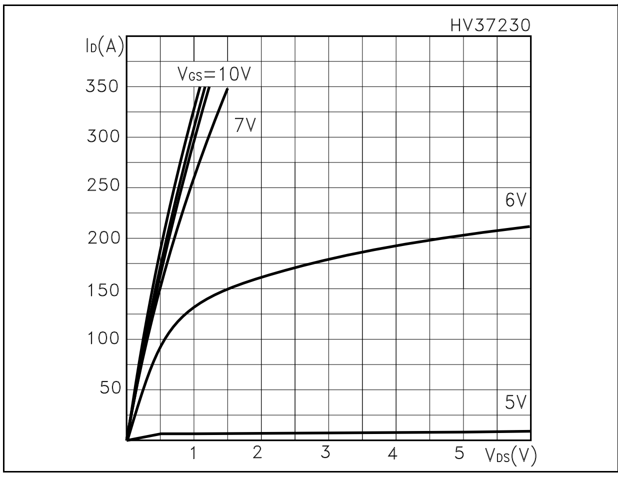


Figure 5. Transfer characteristics

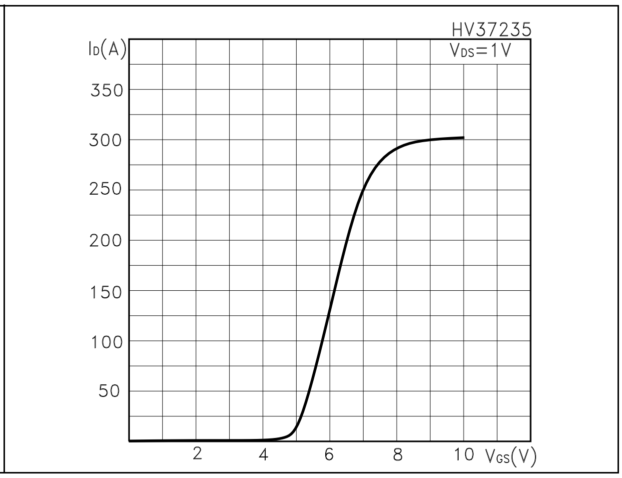


Figure 6. Normalized B_{VDSS} vs temperature

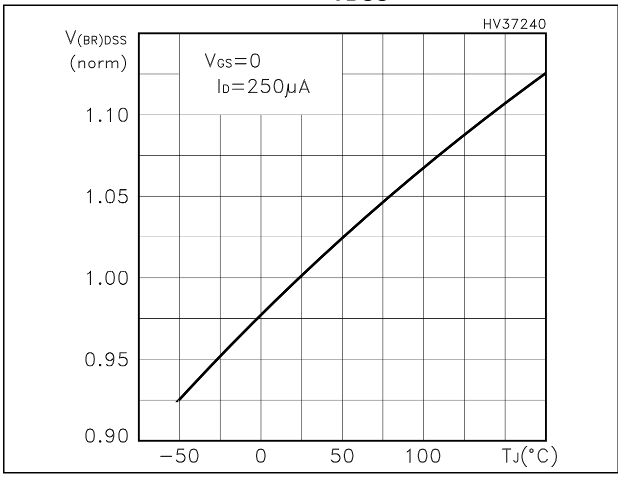


Figure 7. Static drain-source on resistance

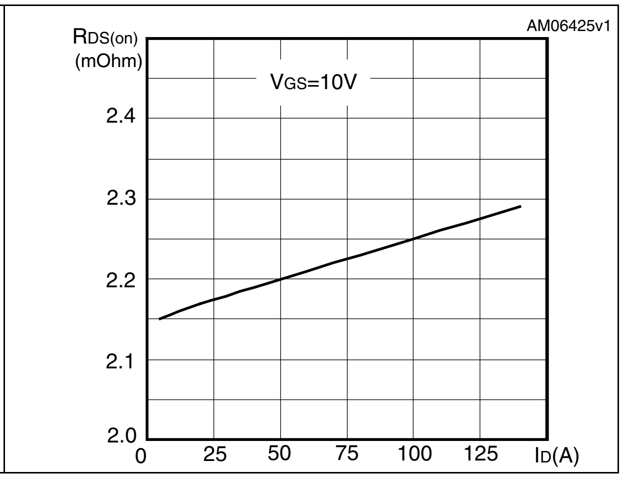


Figure 8. Gate charge vs gate-source voltage

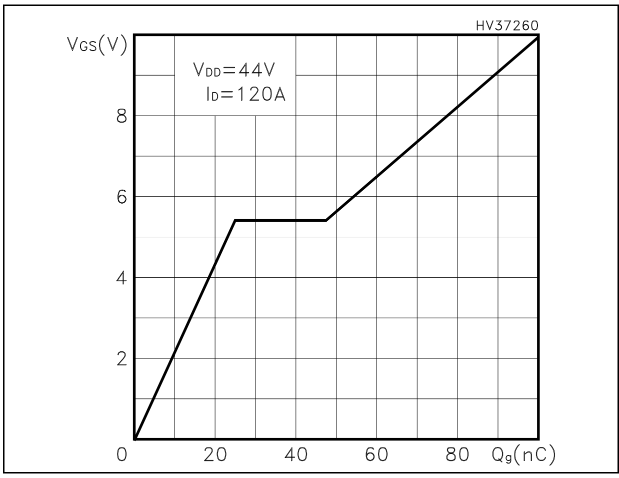


Figure 9. Capacitance variations

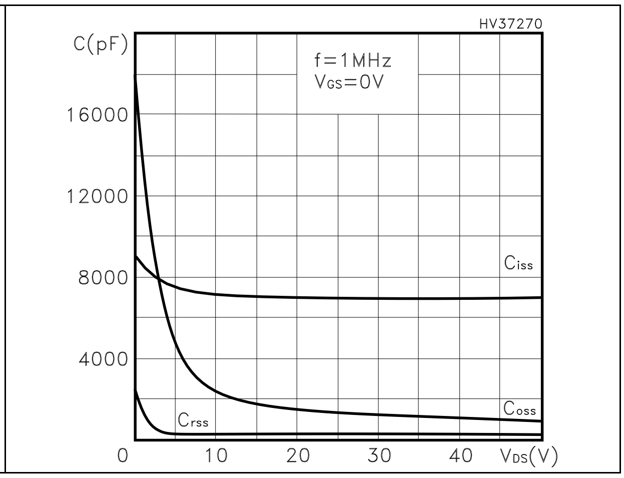


Figure 10. Normalized gate threshold voltage vs temperature

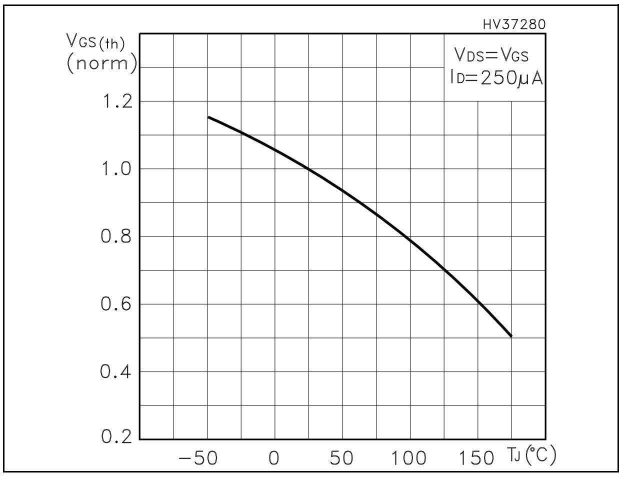


Figure 11. Normalized on resistance vs temperature

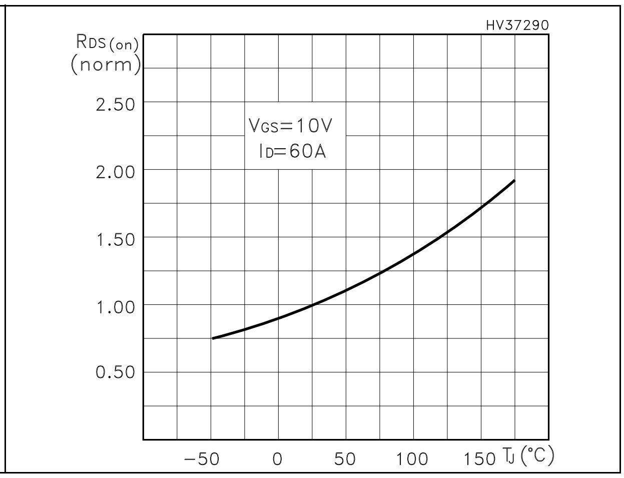
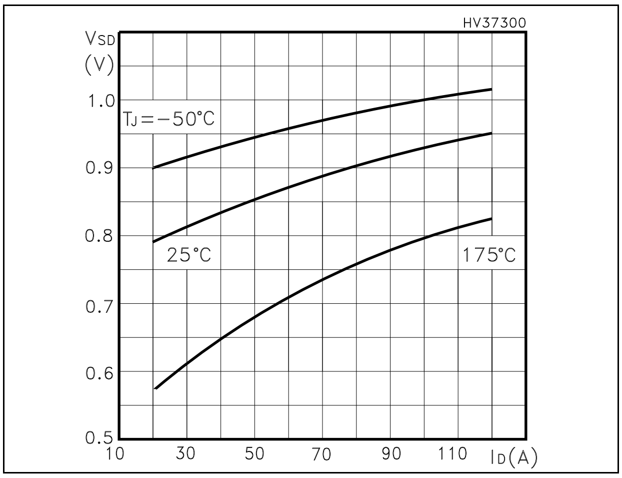


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

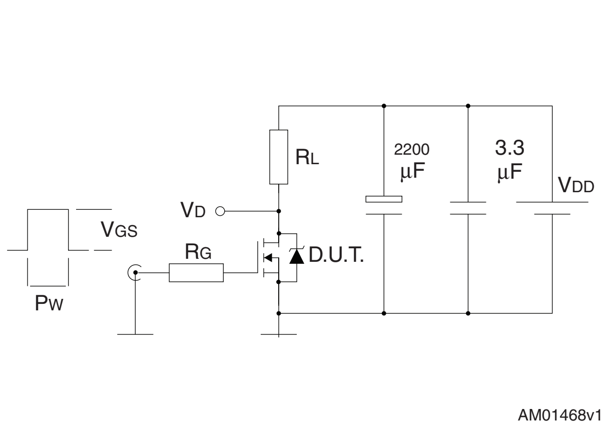


Figure 14. Gate charge test circuit

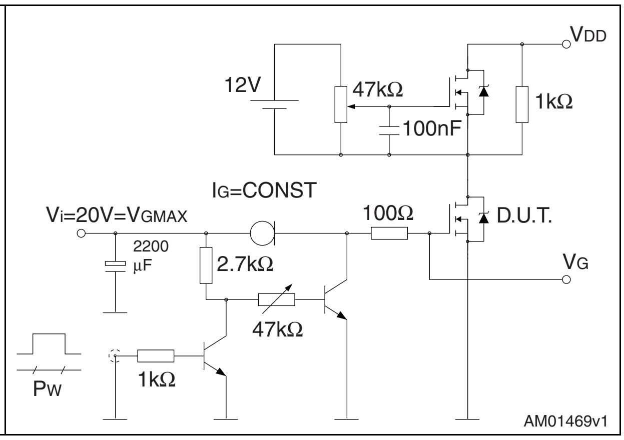


Figure 15. Test circuit for inductive load switching and diode recovery times

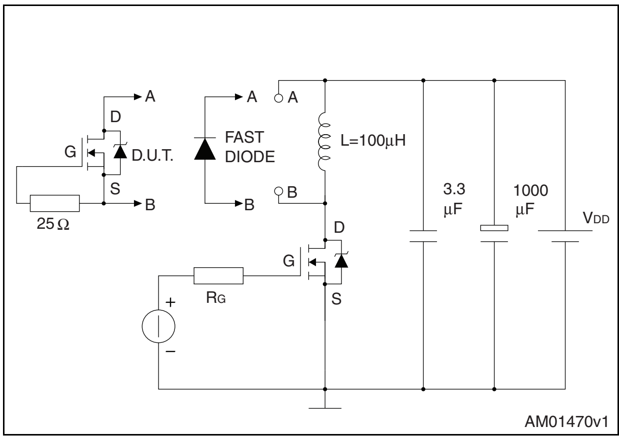


Figure 16. Unclamped inductive load test circuit

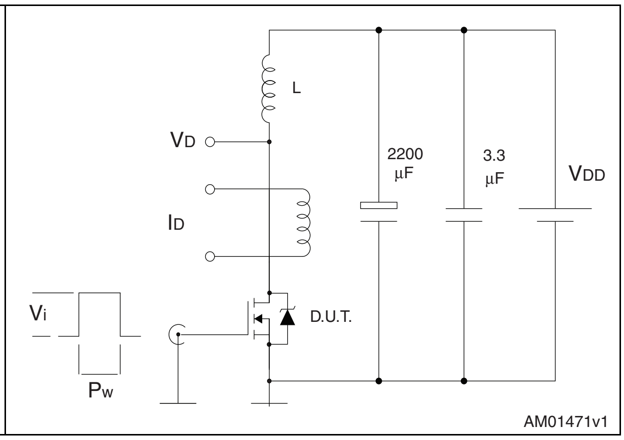


Figure 17. Unclamped inductive waveform

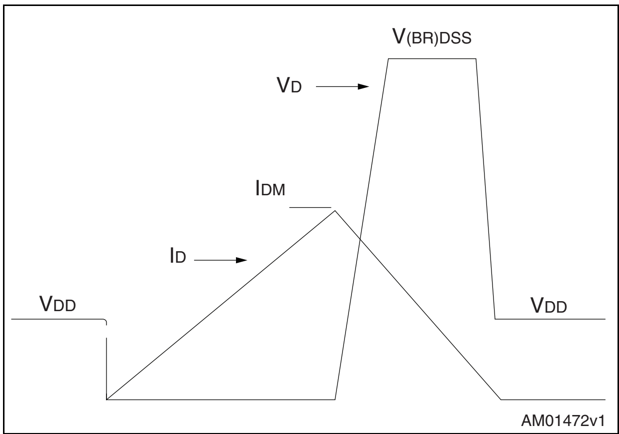
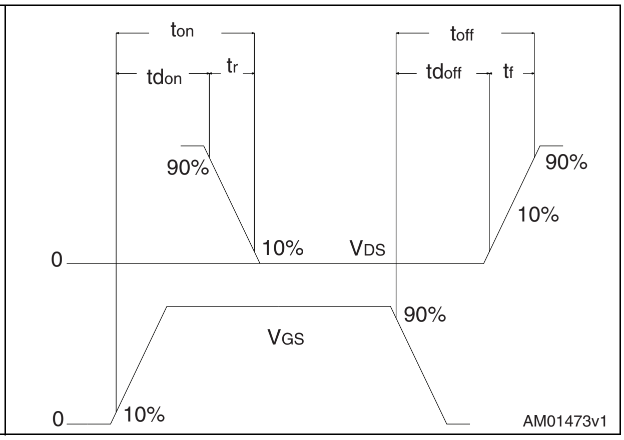


Figure 18. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 7. H²PAK-6 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30	-	4.80
A1	0.03		0.20
C	1.17		1.37
e	2.34		2.74
e1	4.88		5.28
e2	7.42		7.82
E	0.45		0.60
F	0.50		0.70
H	10.00		10.40
H1	7.80		8.20
L	14.75		15.25
L1	1.27		1.40
L2	4.35		4.95
L3	7.45		7.85
L4	1.5		1.75
M	1.90		2.50
R	0.20		0.60
V	0°		8°

Figure 19. H²PAK-6 drawing

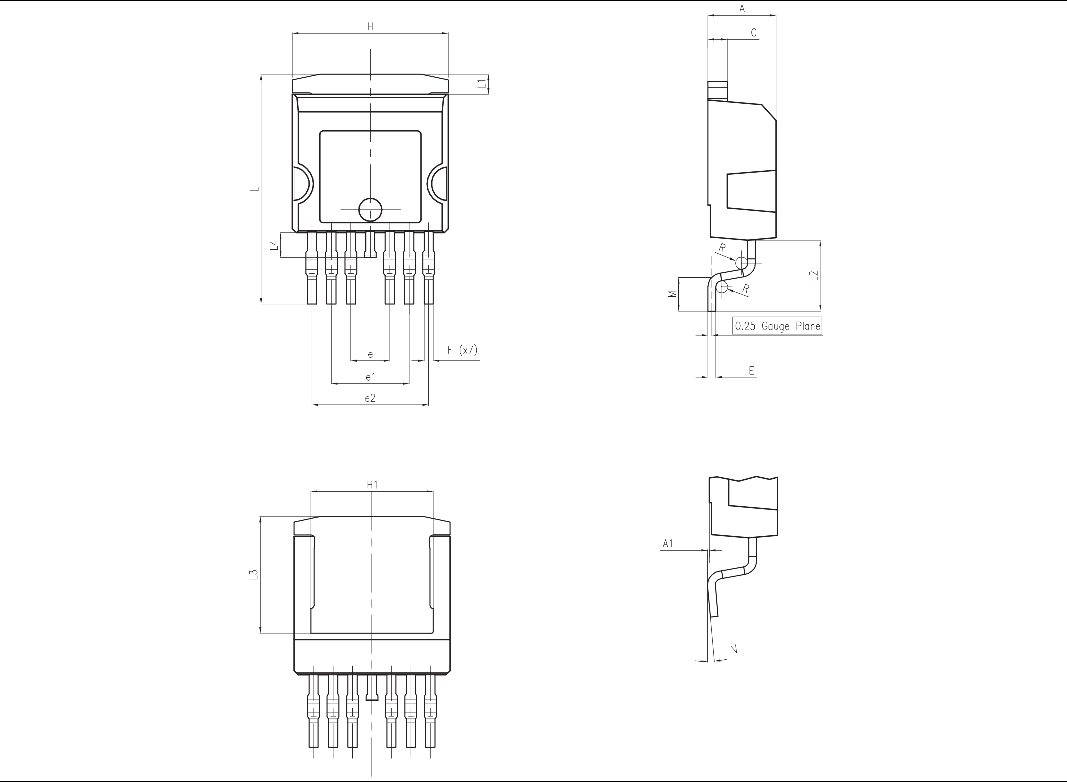
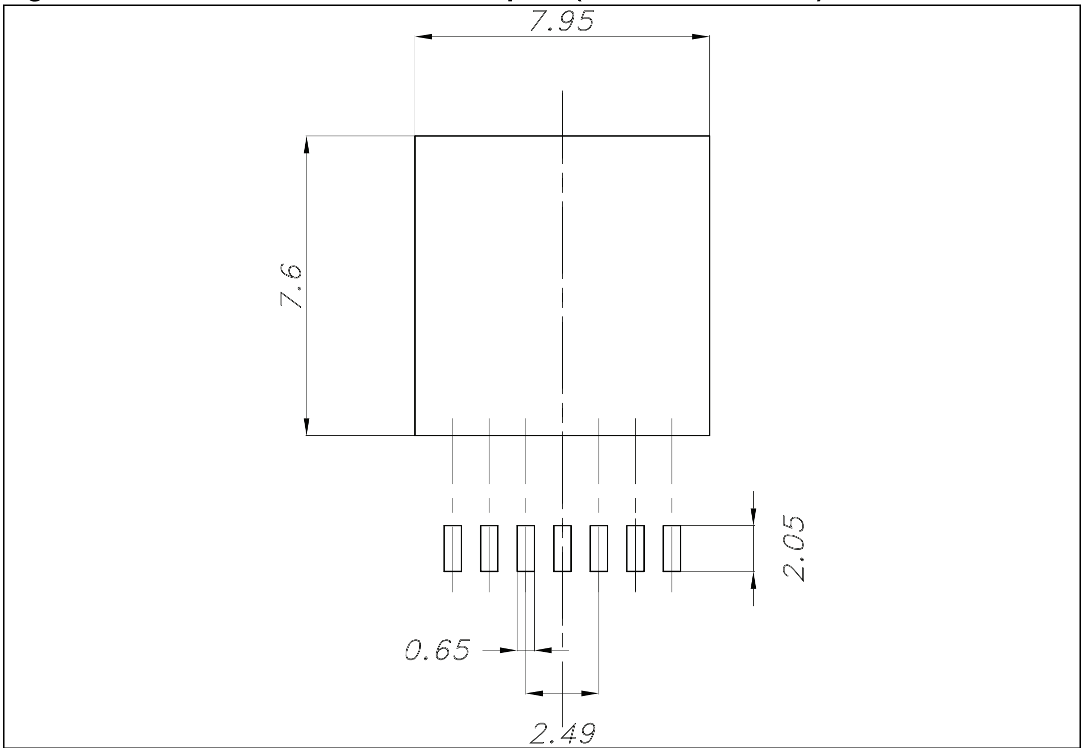
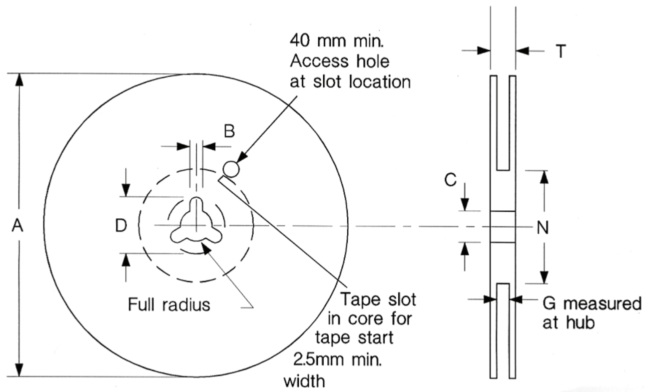


Figure 20. H²PAK-6 recommended footprint (dimensions in mm)



5 Packaging mechanical data

Figure 21. H²PAK-6 tape and reel



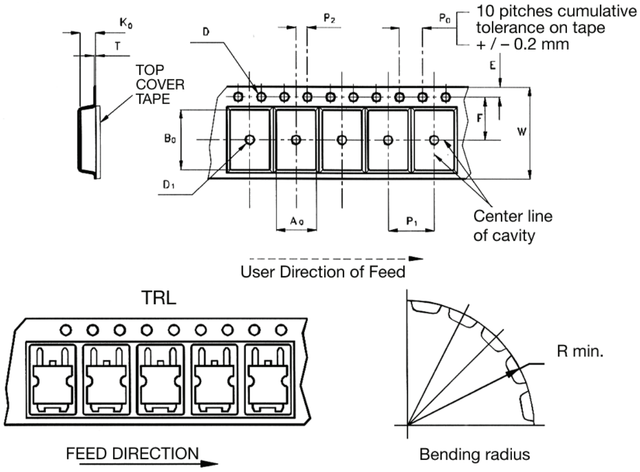
REEL MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0795	
G	24.4	26.4	0.960	1.039
N	100		3.937	
T		30.4		1.197

BASE QTY	BULK QTY
1000	1000

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	10.5	10.7	0.413	0.421
B0	15.7	15.9	0.618	0.626
D	1.5	1.6	0.059	0.063
D1	1.59	1.61	0.062	0.063
E	1.65	1.85	0.065	0.073
F	11.4	11.6	0.449	0.456
K0	4.8	5.0	0.189	0.197
P0	3.9	4.1	0.153	0.161
P1	11.9	12.1	0.468	0.476
P2	1.9	2.1	0.075	0.082
R	50		1.574	
T	0.25	0.35	0.0098	0.0137
W	23.7	24.3	0.933	0.956



6 Revision history

Table 8. Revision history

Date	Revision	Changes
01-Oct-2010	1	First release

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