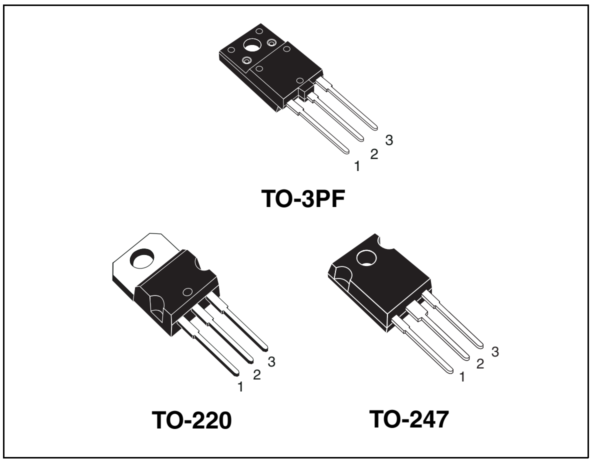
STFW6N120K3
STP6N120K3, STW6N120K3

N-channel 1200 V, 1.95 Ω, 6 A, TO-3PF, TO-220, TO-247
Zener-protected SuperMESH3™ Power MOSFET

Features

Type	V_{DSS}	$R_{DS(on)}$ max	I_D	Pw
STFW6N120K3	1200 V	< 2.4 Ω	6 A	63
STP6N120K3	1200 V	< 2.4 Ω	6 A	150 W
STW6N120K3	1200 V	< 2.4 Ω	6 A	150 W

- 100% avalanche tested
- Extremely large avalanche performance
- Gate charge minimized
- Very low intrinsic capacitances
- Zener-protected



Application

- Switching applications

Description

These devices are an N-channel SuperMESH™ Power MOSFET obtained through optimization of ST's well-established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special attention has been taken to ensure a very good dynamic performance coupled with a very large avalanche capability for the most demanding application.

Figure 1. Internal schematic diagram

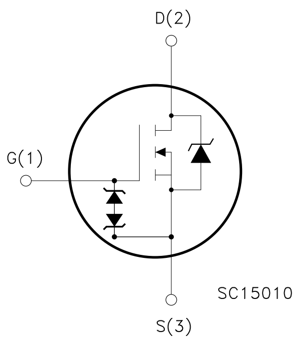


Table 1. Device summary

Order codes	Marking	Package	Packaging
STFW6N120K3	6N120K3	TO-3PF	Tube
STP6N120K3		TO-220	
STW6N120K3		TO-247	

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value			Unit
		TO-3PF	TO-220	TO-247	
V_{GS}	Gate- source voltage	30			V
I_D	Drain current (continuous) at T_C = 25 °C	6			A
I_D	Drain current (continuous) at T_C = 100 °C	3.8			A
I_{DM} (1)	Drain current (pulsed)	20			A
P_{TOT}	Power dissipation at T_C = 25 °C	63	150	150	W
I_{AR}	Max current during repetitive or single pulse avalanche (pulse width limited by T_{JMAX})	7			A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	180			mJ
$V_{ESD(G-S)}$	G-S ESD (HBM-C = 100 pF, R = 1.5 kΩ)	6000			V
V_{ISO}	Insulation withstand voltage (AC)	3500	-	-	V
T_{stg}	Storage temperature	-55 to 150			°C
T_J	Operating junction temperature				

1. Pulse width limited by safe operating area

Table 3. Thermal data

Symbol	Parameter	TO-3PF	TO-220	TO-247	Unit
$R_{thj-case}$	Thermal resistance junction-case	1.98	0.83		°C/W
$R_{thj-pcb}$	Thermal resistance junction to pcb minimum footprint	-	-	-	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max	50	62.5	50	°C/W
T_J	Maximum lead temperature for soldering purpose	300			°C

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4. On / off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	1200	-	-	V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating V_{DS} = Max rating, T_J = 125 °C	-	-	1 50	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V, V_{DS} = 0	-	-	± 10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 2.5 A	-	1.95	2.4	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0	-	1050 90 1	-	pF pF pF
$C_{o(tr)}$ (1)	Equivalent capacitance time related	V_{GS} = 0, V_{DS} = 0 to 960 V	-	40	-	pF
$C_{o(er)}$ (2)	Equivalent capacitance energy related	V_{GS} = 0, V_{DS} = 0 to 960 V	-	25	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	3	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 960 V, I_D = 7.2 A, V_{GS} = 10 V (see *Figure 20*)	-	34 7 23	-	nC nC nC

1. C_{oss} eq. time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.
2. C_{oss} eq. energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 6. Switching times on/off

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off-delay time Fall time	V_{DD} = 600 V, I_D = 3.6 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 19*)	-	30 12 58 32	-	ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)		-	-	6 20	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 5 A, V_{GS} = 0	-	--	1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 7.2 A, di/dt = 100 A/µs V_{DD} = 60 V T_J = 25 °C (see *Figure 24*)	-	580 7 25	-	ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 7.2 A, di/dt = 100 A/µs V_{DD} = 60 V, T_J = 150 °C (see *Figure 24*)	-	840 9 22	-	ns µC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-source breakdown voltage	I_{GS} = ± 1 mA (open drain)	30	-	-	V

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-3PF

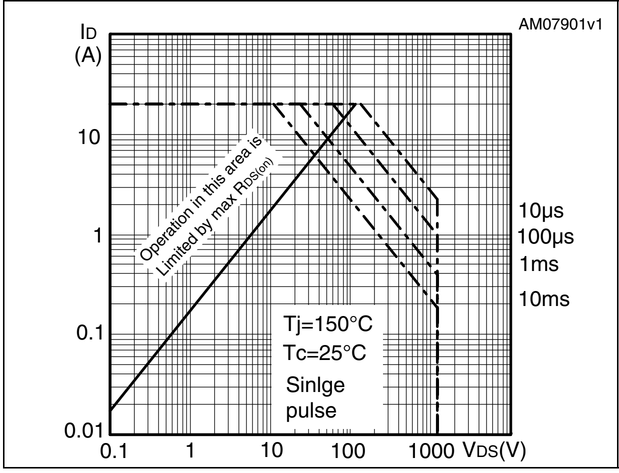


Figure 3. Thermal impedance for TO-3PF

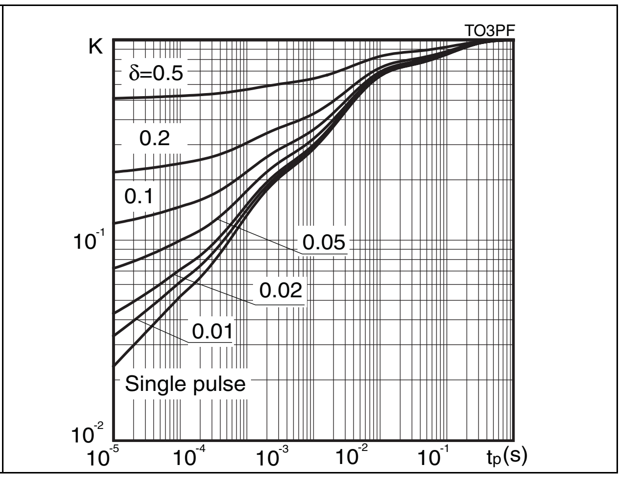


Figure 4. Safe operating area for TO-220

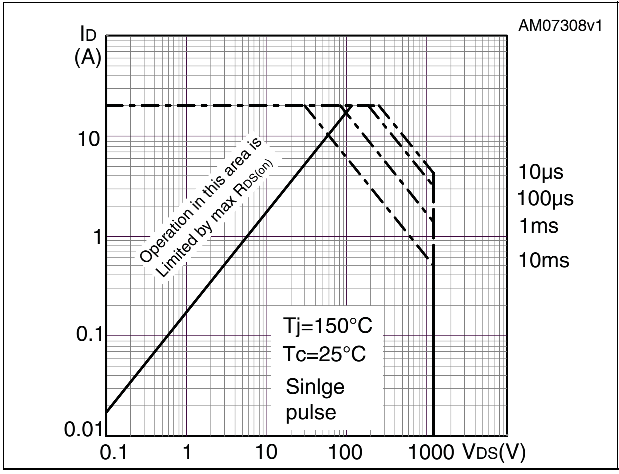


Figure 5. Thermal impedance for TO-220

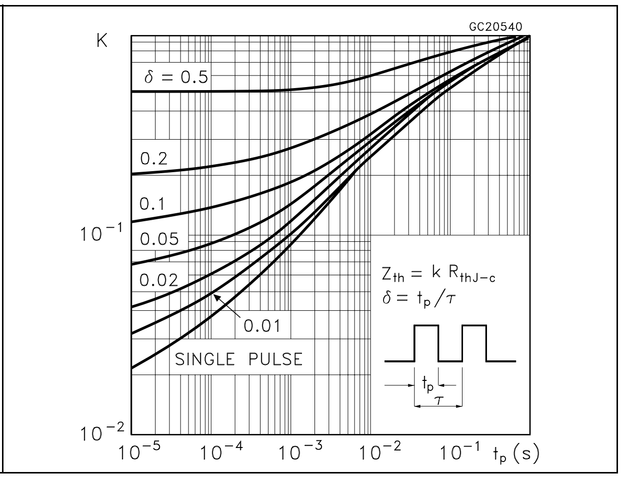


Figure 6. Safe operating area for TO-247

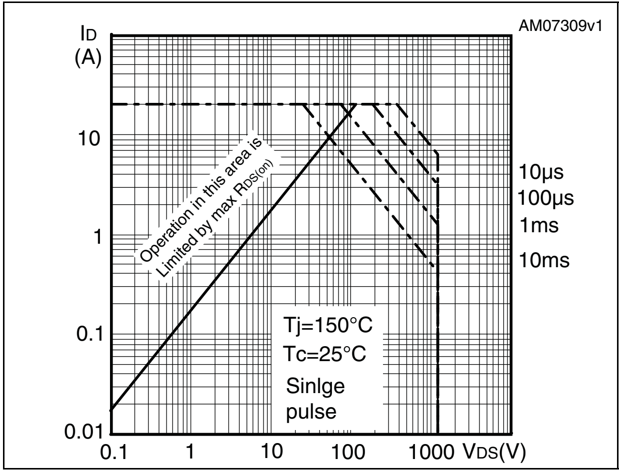


Figure 7. Thermal impedance for TO-247

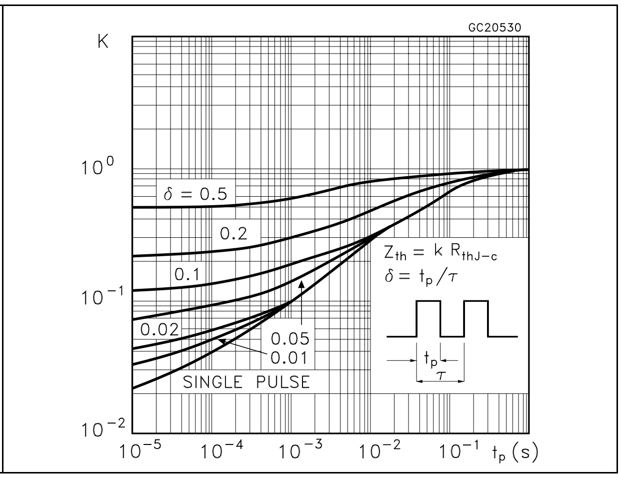


Figure 8. Output characteristics

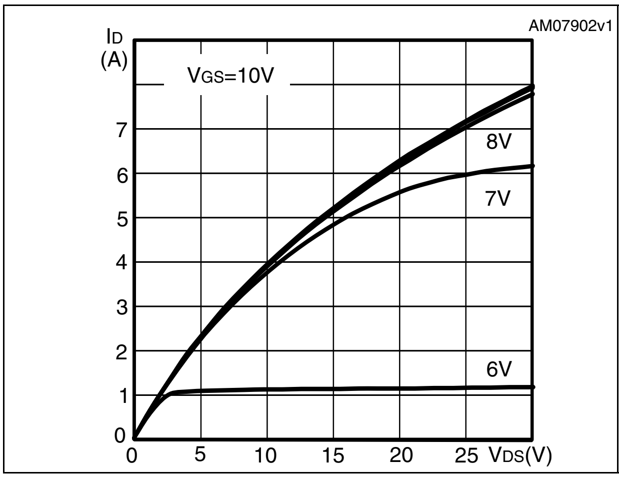


Figure 9. Transfer characteristics

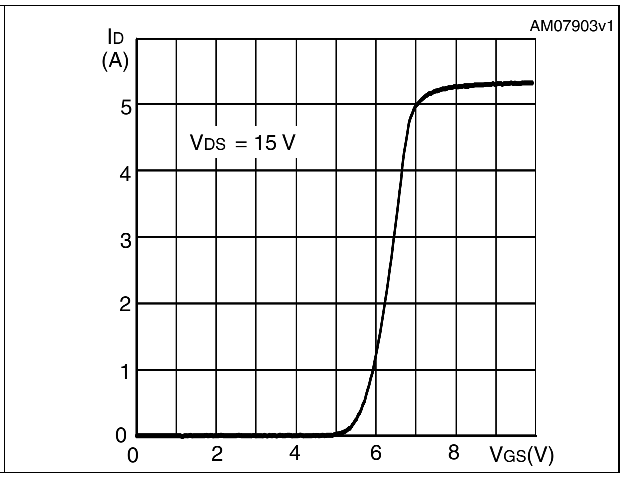


Figure 10. Normalized BV_{DSS} vs temperature

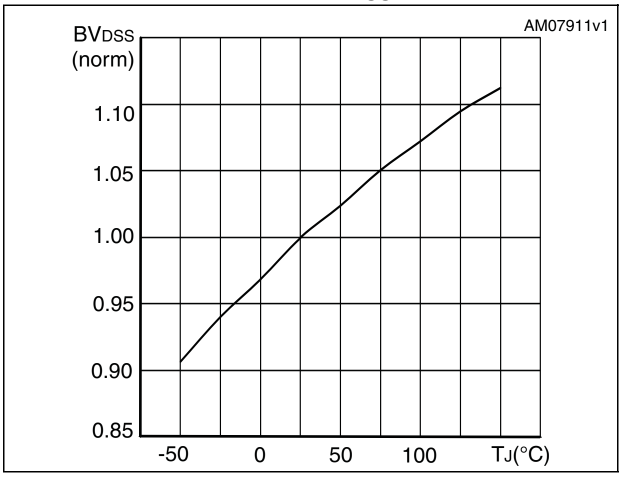


Figure 11. Static drain-source on resistance

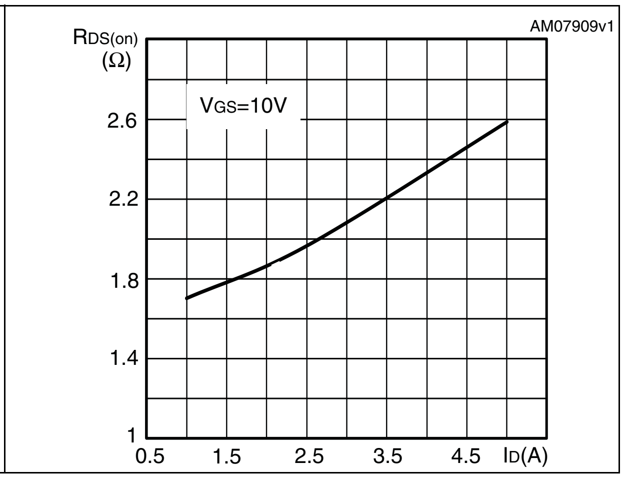


Figure 12. Output capacitance stored energy

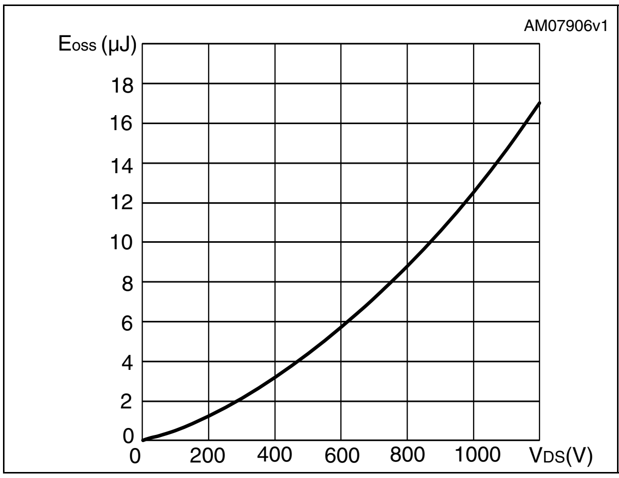


Figure 13. Capacitance variations

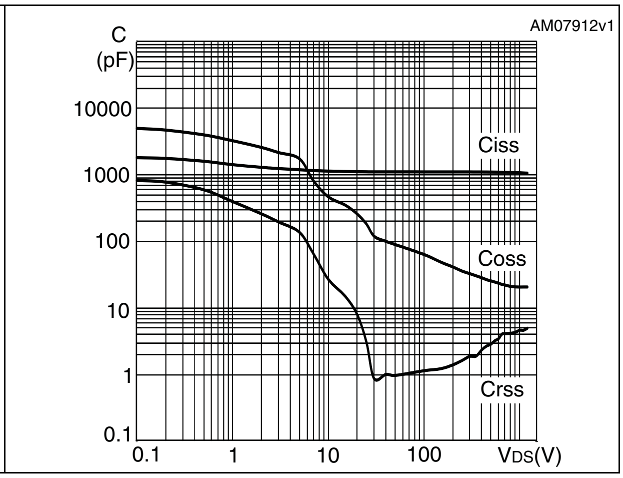


Figure 14. Gate charge vs gate-source voltage

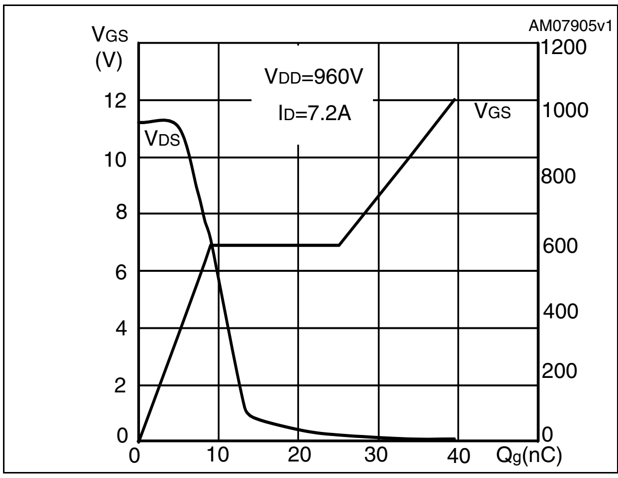


Figure 15. Normalized on resistance vs temperature

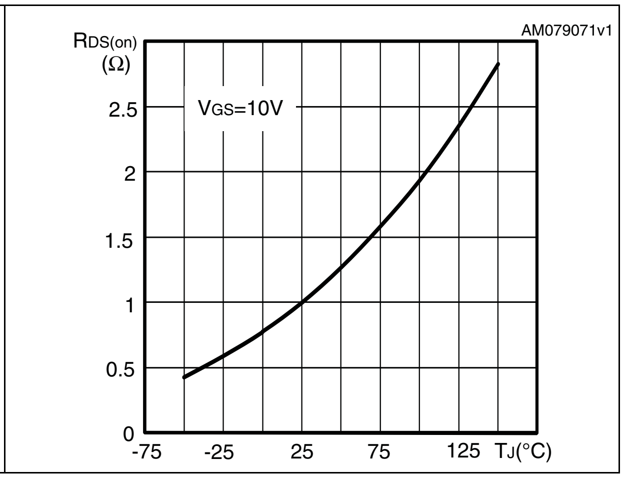


Figure 16. Normalized gate threshold voltage vs temperature

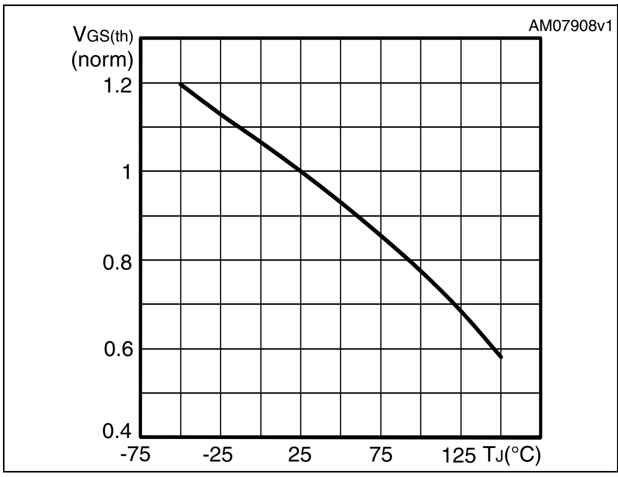


Figure 17. Maximum avalanche energy vs temperature

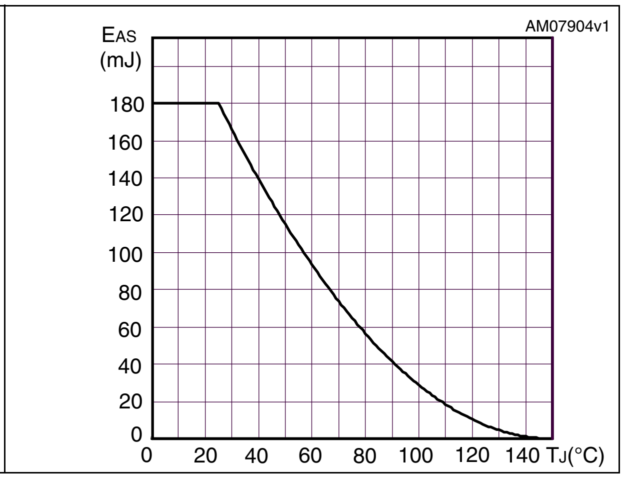
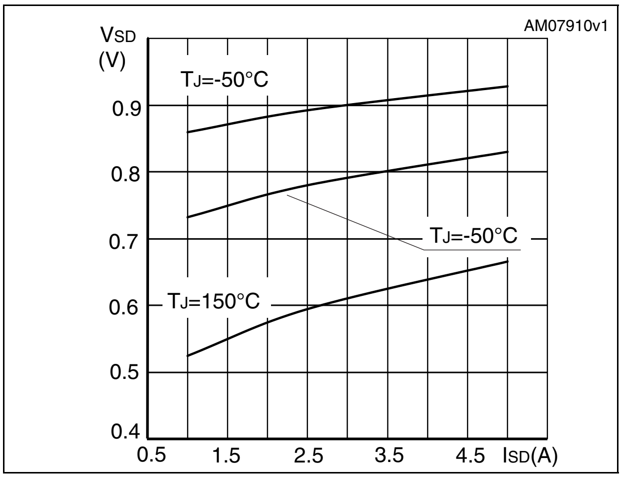


Figure 18. Source-drain diode forward characteristics



3 Test circuits

Figure 19. Switching times test circuit for resistive load

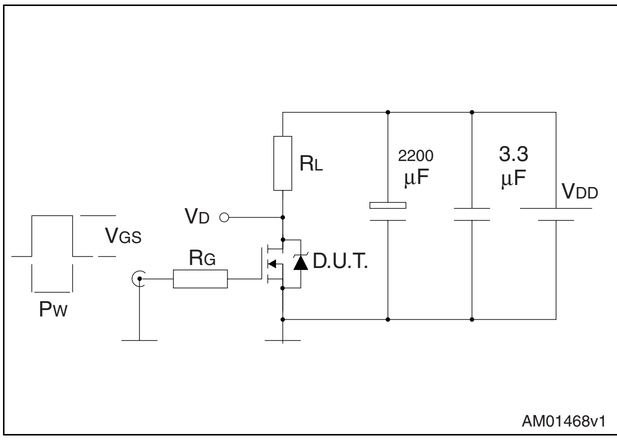


Figure 20. Gate charge test circuit

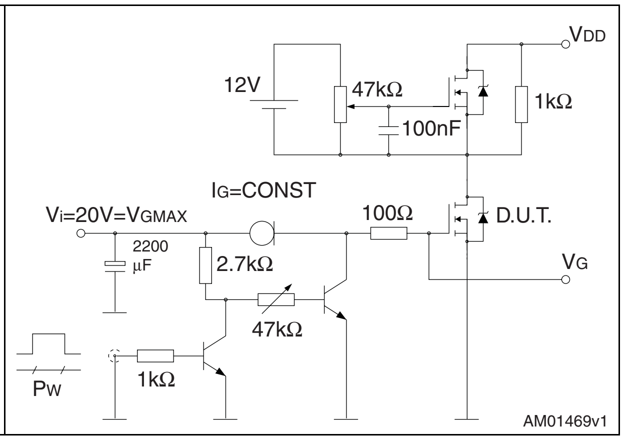


Figure 21. Test circuit for inductive load switching and diode recovery times

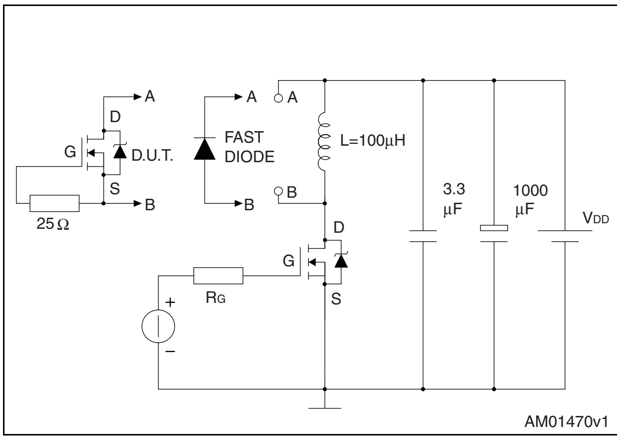


Figure 22. Unclamped inductive load test circuit

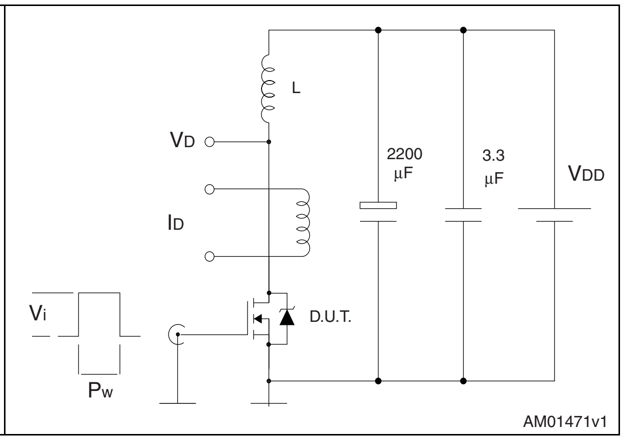


Figure 23. Unclamped inductive waveform

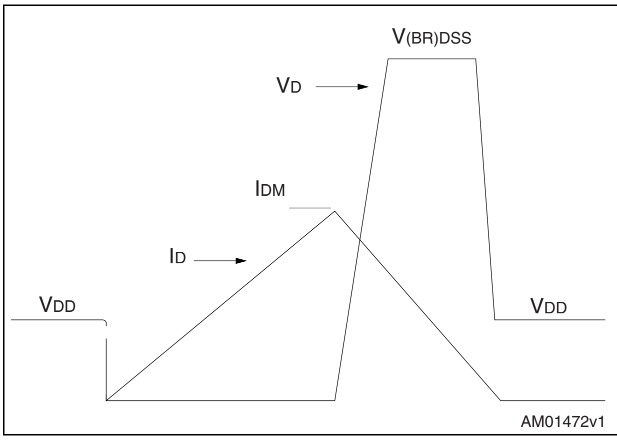
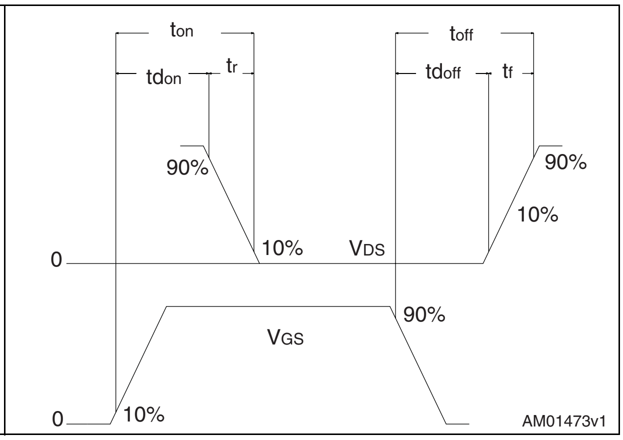


Figure 24. Switching time waveform

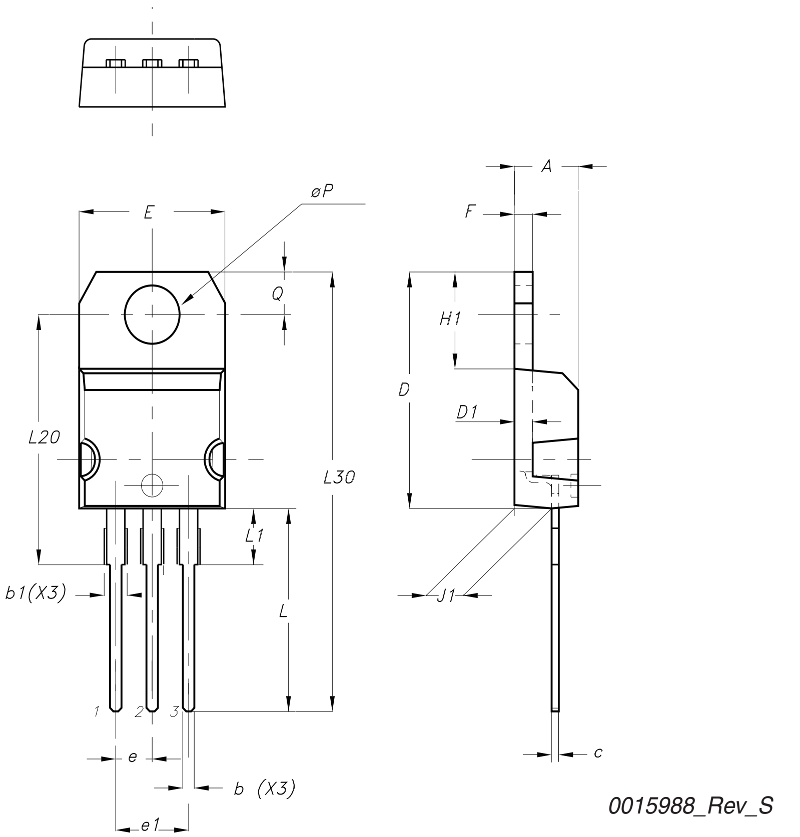


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

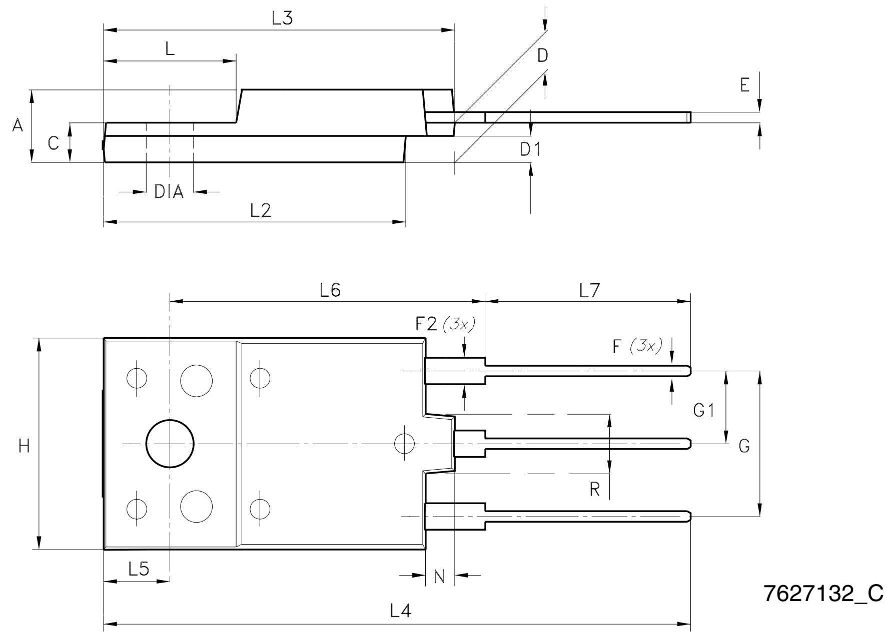
TO-220 type A mechanical data

Dim	mm		
	Min	Typ	Max
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
∅P	3.75		3.85
Q	2.65		2.95



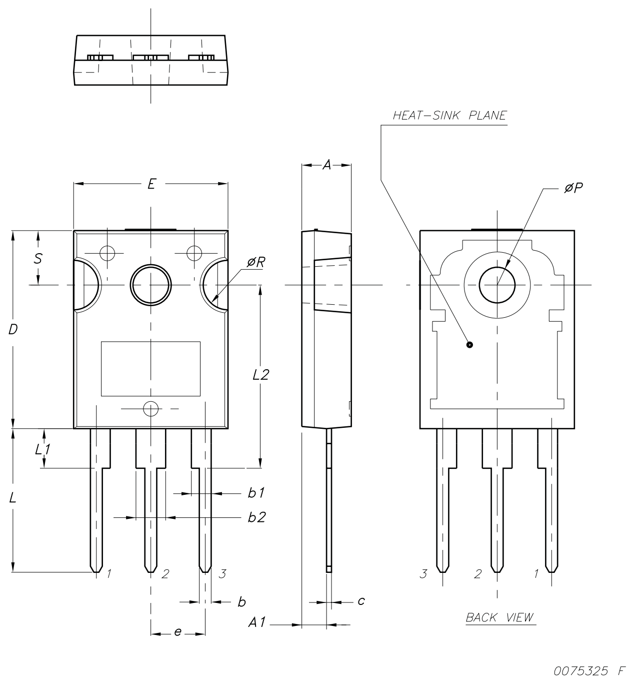
TO-3PF mechanical data

DIM.	mm.		
	min.	typ	max.
A	5.30		5.70
C	2.80		3.20
D	3.10		3.50
D1	1.80		2.20
E	0.80		1.10
F	0.65		0.95
F2	1.80		2.20
G	10.30		11.50
G1		5.45	
H	15.30		15.70
L	9.80	10	10.20
L2	22.80		23.20
L3	26.30		26.70
L4	43.20		44.40
L5	4.30		4.70
L6	24.30		24.70
L7	14.60		15
N	1.80		2.20
R	3.80		4.20
Dia	3.40		3.80



TO-247 mechanical data

Dim.	mm.		
	Min.	Typ	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e		5.45	
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
øP	3.55		3.65
øR	4.50		5.50
S		5.50	



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
15-Apr-2009	1	First release.
02-Aug-2010	2	Document status promoted from preliminary data to datasheet. Inserted *Section 2.1: Electrical characteristics (curves)*.