



# STL7NM60N

N-channel 600 V, 0.805  $\Omega$ , 5.8 A PowerFLAT™ 5x5 MDmesh™ II Power MOSFET

## Features

Order code	V <sub>DSS</sub> @ T <sub>JMAX</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STL7NM60N	650 V	< 0.90 $\Omega$	5.8 A <sup>(1)</sup>

1. The value is rated according Rthj-case

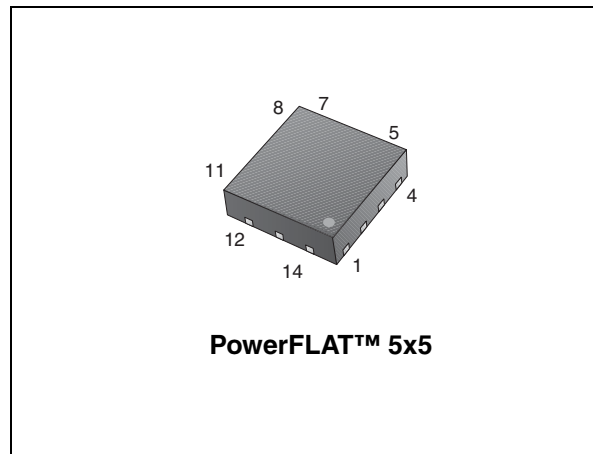
- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

## Application

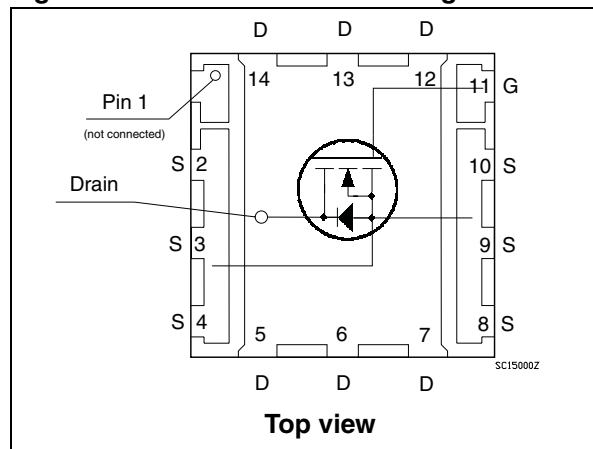
- Switching applications

## Description

This device is an N-channel Power MOSFET developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.



**Figure 1. Internal schematic diagram**



**Table 1. Device summary**

Order code	Marking	Package	Packaging
STL7NM60N	7NM60N	PowerFLAT™ 5x5	Tape and reel

# Contents

<b>1</b>	<b>Electrical ratings</b> .....	<b>3</b>
<b>2</b>	<b>Electrical characteristics</b> .....	<b>4</b>
	2.1 Electrical characteristics (curves) .....	6
<b>3</b>	<b>Test circuits</b> .....	<b>8</b>
<b>4</b>	<b>Package mechanical data</b> .....	<b>9</b>
<b>5</b>	<b>Revision history</b> .....	<b>12</b>

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	600	V
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	5.8	A
$I_D^{(1)}$	Drain current (continuous) at $T_C=100\text{ }^\circ\text{C}$	3.7	A
$I_D^{(2)}$	Drain current (continuous) at $T_{amb} = 25\text{ }^\circ\text{C}$	1.4	A
$I_D^{(2)}$	Drain current (continuous) at $T_{amb}=100\text{ }^\circ\text{C}$	0.9	A
$I_{DM}^{(2)(3)}$	Drain current (pulsed)	5.6	A
$P_{TOT}^{(2)}$	Total dissipation at $T_{amb} = 25\text{ }^\circ\text{C}$	4	W
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	68	W
$I_{AS}$	Avalanche current, repetitive or not-repetitive <sup>(3)</sup>	2	A
$E_{AS}$	Single pulse avalanche energy <sup>(4)</sup>	119	mJ
$dv/dt^{(5)}$	Peak diode recovery voltage slope	15	V/ns
$T_J$ $T_{stg}$	Operating junction temperature storage temperature	-55 to 150	$^\circ\text{C}$

1. The value is rated according  $R_{thj-case}$ .
2. When mounted on FR-4 board of 1inch<sup>2</sup>, 2oz Cu,  $t < 10$  sec
3. Pulse width limited by  $T_{jmax}$
4. Starting  $T_j = 25\text{ }^\circ\text{C}$ ,  $I_D = I_{AS}$ ,  $V_{DD} = 50$  V
5.  $I_{SD} \leq 5.8$  A,  $dv/dt \leq 400$  A/ $\mu\text{s}$ ,  $V_{DS\ peak} \leq V_{(BR)DSS}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$ .

**Table 3. Thermal resistance**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max.	1.85	$^\circ\text{C/W}$
$R_{thj-amb}^{(1)}$	Thermal resistance junction-amb max.	31.3	$^\circ\text{C/W}$

1. When mounted on FR-4 board of 1inch<sup>2</sup>, 2oz Cu,  $t < 10$  sec.

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}C$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage ( $V_{GS}=0$ )	$I_D = 1 \text{ mA}$	600			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS}=0$ )	$V_{DS} = 600 \text{ V}$ , $V_{DS} = 600 \text{ V}$ , $T_c = 125^{\circ}C$			1 100	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate body leakage current ( $V_{DS}=0$ )	$V_{GS} = \pm 25 \text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS}=V_{GS}$ , $I_D = 250 \mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS}=10 \text{ V}$ , $I_D=2.5 \text{ A}$		0.805	0.90	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 50\text{V}$ , $f=1 \text{ MHz}$ , $V_{GS}=0$	-	363	-	pF
$C_{oss}$	Output capacitance			24.6		
$C_{rss}$	Reverse transfer capacitance			1.1		
$C_{oss \text{ eq. (1)}}$	Output equivalent capacitance	$V_{GS}=0$ , $V_{DS}=0$ to 480 V	-	130	-	pF
$R_g$	Gate input resistance	$f=1 \text{ MHz}$ gate DC bias=0 test signal level = 20 mV open drain	-	5.4	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD}=480 \text{ V}$ , $I_D = 5 \text{ A}$	-	14	-	nC
$Q_{gs}$	Gate-source charge	$V_{GS}=10 \text{ V}$		2.7		
$Q_{gd}$	Gate-drain charge	(see Figure 15)		2.7		

1.  $C_{oss \text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD}=300 \text{ V}$ , $I_D = 2.5 \text{ A}$ , $R_G = 4.7 \Omega$ , $V_{GS} = 10 \text{ V}$ (see Figure 14)		7		ns
$t_r$	Rise time			10		
$t_{d(off)}$	Turn-off delay time			26		
$t_f$	Fall time			12		

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$I_{SD}$	Source-drain current		-		5.8	A
$I_{SDM}^{(1)(2)}$	Source-drain current (pulsed)		-		23	A
$V_{SD}^{(3)}$	Forward on voltage	$I_{SD}=5\text{ A}$ , $V_{GS}=0$	-		1.3	V
$t_{rr}$	Reverse recovery time	$I_{SD}=5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$ (see <a href="#">Figure 16</a> )	-	213		ns
$Q_{rr}$	Reverse recovery charge			1.5		nC
$I_{RRM}$	Reverse recovery current			14		A
$t_{rr}$	Reverse recovery time	$I_{SD}=5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 16</a> )	-	265		ns
$Q_{rr}$	Reverse recovery charge			1.8		nC
$I_{RRM}$	Reverse recovery current			14		A

1. Pulse width limited by safe operating area.
2. When mounted on FR-4 board of 1inch<sup>2</sup>, 2 oz Cu.
3. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

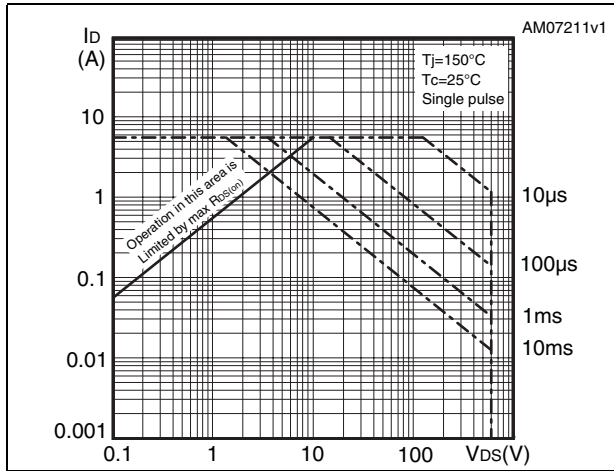


Figure 3. Thermal impedance

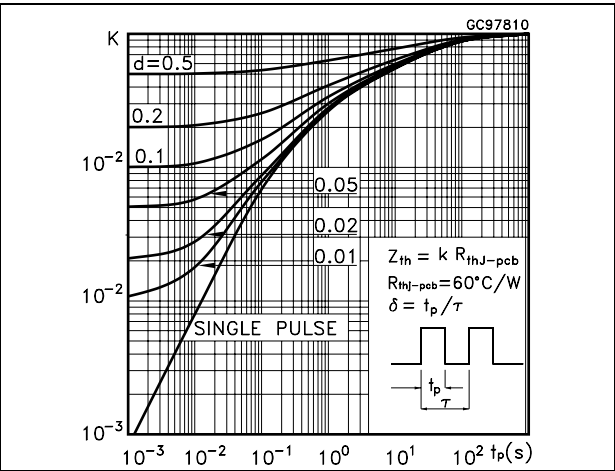


Figure 4. Output characteristics

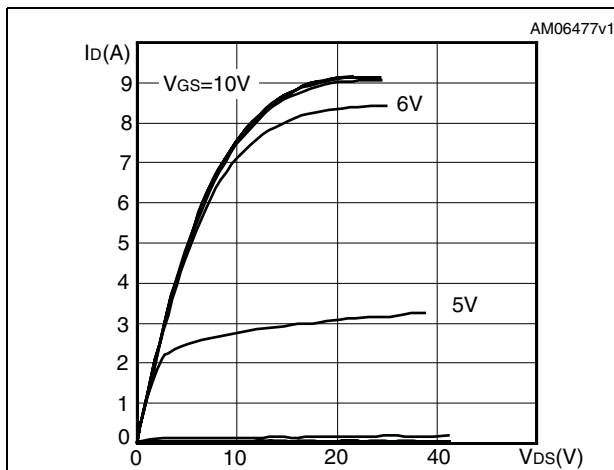


Figure 5. Transfer characteristics

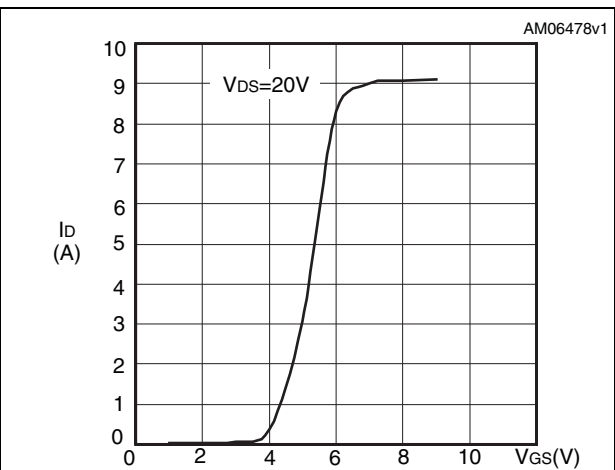


Figure 6. Gate charge vs gate-source voltage

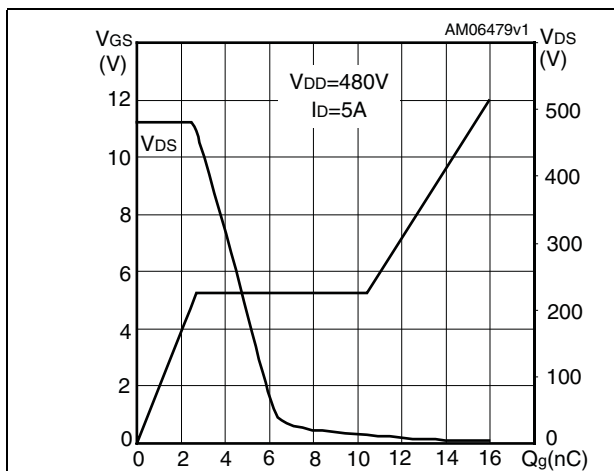


Figure 7. Static drain-source on resistance

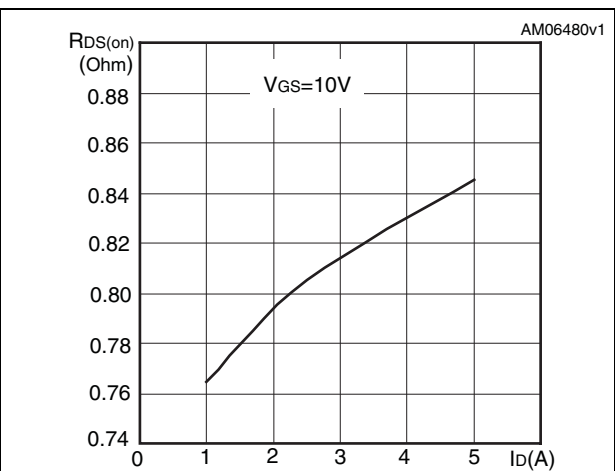


Figure 8. Capacitance variations

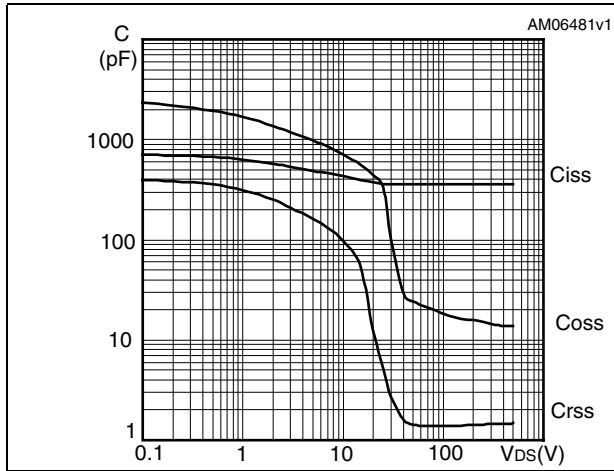


Figure 9. Output capacitance stored energy

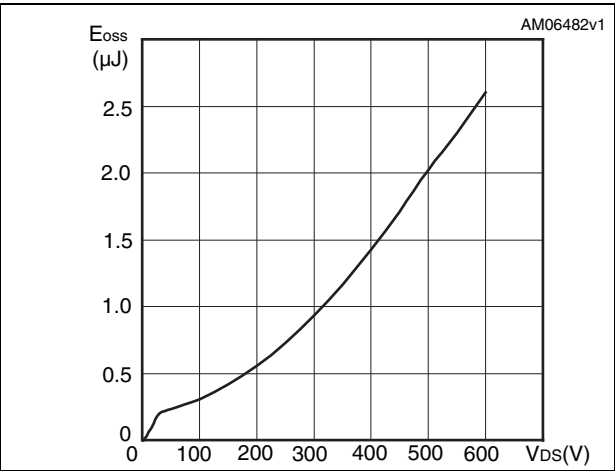


Figure 10. Normalized gate threshold voltage vs temperature

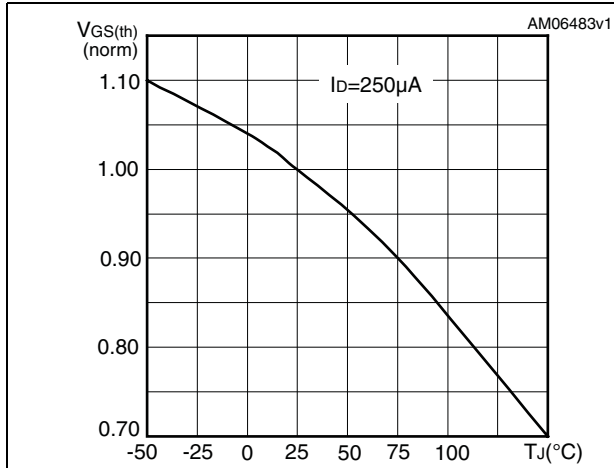


Figure 11. Normalized on resistance vs temperature

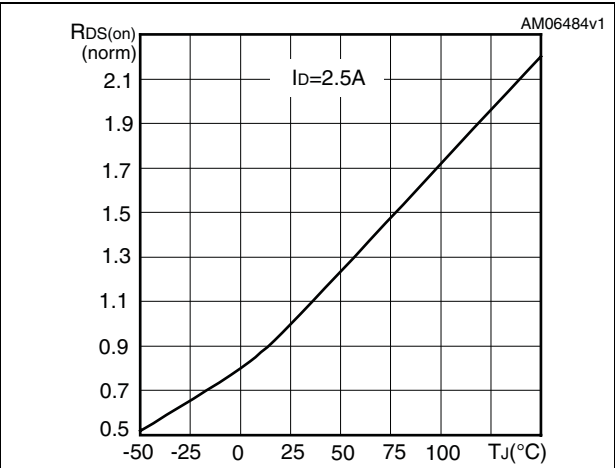


Figure 12. Normalized B<sub>VDS</sub> vs temperature

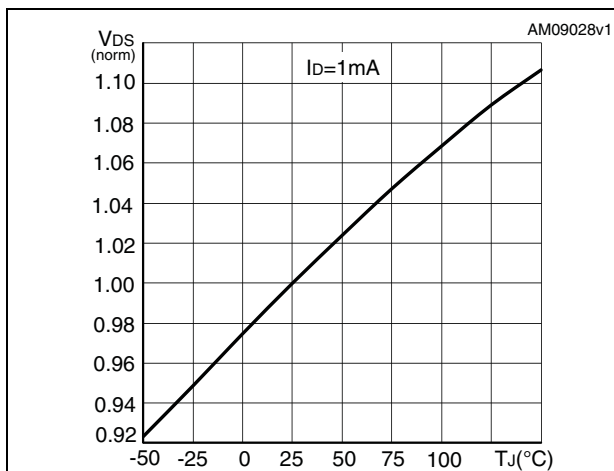
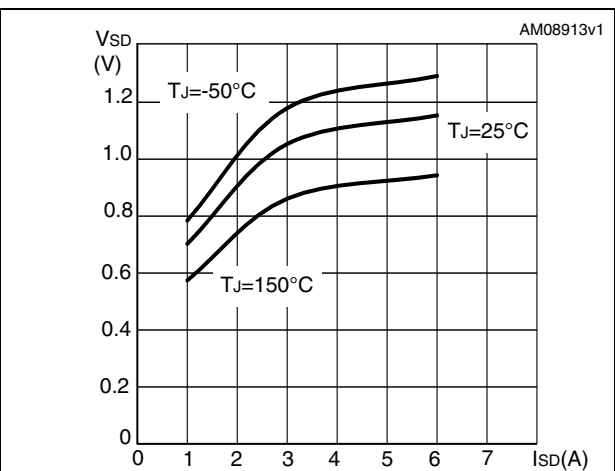


Figure 13. Source-drain diode forward characteristics



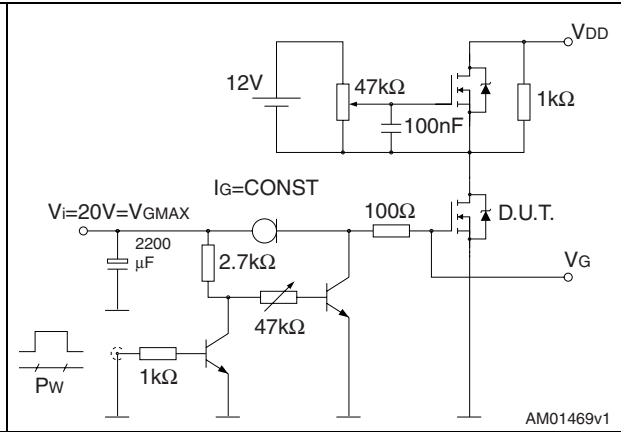
### 3 Test circuits

**Figure 14. Switching times test circuit for resistive load**



AM01468v1

**Figure 15. Gate charge test circuit**



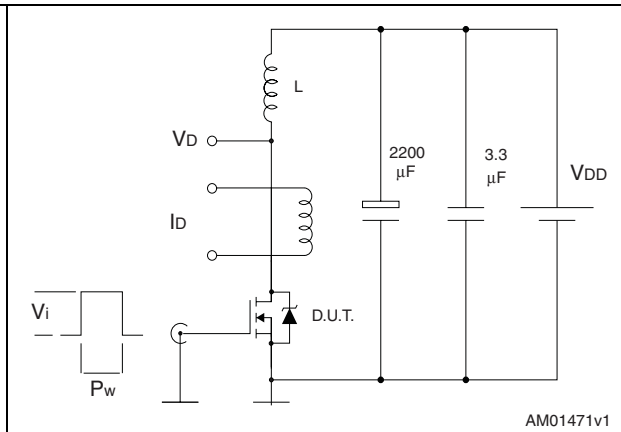
AM01469v1

**Figure 16. Test circuit for inductive load switching and diode recovery times**



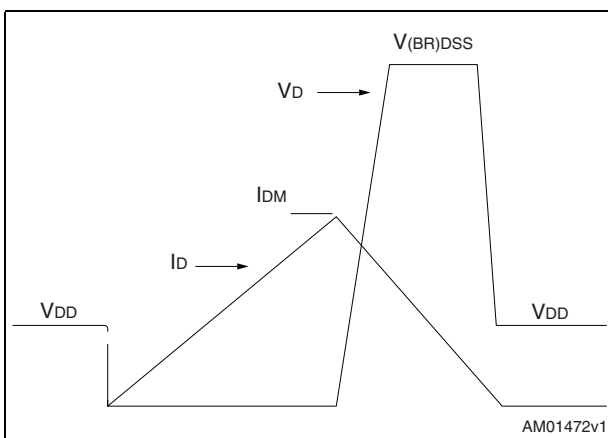
AM01470v1

**Figure 17. Unclamped inductive load test circuit**



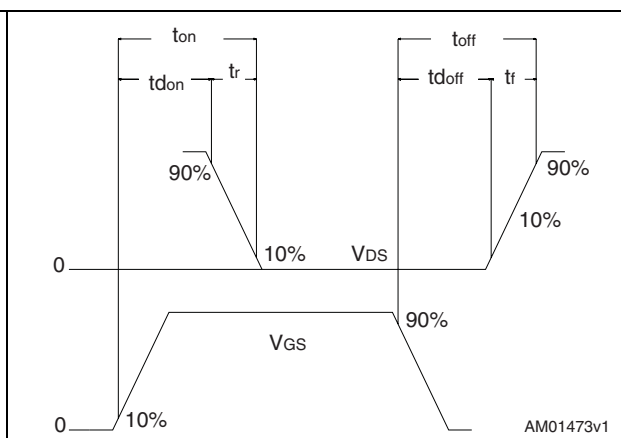
AM01471v1

**Figure 18. Unclamped inductive waveform**



AM01472v1

**Figure 19. Switching time waveform**



AM01473v1



## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

Table 8. PowerFLAT™ 5x5 mechanical dimensions

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.0
A1	0	0.02	0.05
A3		0.24	
D	4.90	5.0	5.10
E	4.90	5.0	5.10
E2	2.49	2.57	2.64
e	1.22	1.27	1.32
b	0.43	0.51	0.58
c	0.64	0.71	0.79

Figure 20. PowerFLAT™ 5x5 mechanical drawing

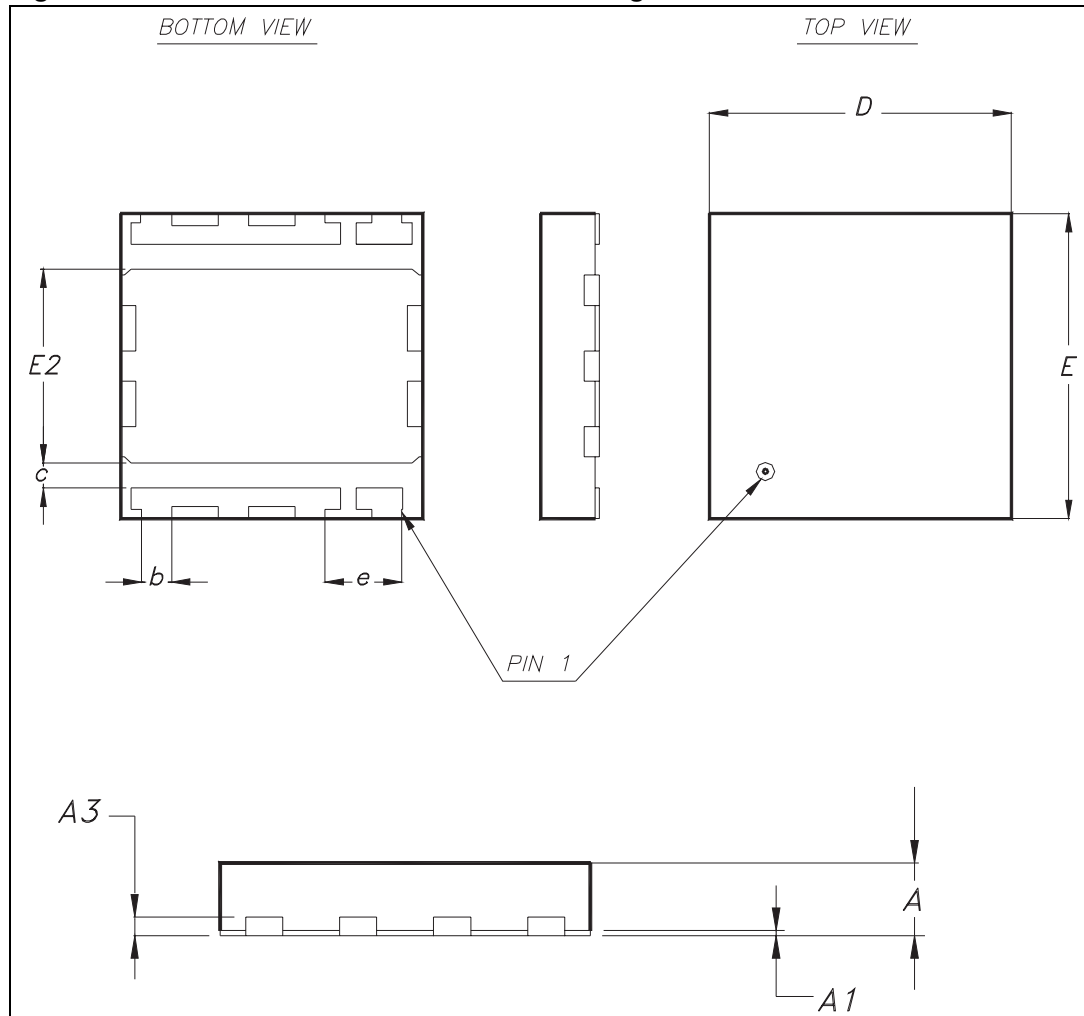
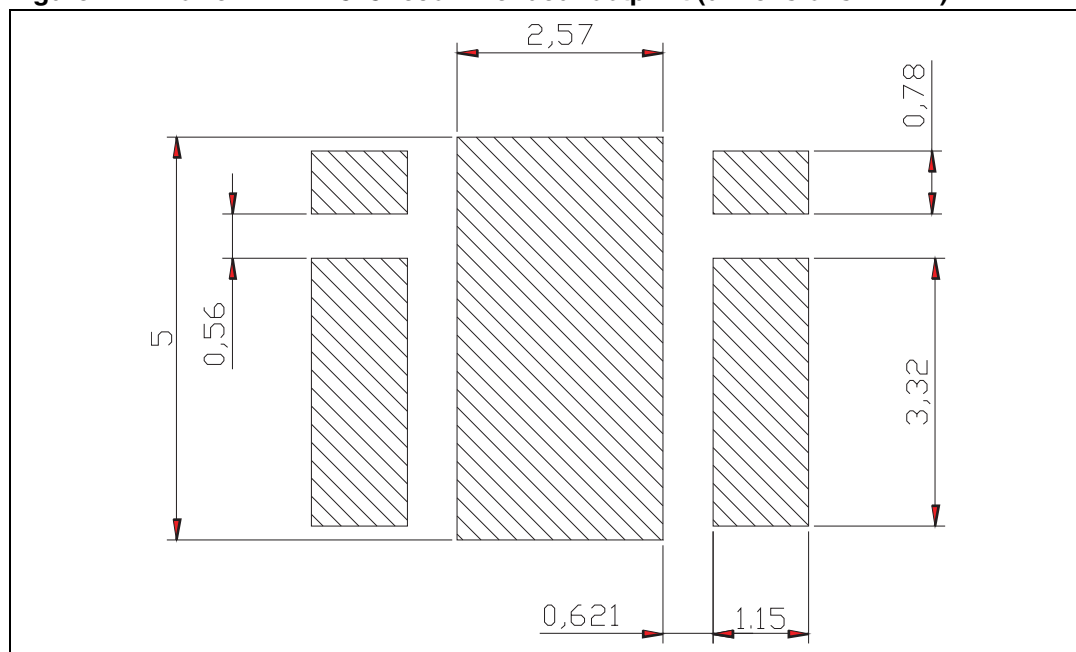


Figure 21. PowerFLAT™ 5x5 recommended footprint (dimensions in mm)



## 5 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
18-Jan-2011	1	First release.
10-Nov-2011	2	Updated <i>Figure 1: Internal schematic diagram</i> in cover page. Updated <i>Table 2: Absolute maximum ratings</i> and <i>Section 4: Package mechanical data</i> . Minor text changes.

**Please Read Carefully:**

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

**UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.**

**UNLESS EXPRESSLY APPROVED IN WRITING BY TWO AUTHORIZED ST REPRESENTATIVES, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.**

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2011 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

[www.st.com](http://www.st.com)