



STL11N3LLH6

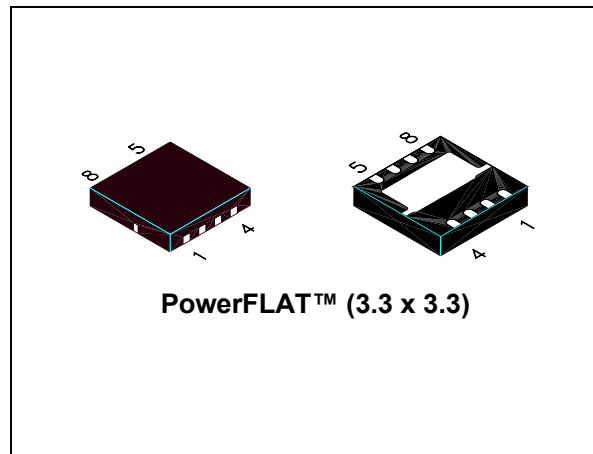
N-channel 30 V, 0.006 Ω , 11 A PowerFLAT™ (3.3 x 3.3)
 STripFET™ VI DeepGATE™ Power MOSFET

Features

Order code	V _{DSS}	R _{DS(on)} max.	I _D
STL11N3LLH6	30 V	0.0075 Ω	11 A ⁽¹⁾

1. The value is rated according R_{thj-pcb}

- R_{DS(on)} * Q_g industry benchmark
- Extremely low on-resistance R_{DS(on)}
- High avalanche ruggedness
- Low gate drive power losses
- Very low switching gate charge



Application

Switching applications

Description

This product is a 30 V N-channel STripFET™ VI Power MOSFET based on the ST's proprietary STripFET™ technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest R_{DS(on)} in all packages.

Figure 1. Internal schematic diagram

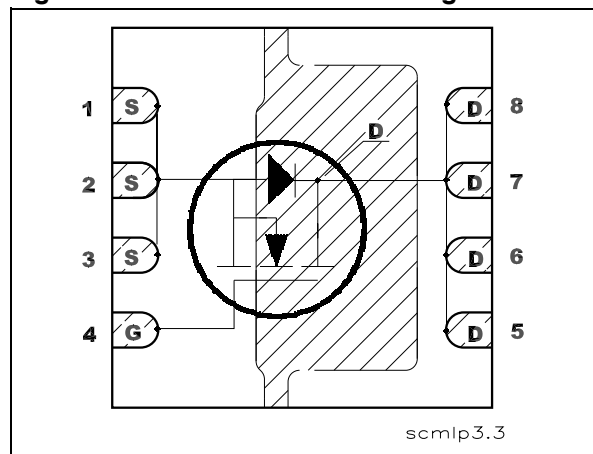


Table 1. Device summary

Order code	Marking	Package	Packaging
STL11N3LLH6	11N3L	PowerFLAT™ (3.3 x 3.3)	Tape and reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	30	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	11	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	6.9	A
$I_{DM}^{(2)}$	Drain current (pulsed)	44	A
$P_{TOT}^{(3)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	50	W
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	2	W
	Derating factor	0.03	W/ $^\circ\text{C}$
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150	$^\circ\text{C}$

1. The value is rated according $R_{thj-pcb}$
2. Pulse width limited by safe operating area
3. The value is rated according R_{thj-c}

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case (drain) (steady state)	2.5	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	42.8	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(2)}$	Thermal resistance junction-pcb	63.5	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of 1inch², 2oz Cu, $t < 10$ sec
2. Steady state

Table 4. Avalanche data

Symbol	Parameter	Value	Unit
I_{AV}	Not-repetitive avalanche current, (pulse width limited by T_J max.)	TBD	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AV}$, $V_{DD} = 24\text{ V}$)	TBD	mJ

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0$	30			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$, $V_{DS} = \text{Max rating @ } 125\text{ °C}$			1 10	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	1			V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 5.5\text{ A}$ $V_{GS} = 4.5\text{ V}$, $I_D = 5.5\text{ A}$		0.006 0.0084	0.0075 0.0095	Ω Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$		1690		pF
C_{oss}	Output capacitance			290		pF
C_{rss}	Reverse transfer capacitance			176		pF
Q_g	Total gate charge	$V_{DD} = 15\text{ V}$, $I_D = 11\text{ A}$ $V_{GS} = 4.5\text{ V}$ (see Figure 3)		17		nC
Q_{gs}	Gate-source charge			8		nC
Q_{gd}	Gate-drain charge			6		nC
R_G	Gate input resistance	$f = 1\text{ MHz}$ Gate DC Bias = 0 Test signal level = 20 mV open drain		1.7		Ω

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 15\text{ V}$, $I_D = 5.5\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 2)		TBD		ns
t_r	Rise time			TBD		ns
$t_{d(off)}$	Turn-off delay time				TBD	ns
t_f	Fall time				TBD	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				11	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				44	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 11 \text{ A}, V_{GS} = 0$			1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = 11 \text{ A},$ $di/dt = 100 \text{ A}/\mu\text{s},$ $V_{DD} = 25 \text{ V}$		TBD		ns
Q_{rr}	Reverse recovery charge			TBD		nC
I_{RRM}	Reverse recovery current			TBD		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

3 Test circuits

Figure 2. Switching times test circuit for resistive load

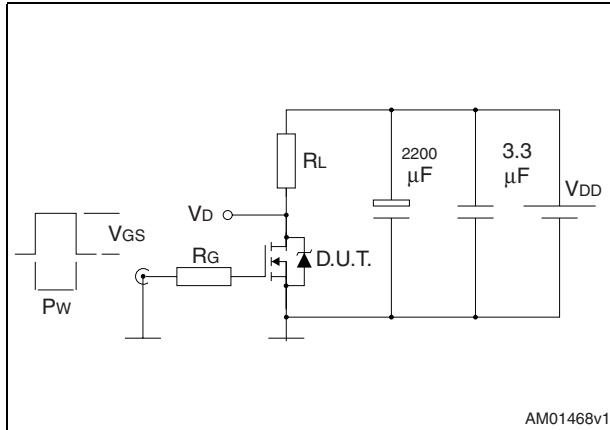


Figure 3. Gate charge test circuit

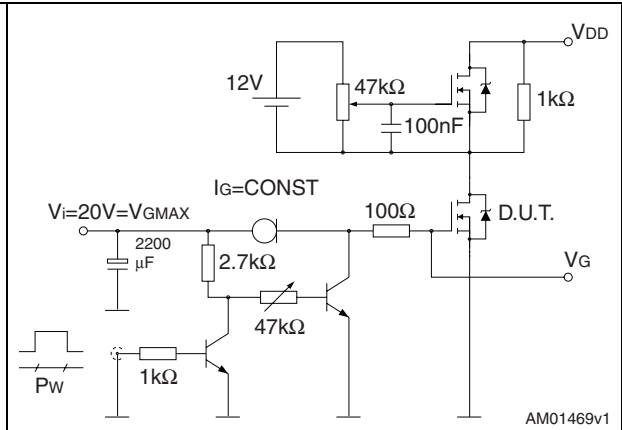


Figure 4. Test circuit for inductive load switching and diode recovery times

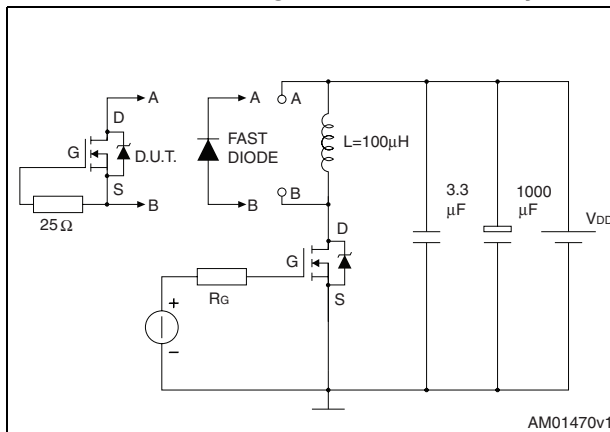


Figure 5. Unclamped inductive load test circuit

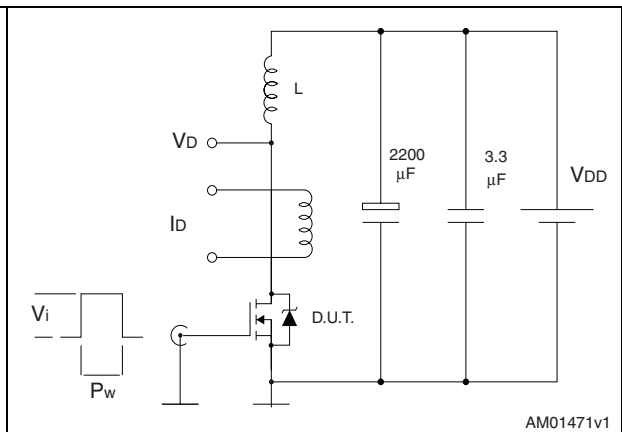


Figure 6. Unclamped inductive waveform

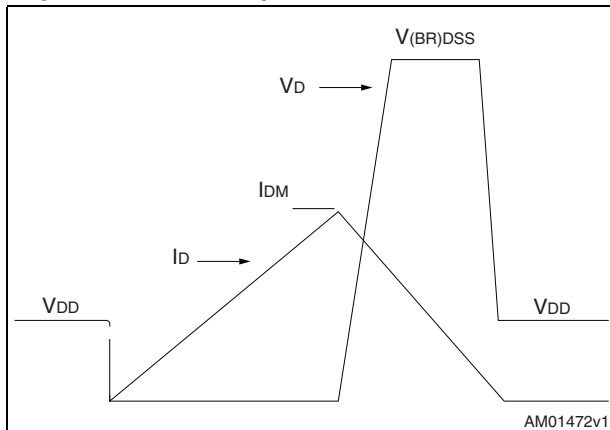
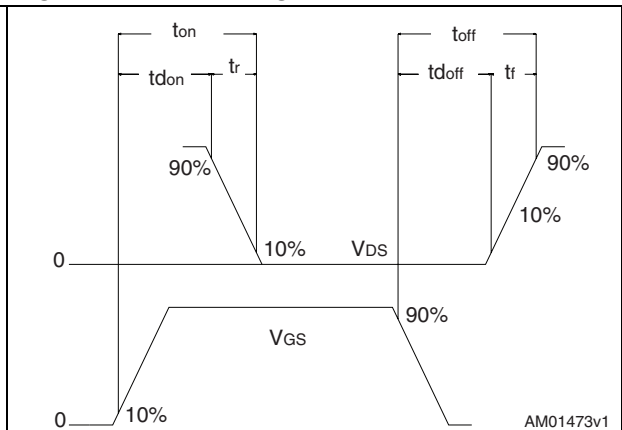


Figure 7. Switching time waveform

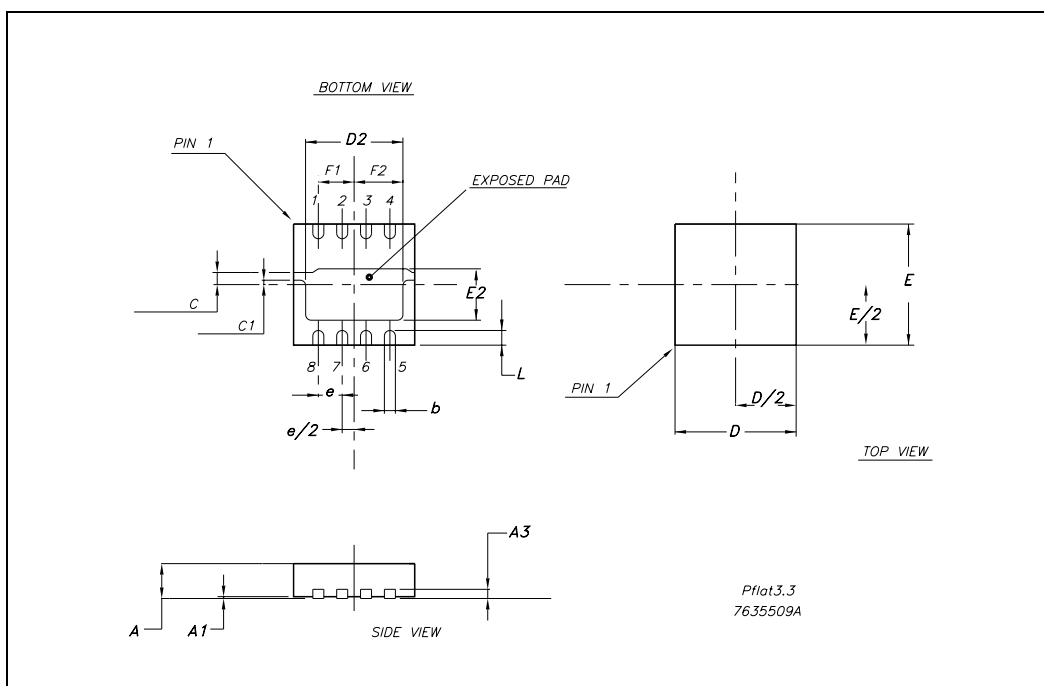


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

PowerFLAT™ (3.3x3.3) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	0.80	0.90	1.00	0.031	0.035	0.039
A1		0.02	0.05		0.0007	0.0019
A3		0.20			0.007	
b	0.23	0.30	0.38	0.009	0.011	0.015
C		0.328			0.012	
C1		0.12			0.004	
D		3.30			0.13	
D2	2.50	2.65	2.75	0.098	0.104	0.108
E		3.30			0.13	
E2	1.25	1.40	1.50	0.049	0.055	0.059
F		1.325			0.052	
F1		0.975			0.038	
e		0.65			0.025	
L	0.30		0.50	0.011		0.019



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
02-Sep-2010	1	First release

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