



STL17N3LLH6

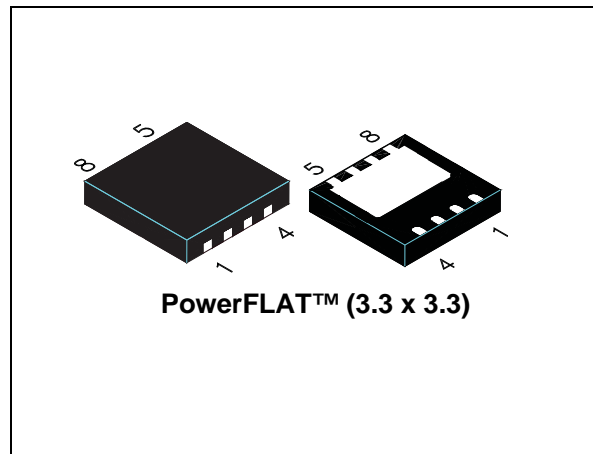
N-channel 30 V, 0.0038 Ω , 17 A PowerFLAT™(3.3x3.3)
STripFET™ VI DeepGATE™ Power MOSFET

Features

Order code	V _{DSS}	R _{DS(on)} max.	I _D
STL17N3LLH6	30 V	0.0045 Ω	17 A ⁽¹⁾

1. The value is rated according R_{thj-pcb}

- R_{DS(on)} * Q_g industry benchmark
- Extremely low on-resistance R_{DS(on)}
- High avalanche ruggedness
- Low gate drive power losses
- Very low switching gate charge



Application

Switching applications

Description

This product utilizes the 6th generation of design rules of ST's proprietary STripFET™ technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest R_{DS(on)} in a standard package, that makes it suitable for the most demanding DC-DC converter applications, where high power density has to be achieved.

Figure 1. Pin-out configuration

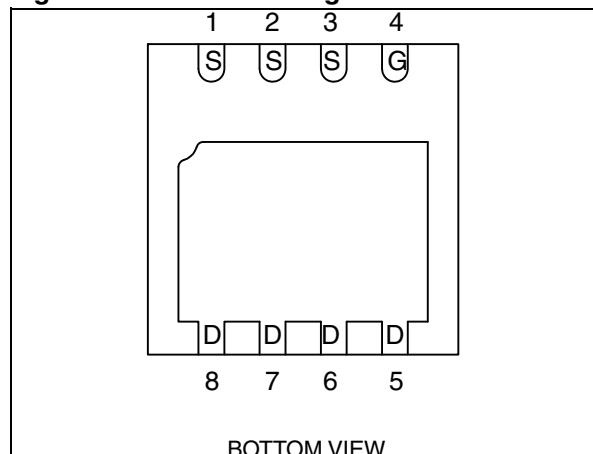


Table 1. Device summary

Order code	Marking	Package	Packaging
STL17N3LLH6	17N3L	PowerFLAT™ (3.3 x 3.3)	Tape and reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	30	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	17	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	11	A
$I_{DM}^{(2)}$	Drain current (pulsed)	68	A
$P_{TOT}^{(3)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	50	W
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	2	W
	Derating factor	0.03	W/ $^\circ\text{C}$
T_J	Operating junction temperature	-55 to 150	$^\circ\text{C}$
T_{stg}	Storage temperature		

1. The value is rated according $R_{thj-pcb}$
2. Pulse width limited by safe operating area
3. The value is rated according R_{thj-c}

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case (drain) (steady state)	2.5	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	42.8	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(2)}$	Thermal resistance junction-pcb	63.5	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of 1inch², 2oz Cu, $t < 10\text{ sec}$
2. Steady state

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0$	30			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$, $V_{DS} = \text{Max rating @ } 125\text{ °C}$			1 10	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	1			V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 8.5\text{ A}$ $V_{GS} = 4.5\text{ V}$, $I_D = 8.5\text{ A}$		0.0038 0.0057	0.0045 0.0073	Ω Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	1690	-	pF
C_{oss}	Output capacitance			290		pF
C_{rss}	Reverse transfer capacitance			176		pF
Q_g	Total gate charge	$V_{DD} = 15\text{ V}$, $I_D = 17\text{ A}$ $V_{GS} = 4.5\text{ V}$ <i>(see Figure 14)</i>	-	17	-	nC
Q_{gs}	Gate-source charge			8		nC
Q_{gd}	Gate-drain charge			6		nC
R_G	Gate input resistance	$f = 1\text{ MHz}$ Gate DC Bias = 0 Test signal level = 20 mV open drain	-	1.7	-	Ω

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 15\text{ V}$, $I_D = 8.5\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ <i>(see Figure 13)</i>	-	9.5	-	ns
t_r	Rise time			30		ns
$t_{d(off)}$	Turn-off delay time			37		ns
t_f	Fall time			12		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		17	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		68	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 17\text{ A}, V_{GS} = 0$	-		1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = 17\text{ A},$ $di/dt = 100\text{ A}/\mu\text{s},$ $V_{DD} = 25\text{ V}$	-	24		ns
Q_{rr}	Reverse recovery charge			16.8		nC
I_{RRM}	Reverse recovery current			1.4		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

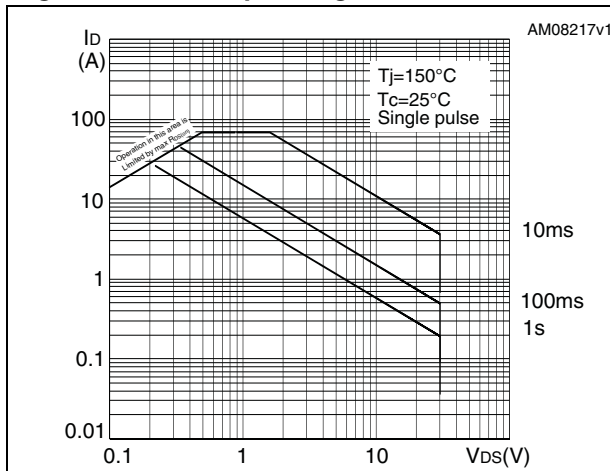


Figure 3. Thermal impedance

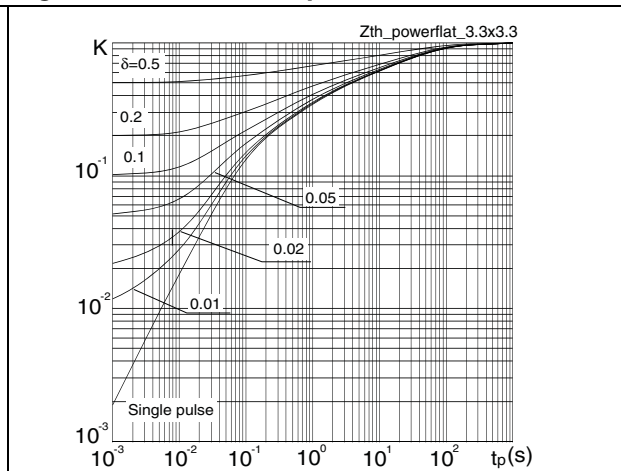


Figure 4. Output characteristics

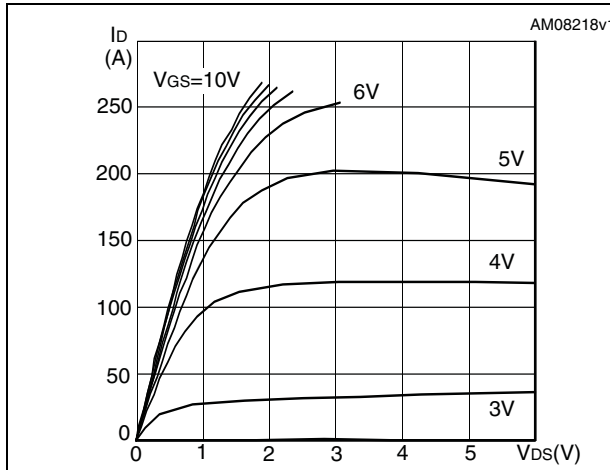


Figure 5. Transfer characteristics

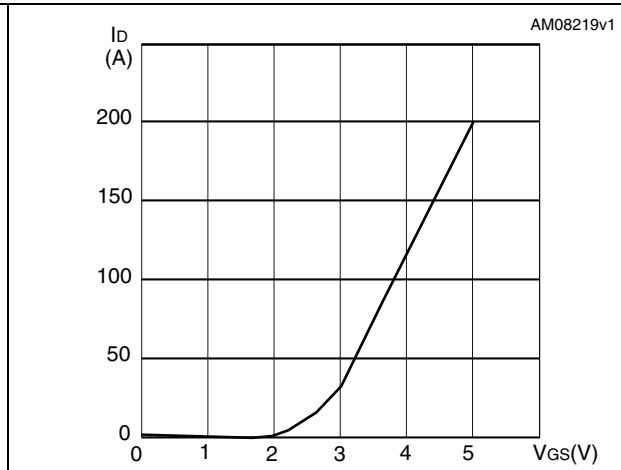


Figure 6. Normalized BV_{DSS} vs temperature

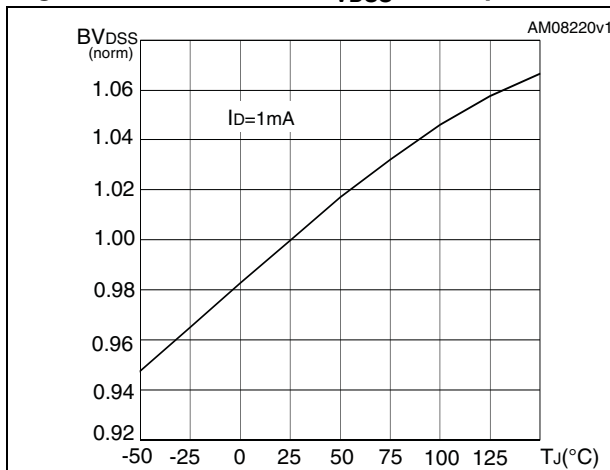


Figure 7. Static drain-source on resistance

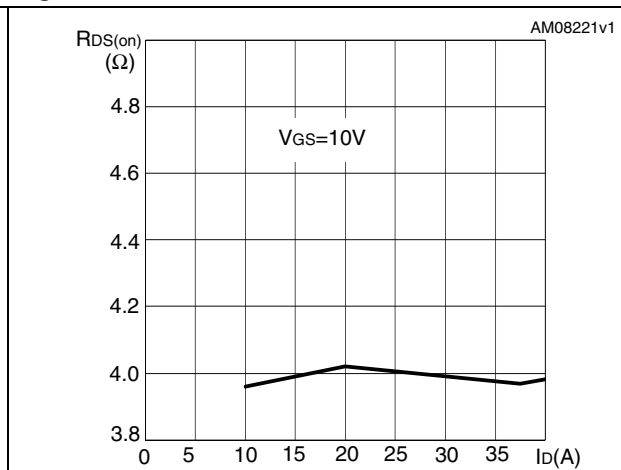


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

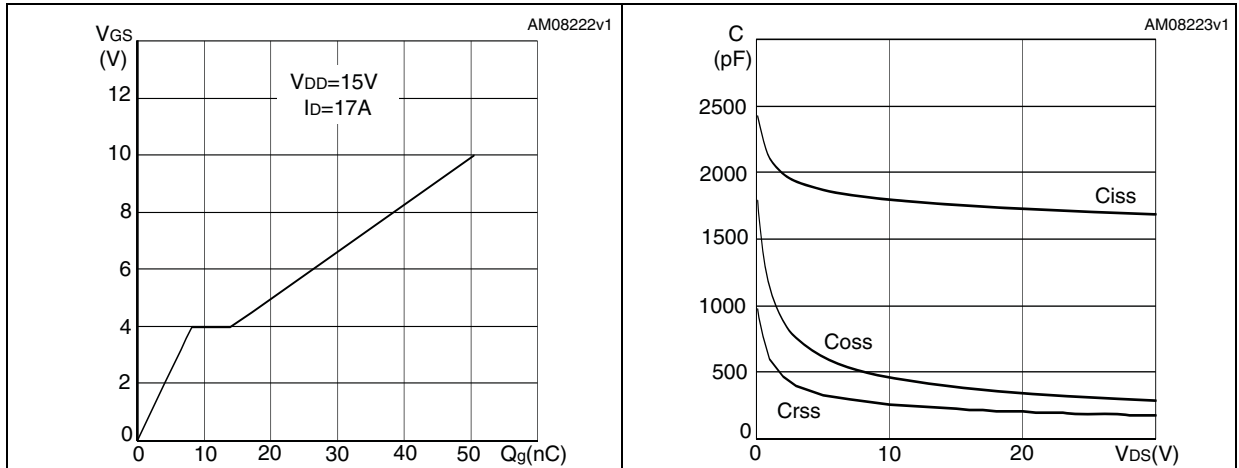


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

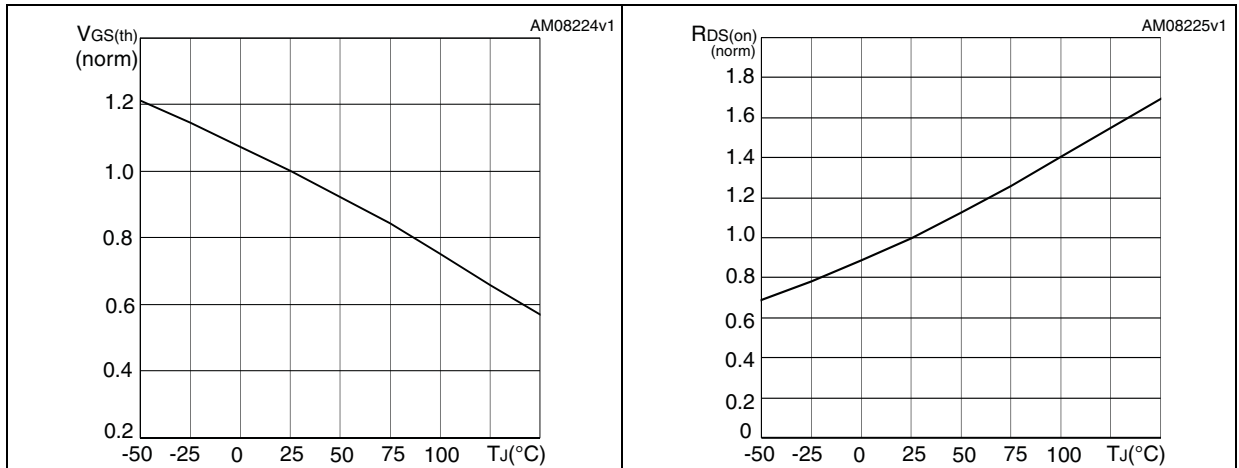
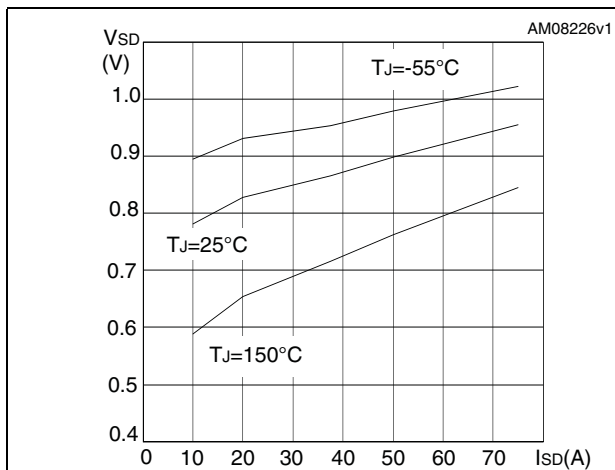


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load



Figure 14. Gate charge test circuit

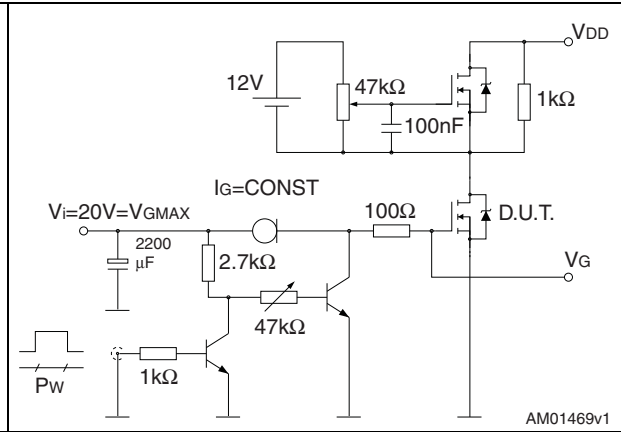


Figure 15. Test circuit for inductive load switching and diode recovery times



Figure 16. Unclamped inductive load test circuit

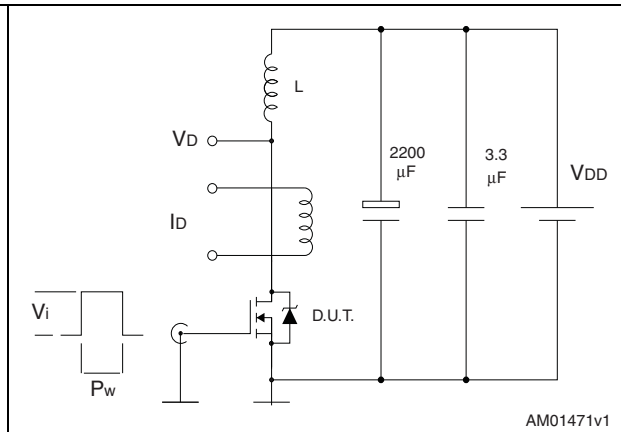


Figure 17. Unclamped inductive waveform

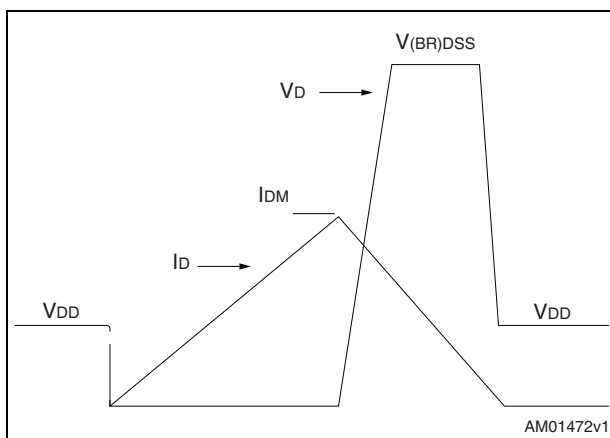
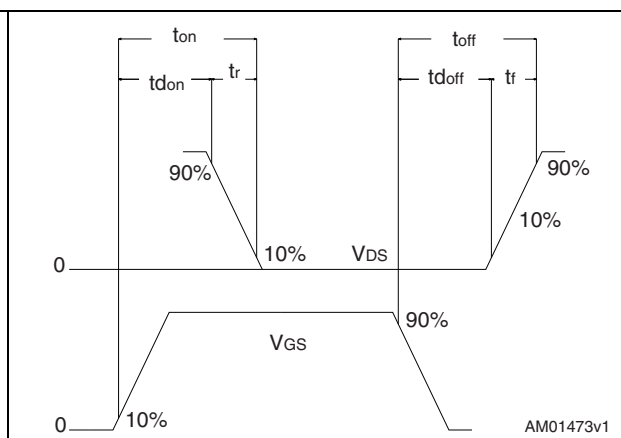


Figure 18. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. Package dimensions

Dim.	mm.		
	Min.	Typ	Max.
A	0.80	0.90	1.00
A1		0.02	0.05
b	0.25	0.30	0.35
D		3.30	
D2	2.50	2.65	2.75
e		0.65	
E		3.30	
E2	1.76	1.91	2.01
L	0.30	0.40	0.50

Figure 19. Package drawing

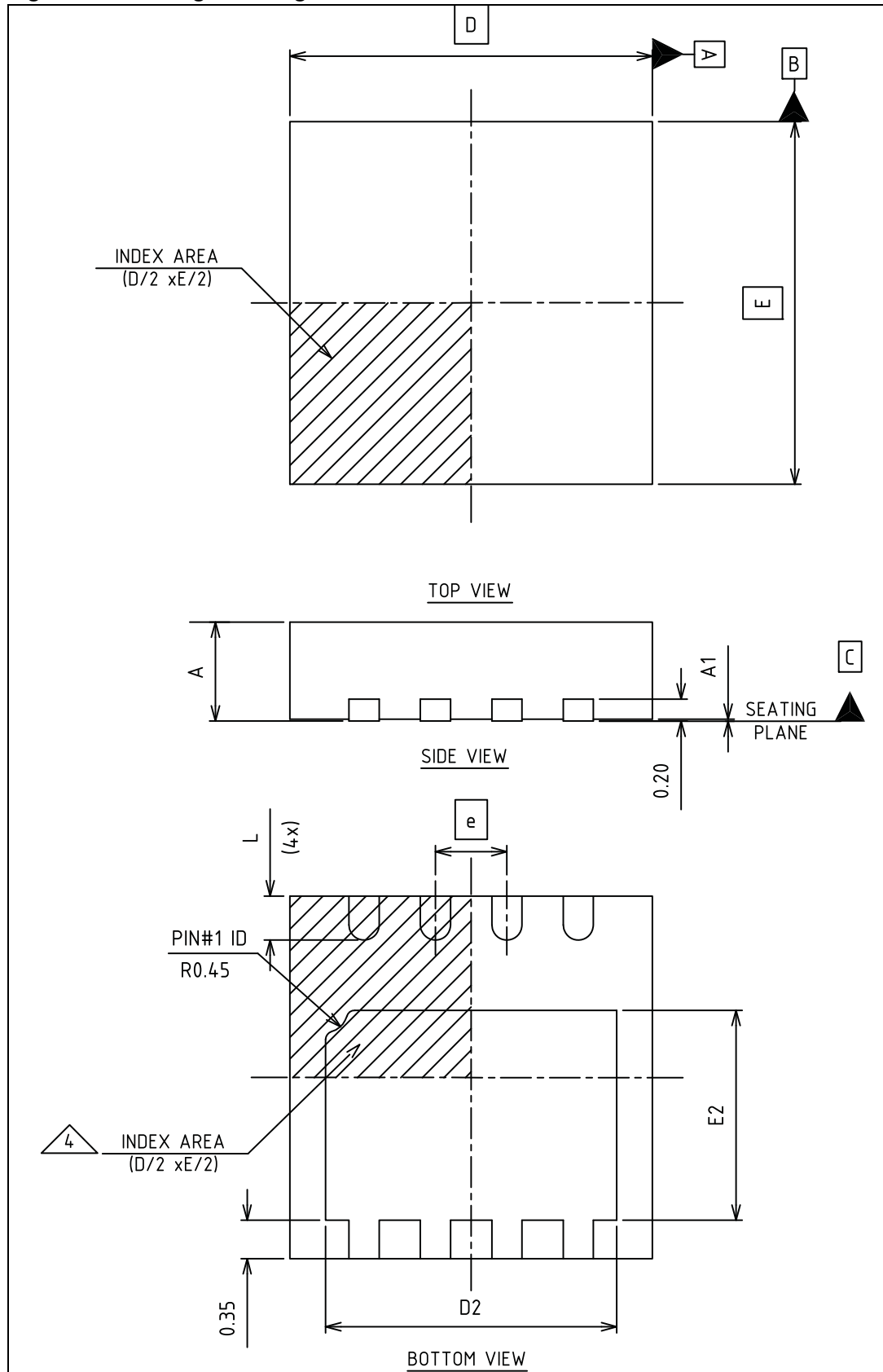
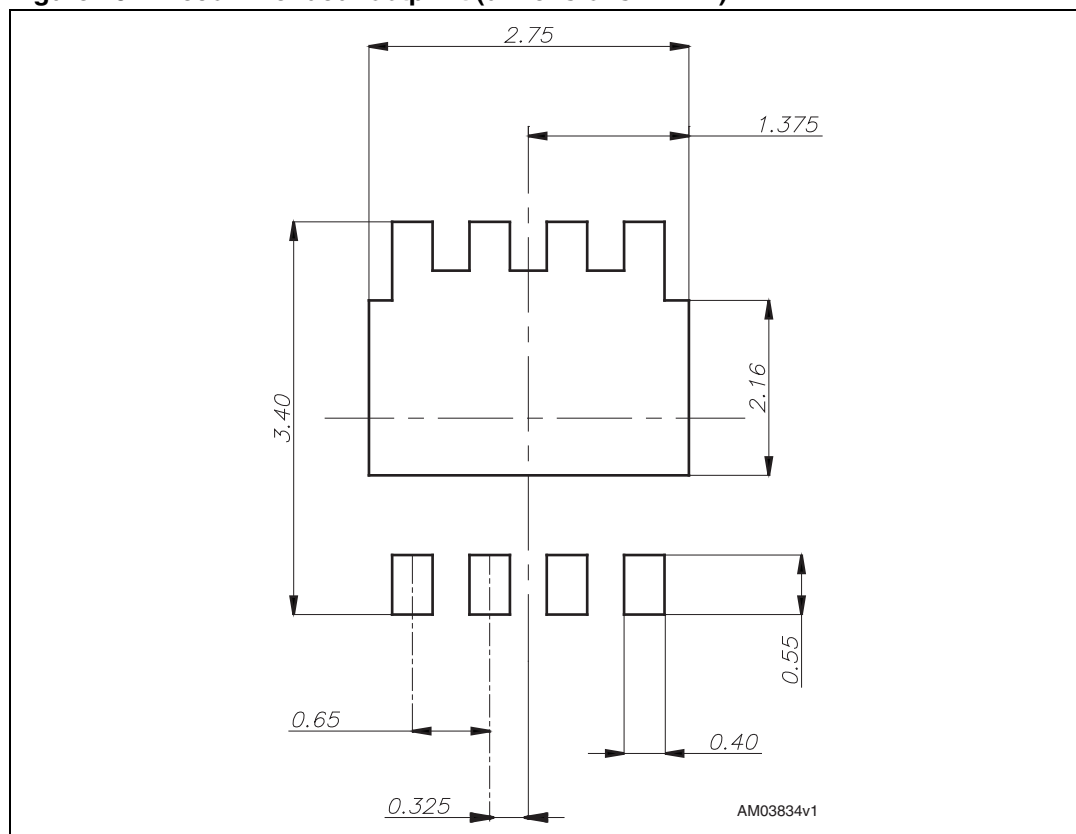


Figure 20. Recommended footprint (dimensions in mm)



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
24-Mar-2009	1	First release.
06-Jul-2010	2	Updated Table 4: On/off states .
10-Nov-2010	3	Document status promoted from preliminary data to datasheet.

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