STL56N3LLH5

N-channel 30 V, 0.0076 Ω, 15 A STripFET™ V Power MOSFET in PowerFLAT™ 5x6 package

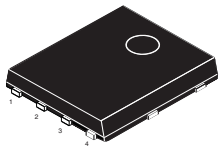
Datasheet — production data

Features

Type	V_{DSS}	$R_{DS(on)}$ max	I_D
STL56N3LLH5	30 V	< 0.009 Ω	15 A (1)

1. The value is rated according $R_{thj\text{-}pcb}$

- $R_{DS(on)}$ * Q_g industry benchmark
- Extremely low on-resistance $R_{DS(on)}$
- Very low switching gate charge
- High avalanche ruggedness
- Low gate drive power losses



PowerFLAT™ 5x6

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using STMicroelectronics' STripFET™V technology. The device has been optimized to achieve very low on-state resistance, contributing to an FOM that is among the best in its class.

Figure 1. Internal schematic diagram

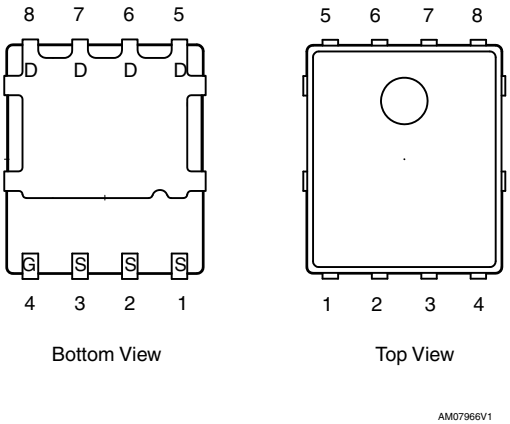


Table 1. Device summary

Order code	Marking	Package	Packaging
STL56N3LLH5	56N3LLH5	PowerFLAT™ 5x6	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	30	V
V_{GS}	Gate-source voltage	+22 / -20	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	56	A
I_D (1)	Drain current (continuous) at T_C = 100 °C	37	A
I_D (2)	Drain current (continuous) at T_{pcb} = 25 °C	15	A
I_D (2)	Drain current (continuous) at T_{pcb} =100°C	10	A
I_{DM} (2)(3)	Drain current (pulsed)	60	A
P_{TOT} (1)	Total dissipation at T_C = 25°C	62.5	W
P_{TOT} (2)	Total dissipation at T_{pcb} = 25°C	4	W
	Derating factor	0.03	W/°C
E_{AS} (4)	Single pulse avalanche energy	150	mJ
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150	°C

1. The value is rated according to $R_{thj\text{-}c}$
2. The value is rated according to $R_{thj\text{-}pcb}$
3. Pulse width limited by safe operating area
4. Starting T_j = 25 °C, I_D = 60 A, V_{DD} = 50 V

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	2	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb	31.3	°C/W

1. When mounted on FR-4 board of 1inch², 2oz Cu, t < 10 sec

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS}= 0, I_D = 250 µA	30			V
I_{DSS}	Zero gate voltage drain current	V_{GS}= 0, V_{DS} = 30 V,			1	µA
		V_{GS}= 0 V_{DS} = 30 V, T_C = 125 °C			10	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0, V_{GS} = +22 / -20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250 µA	1		2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS}= 10 V, I_D= 7.5 A V_{GS}= 4.5 V, I_D= 7.5 A		0.0076 0.0099	0.009 0.0112	Ω Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =25 V, f=1 MHz, V_{GS}=0	-	950 193 27		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}=15 V, I_D = 15 A V_{GS} =4.5 V *Figure 14*	-	6.5 3.3 2.4	10	nC nC nC
R_g	Gate input resistance	f=1 MHz gate DC bias=0 test signal level = 20 mV open drain	-	1.7	2.5	Ω

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD}=15 V, I_D= 7.5 A, R_G=4.7 Ω, V_{GS}=10 V *Figure 13*	-	10.8 15.6 14.2 6	-	ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current		-		15	A
I_{SDM}(1)	Source-drain current (pulsed)		-		60	A
V_{SD}(2)	Forward on voltage	I_{SD} = 15 A, V_{GS}=0	-		1.1	V
t_{rr}	Reverse recovery time	I_{SD} = 15 A,		20	36	ns
Q_{rr}	Reverse recovery charge	di/dt = 100 A/µs,	-	10	18	nC
I_{RRM}	Reverse recovery current	V_{DD}=25 V, Tj=150 °C		1		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration= 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

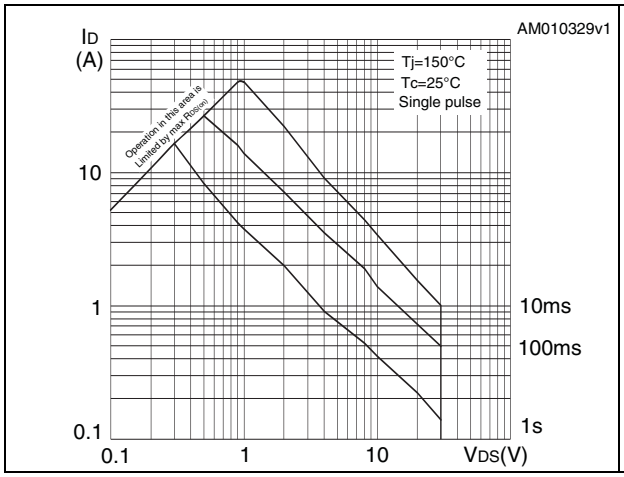


Figure 3. Thermal impedance

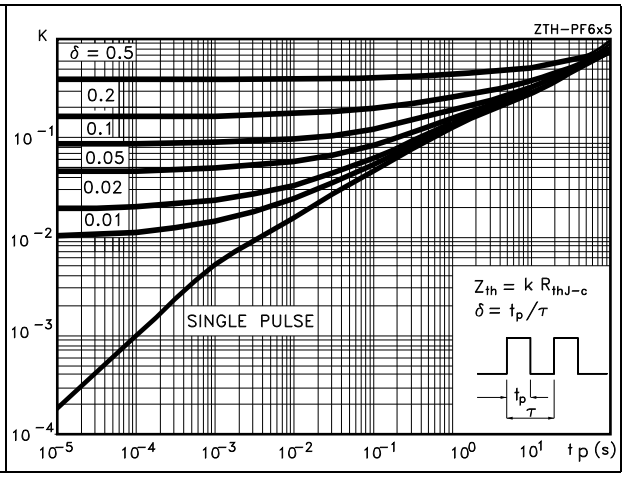


Figure 4. Output characteristics

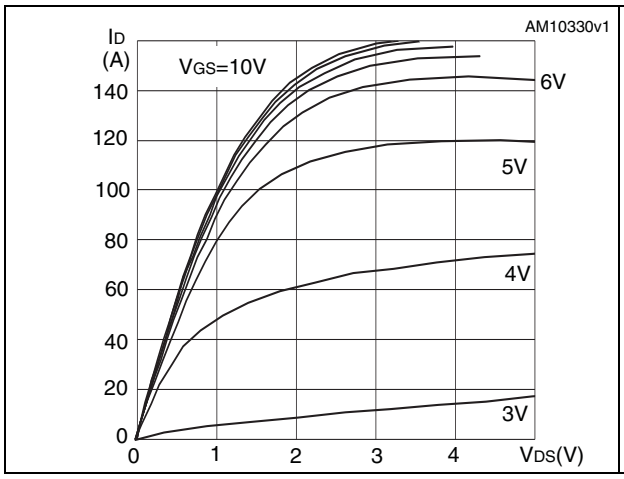


Figure 5. Transfer characteristics

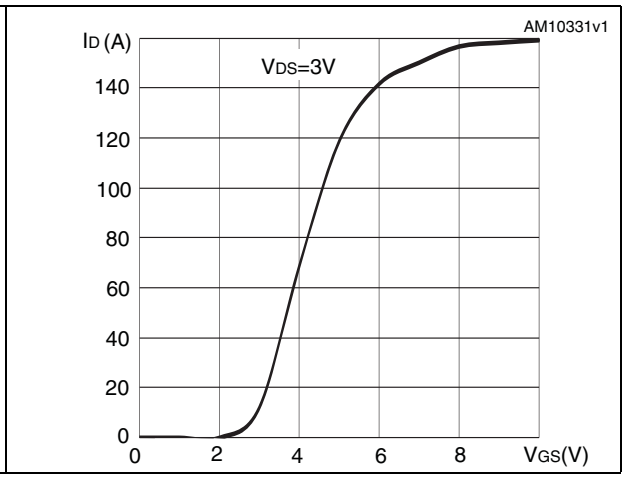


Figure 6. Normalized B_{VDSS} vs temperature

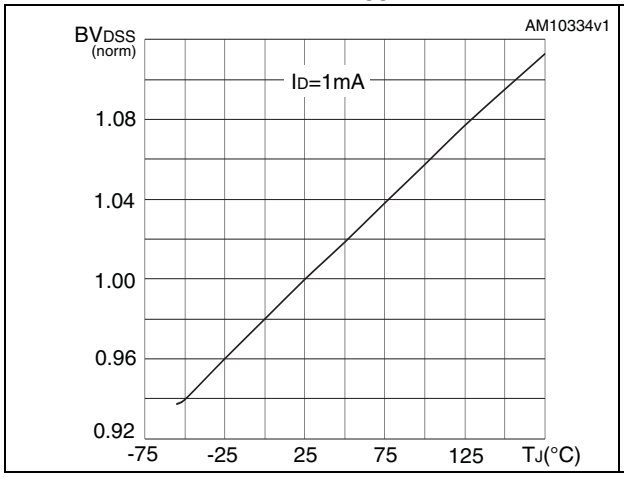


Figure 7. Static drain-source on-resistance

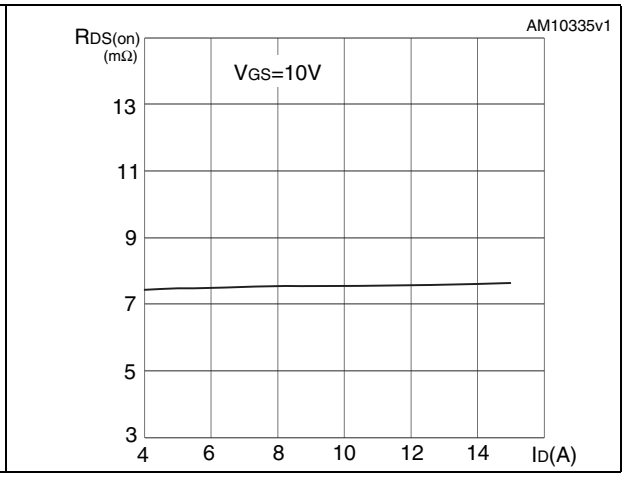


Figure 8. Gate charge vs gate-source voltage

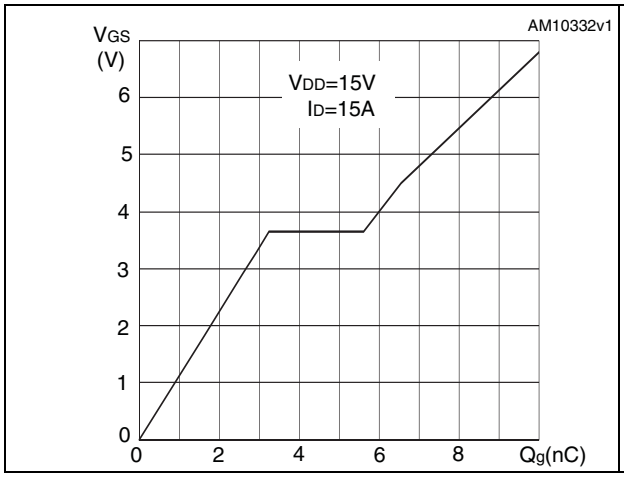


Figure 9. Capacitance variations

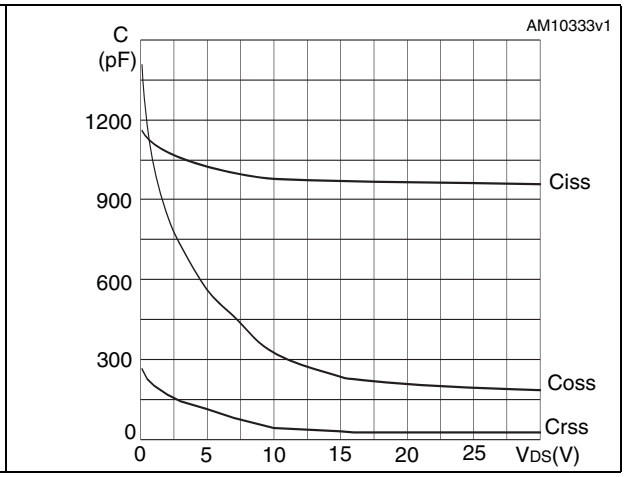


Figure 10. Normalized gate threshold voltage vs temperature

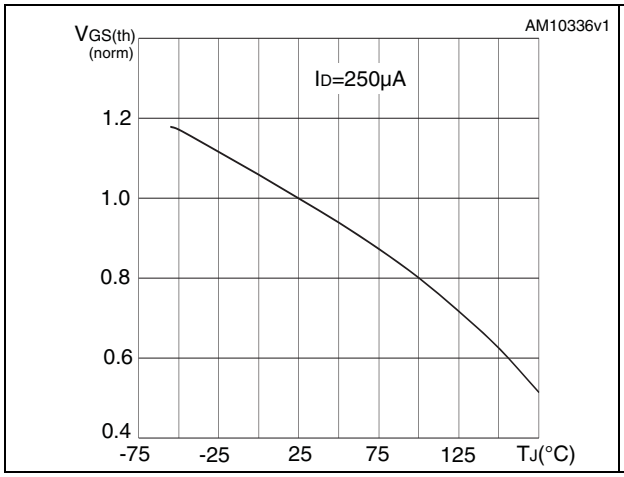


Figure 11. Normalized on resistance vs temperature

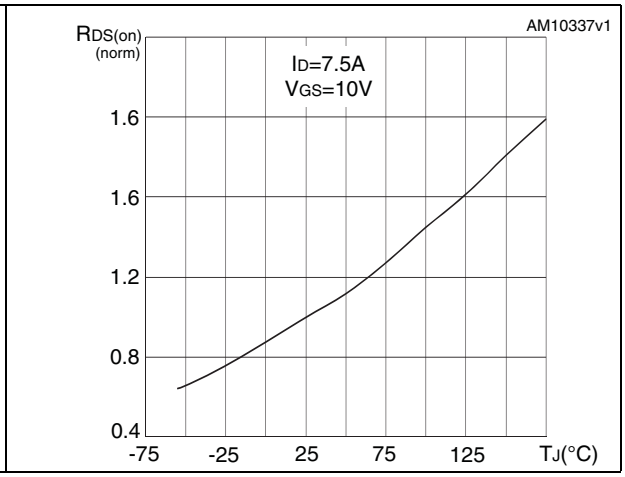
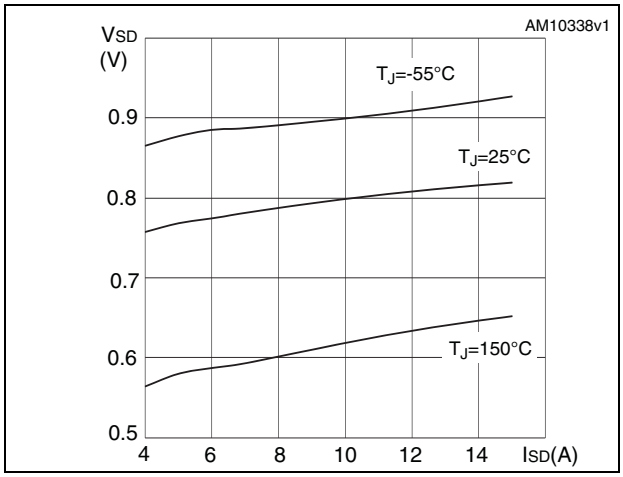


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

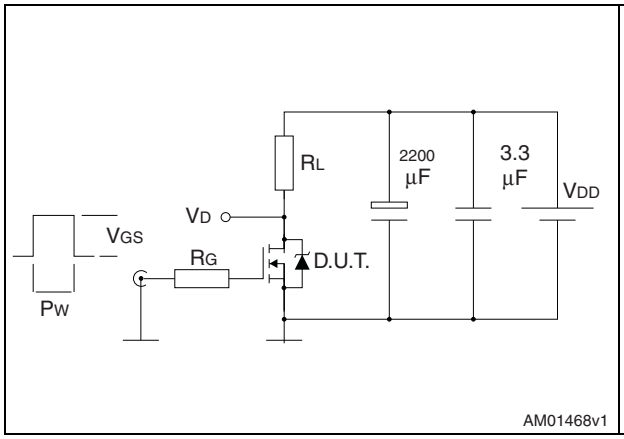


Figure 14. Gate charge test circuit

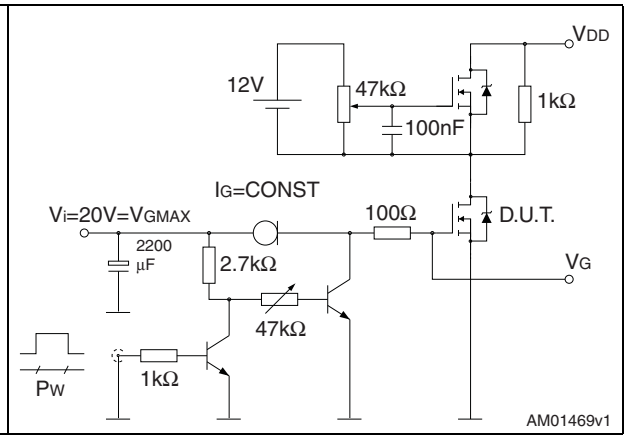


Figure 15. Test circuit for inductive load switching and diode recovery times

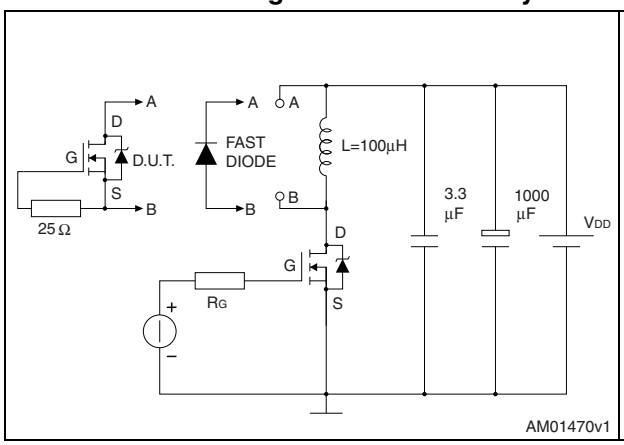


Figure 16. Unclamped inductive load test circuit

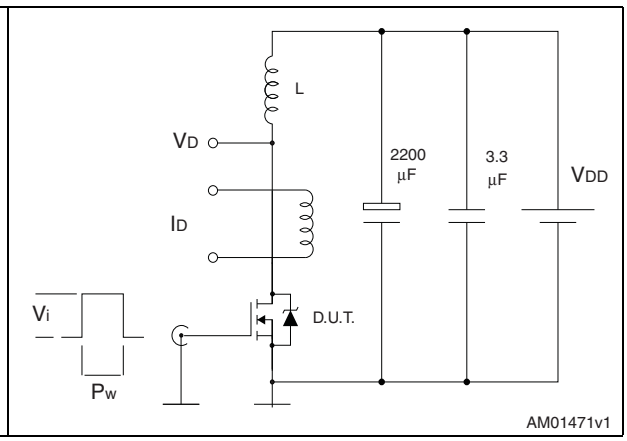


Figure 17. Unclamped inductive waveform

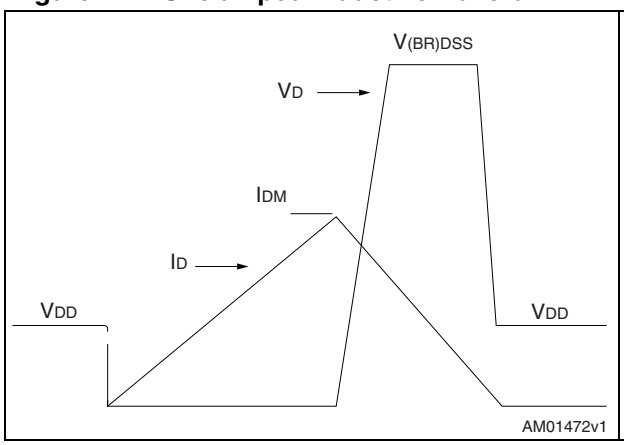
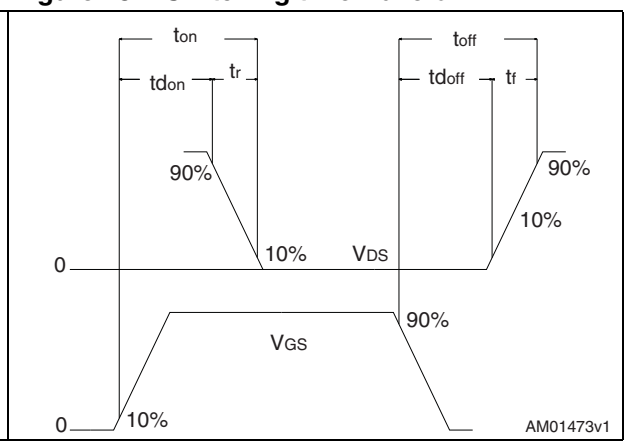


Figure 18. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. PowerFLAT™ 5x6 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D		5.20	
E		6.15	
D2	4.11		4.31
E2	3.50		3.70
e		1.27	
L	0.50		0.80
K	1.275		1.575

Figure 19. PowerFLAT™ 5x6 drawing

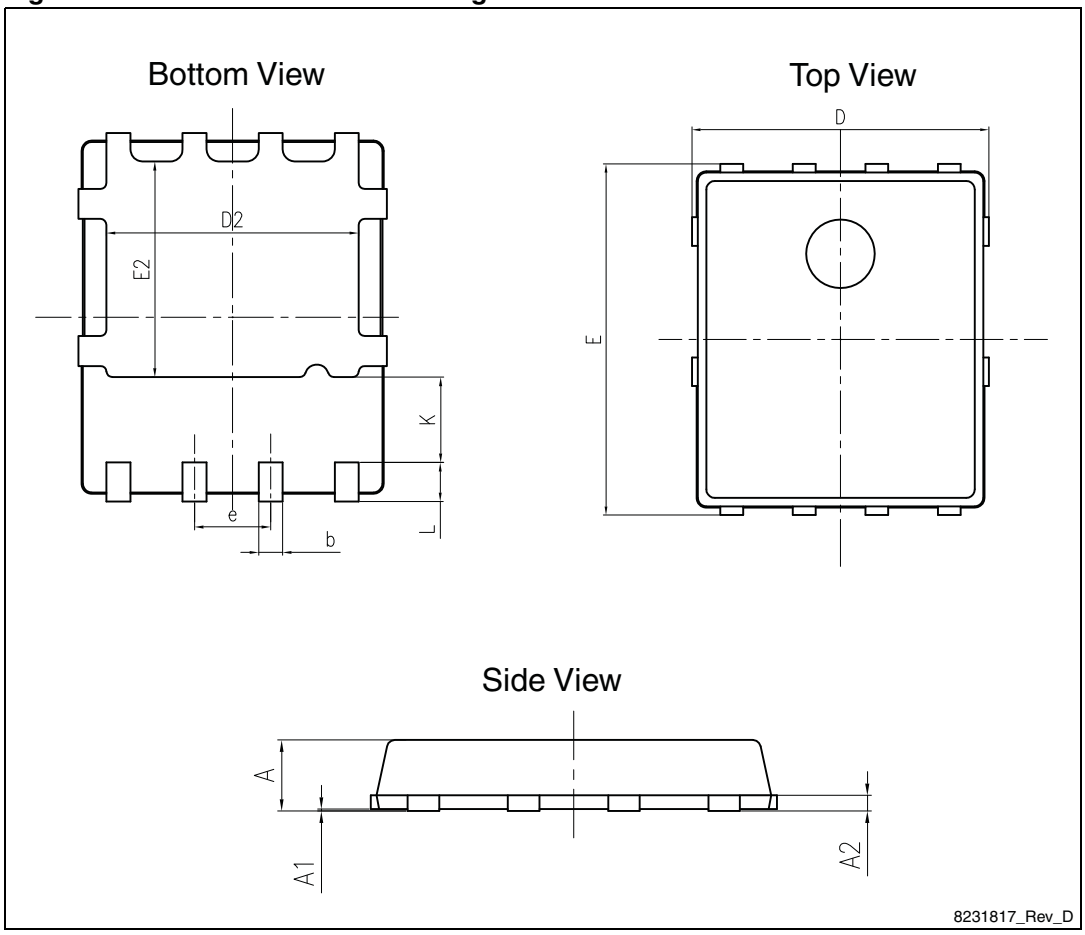
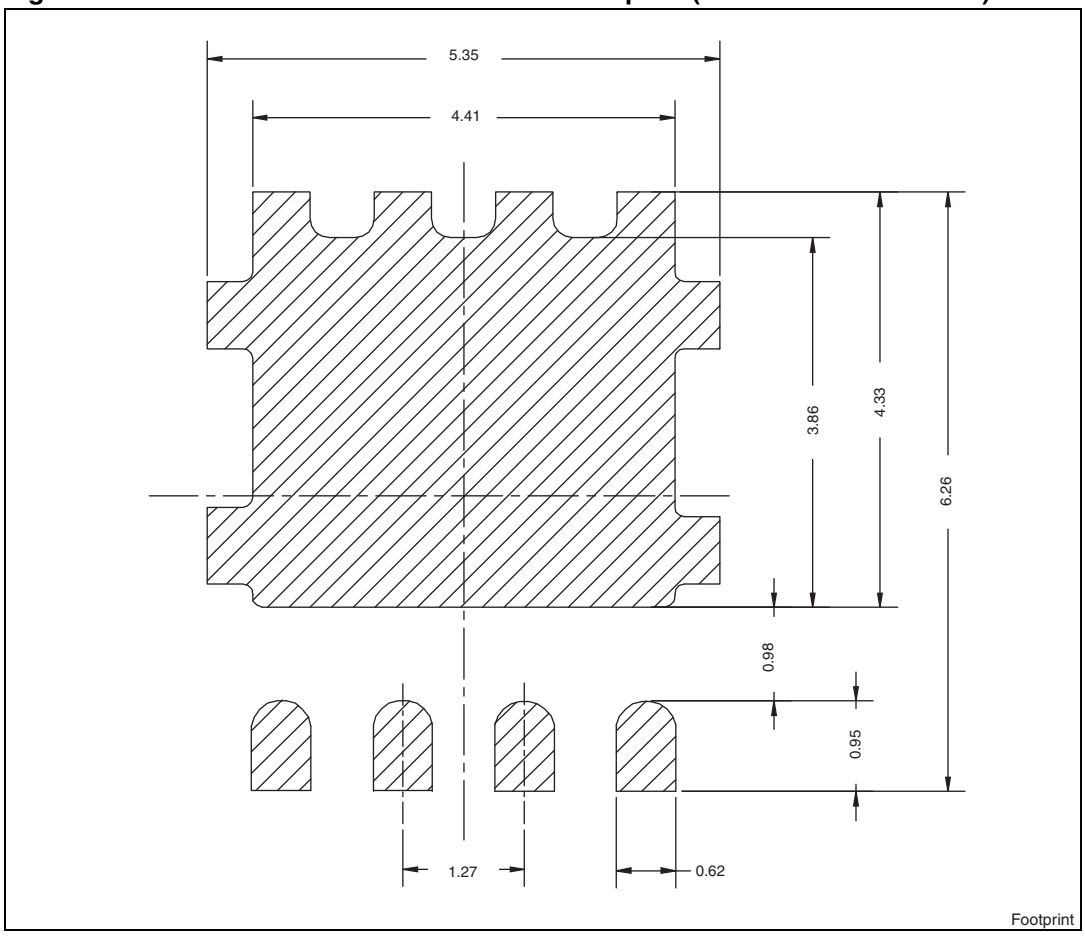


Figure 20. PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
24-Jan-2011	1	First release.
01-Jul-2011	2	Document status promoted from preliminary data to datasheet.
27-Apr-2012	3	Added E_{AS} value in *Table 2: Absolute maximum ratings*. Updated *Table 3: Thermal resistance*, *Table 4: On/off states*, *Table 5: Dynamic* and *Table 7: Source drain diode*. Minor text changes.

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