

N-Channel NexFET™ Power MOSFET

 Check for Samples: [CSD16415Q5](#)

FEATURES

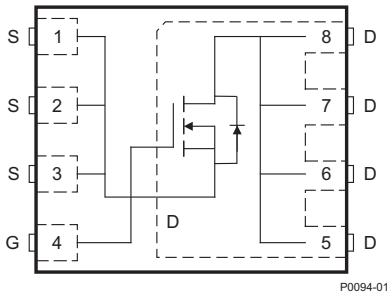
- **Ultralow Qg and Qgd**
- **Very Low On-Resistance**
- **Low Thermal Resistance**
- **Avalanche Rated**
- **Pb Free Terminal Plating**
- **RoHS Compliant**
- **Halogen Free**

APPLICATIONS

- **Point-of-Load Synchronous Buck Converter for Applications in Networking, Telecom and Computing Systems**
- **Optimized for Synchronous FET Applications**

DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion applications.

Top View


PRODUCT SUMMARY

V_{DS}	Drain-to-source voltage	25	V
Q_g	Gate charge, total (4.5 V)	21	nC
Q_{gd}	Gate charge, gate-to-drain	5.2	nC
$r_{DS(on)}$	Drain-to-source on-resistance	$V_{GS} = 4.5\text{ V}$	1.5 mΩ
		$V_{GS} = 10\text{ V}$	0.99 mΩ
$V_{GS(th)}$	Threshold voltage	1.5	V

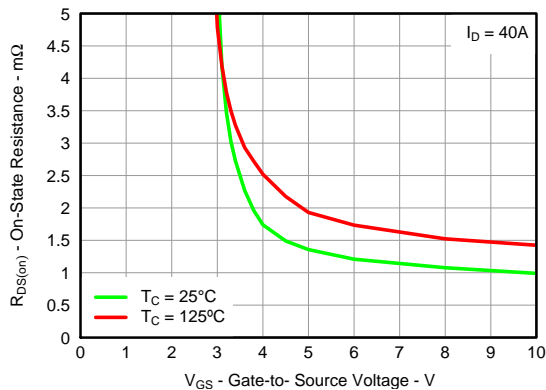
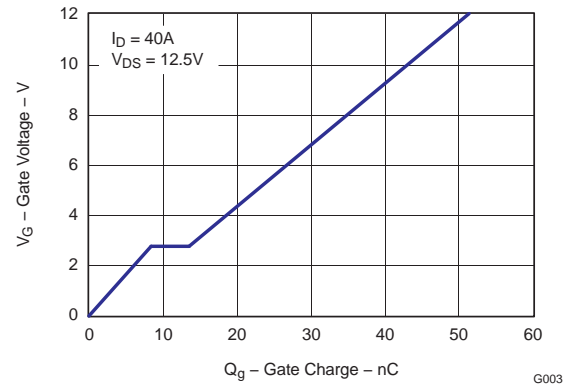
ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD16415Q5	SON 5-mm × 6-mm plastic package	13-inch (33-cm) reel	2500	Tape and reel

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ unless otherwise stated		VALUE	UNIT
V_{DS}	Drain-to-source voltage	25	V
V_{GS}	Gate-to-source voltage	+16/-12	V
I_D	Continuous drain current, $T_C = 25^\circ\text{C}$	100	A
	Continuous drain current ⁽¹⁾	38	A
I_{DM}	Pulsed drain current, $T_A = 25^\circ\text{C}$ ⁽²⁾	200	A
P_D	Power dissipation ⁽¹⁾	3.2	W
T_J, T_{STG}	Operating junction and storage temperature range	-55 to 150	$^\circ\text{C}$
E_{AS}	Avalanche energy, single-pulse $I_D = 100\text{ A}, L = 0.1\text{ mH}, R_G = 25\ \Omega$	500	mJ

- (1) $R_{\theta JA} = 40^\circ\text{C/W}$ on 1-in² (6.45-cm²) Cu [2 oz. (0.071-mm thick)] on 0.060-inch (1.52-mm) thick FR4 PCB.
- (2) Pulse duration $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$

 $r_{DS(on)}$ vs V_{GS}

Gate Charge


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NexFET is a trademark of Texas Instruments.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain-to-source voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	25			V
I_{DSS}	Drain-to-source leakage current	$V_{GS} = 0\text{ V}, V_{DS} = 20\text{ V}$			1	μA
I_{GSS}	Gate-to-source leakage current	$V_{DS} = 0\text{ V}, V_{GS} = -12\text{ V to } 16\text{ V}$			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1.2	1.5	1.9	V
$r_{DS(on)}$	Drain-to-source on-resistance	$V_{GS} = 4.5\text{ V}, I_D = 40\text{ A}$		1.5	1.8	$\text{m}\Omega$
		$V_{GS} = 10\text{ V}, I_D = 40\text{ A}$		0.99	1.15	$\text{m}\Omega$
g_{fs}	Transconductance	$V_{DS} = 15\text{ V}, I_D = 40\text{ A}$		168		S
Dynamic Characteristics						
C_{ISS}	Input capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 12.5\text{ V}, f = 1\text{ MHz}$		3150	4100	pF
C_{OSS}	Output capacitance			2530	3300	pF
C_{RSS}	Reverse transfer capacitance			175	230	pF
R_g	Series gate resistance			1.2	2.4	Ω
Q_g	Gate charge total (4.5 V)	$V_{DS} = 12.5\text{ V}, I_D = 40\text{ A}$		21	29	nC
Q_{gd}	Gate charge, gate-to-drain			5.2		nC
Q_{gs}	Gate charge, gate-to-source			8.3		nC
$Q_{g(th)}$	Gate charge at V_{th}			4.8		nC
Q_{OSS}	Output charge	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}$		55		nC
$t_{d(on)}$	Turnon delay time	$V_{DS} = 12.5\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 40\text{ A}$ $R_G = 2\ \Omega$		16.6		ns
t_r	Rise time			30		ns
$t_{d(off)}$	Turnoff delay time			20		ns
t_f	Fall time			12.7		ns
Diode Characteristics						
V_{SD}	Diode forward voltage	$I_S = 40\text{ A}, V_{GS} = 0\text{ V}$	0.85		1	V
Q_{rr}	Reverse recovery charge	$V_{DD} = 15\text{ V}, I_F = 40\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$		72		nC
t_{rr}	Reverse recovery time	$V_{DD} = 15\text{ V}, I_F = 40\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$		45		ns

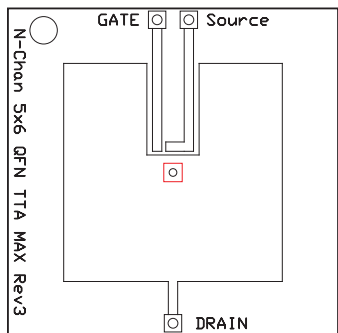
THERMAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal resistance, junction-to-case ⁽¹⁾			1.1	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal resistance, junction-to-ambient ^{(1) (2)}			50	$^\circ\text{C}/\text{W}$

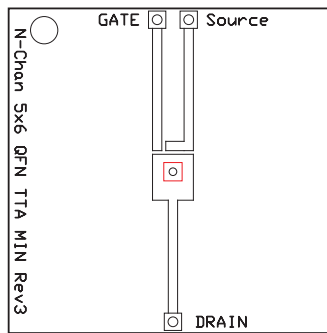
(1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch (2.54-cm) square, 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch \times 1.5-inch (3.81-cm \times 3.81-cm), 0.060-inch (1.52-mm) thick FR4 board. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.

(2) Device mounted on FR4 material with 1 inch² (6.45 cm²) of 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA} = 50^{\circ}\text{C/W}$
when mounted on 1
inch² (6.45 cm²) of
2-oz. (0.071-mm thick)
Cu.

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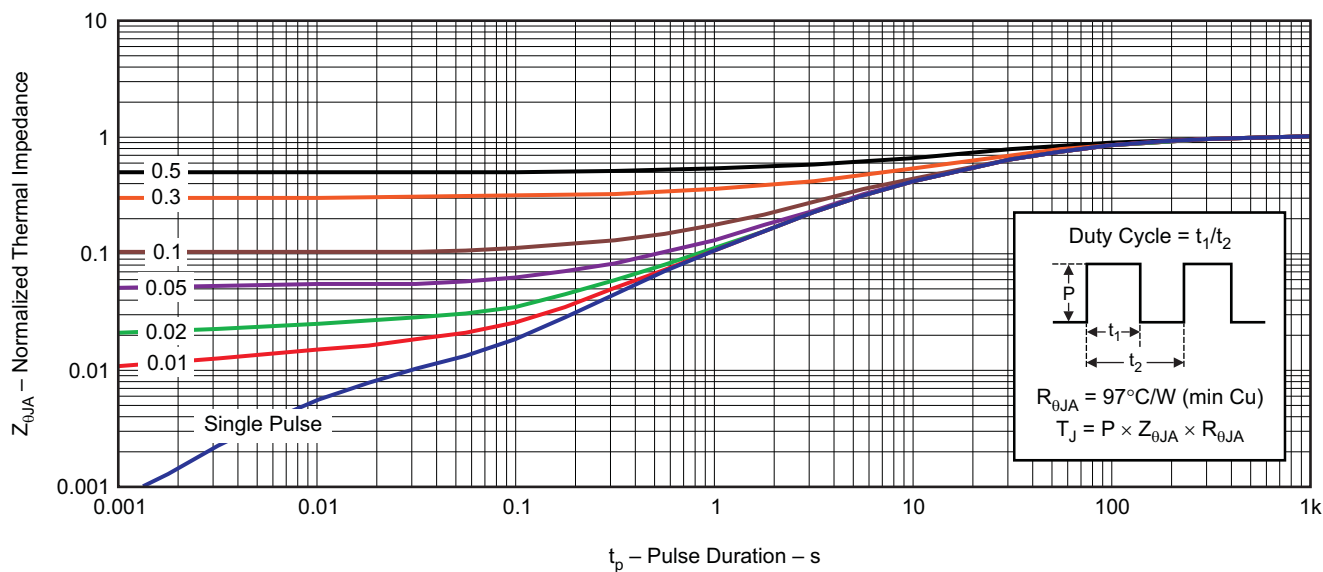


Max $R_{\theta JA} = 121^{\circ}\text{C/W}$
when mounted on
minimum pad area of
2-oz. (0.071-mm thick)
Cu.

M0137-02

TYPICAL MOSFET CHARACTERISTICS

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)



G012

Figure 1. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

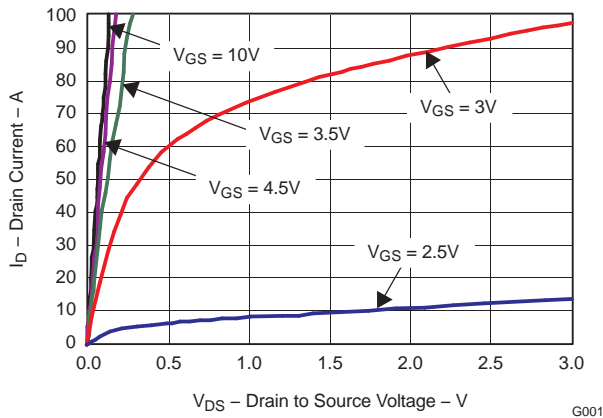


Figure 2. Saturation Characteristics

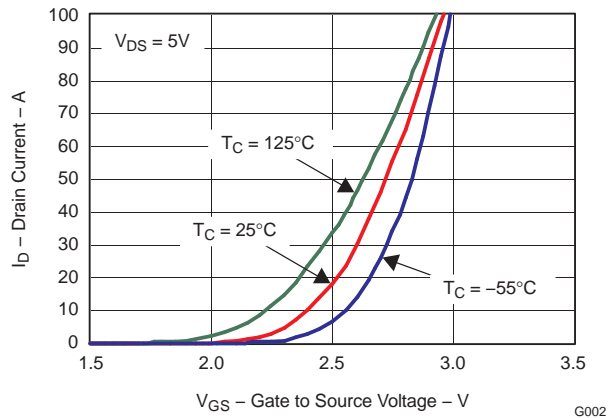


Figure 3. Transfer Characteristics

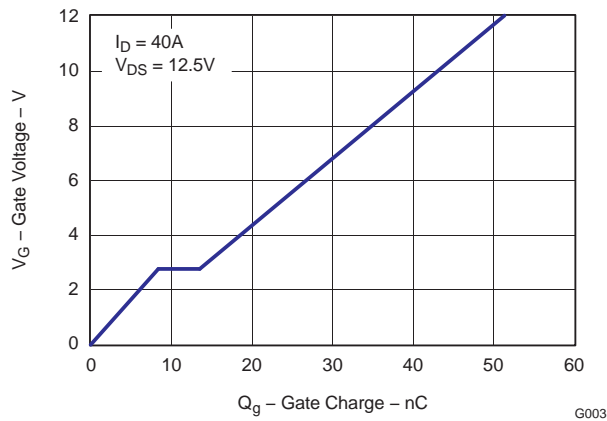


Figure 4. Gate Charge

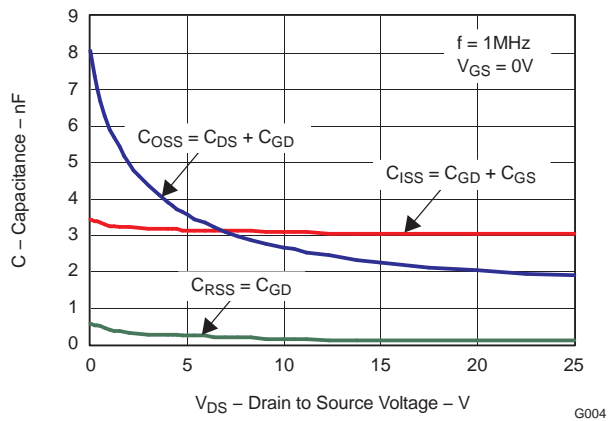


Figure 5. Capacitance

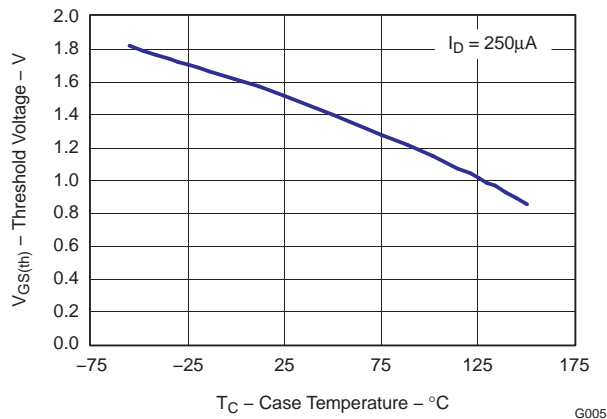


Figure 6. Threshold Voltage vs. Temperature

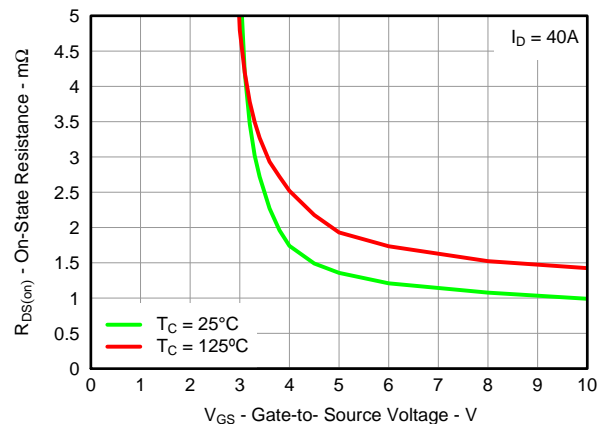


Figure 7. On-Resistance vs. Gate Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

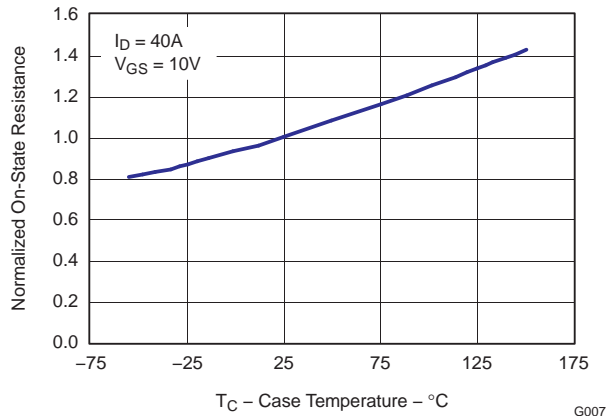


Figure 8. On-Resistance vs. Temperature

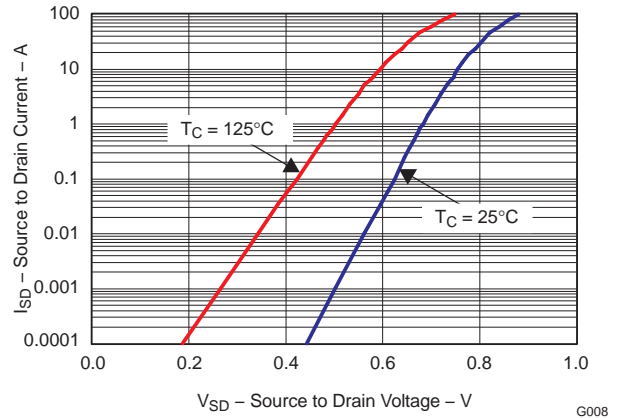


Figure 9. Typical Diode Forward Voltage

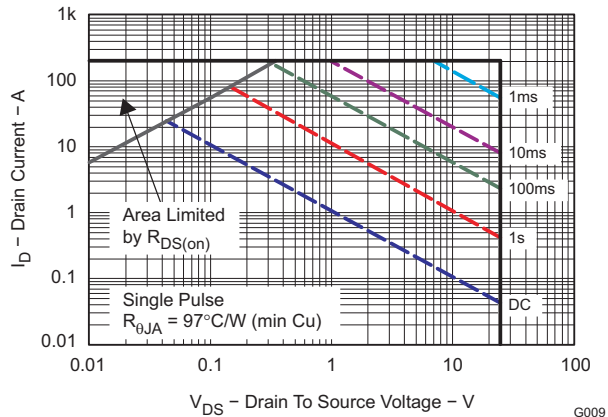


Figure 10. Maximum Safe Operating Area

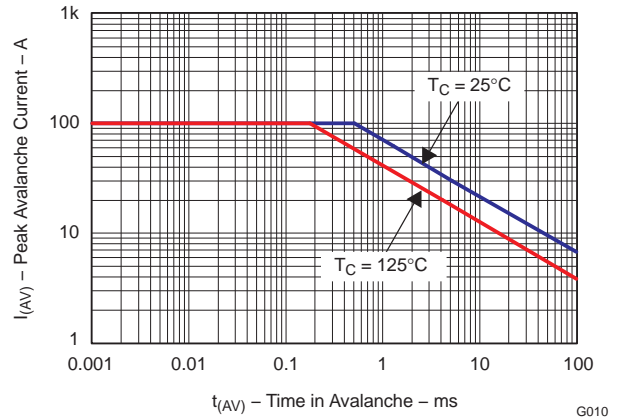


Figure 11. Single-Pulse Unclamped Inductive Switching

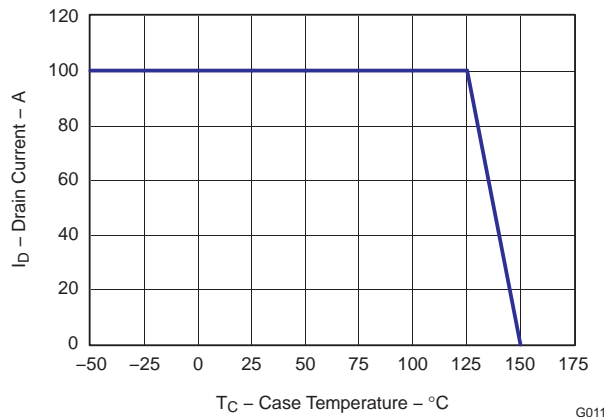
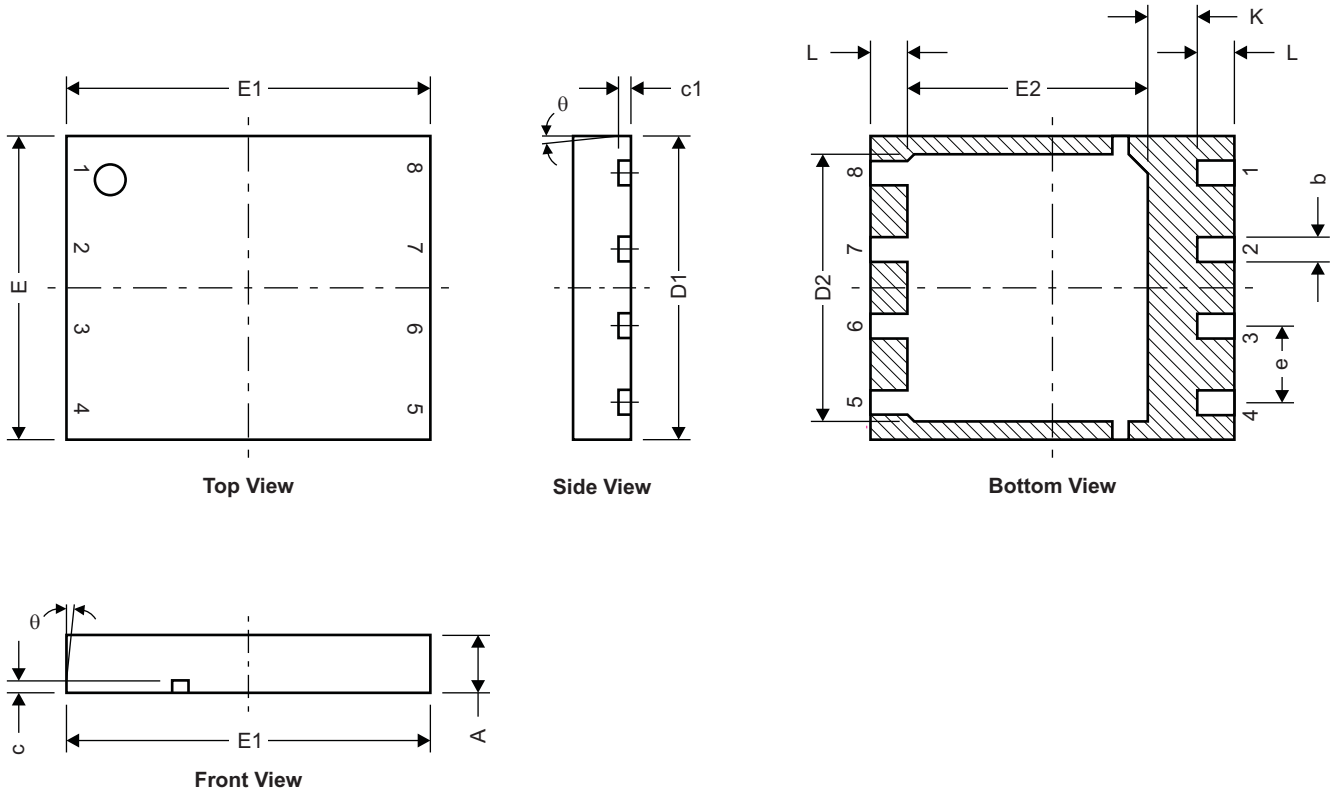


Figure 12. Maximum Drain Current vs. Temperature

MECHANICAL DATA

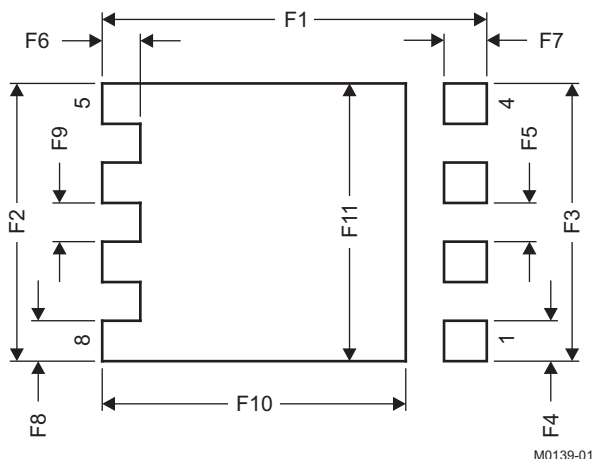
Q5 Package Dimensions



M0140-01

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.950	1.050	0.037	0.039
b	0.360	0.460	0.014	0.018
c	0.150	0.250	0.006	0.010
c1	0.150	0.250	0.006	0.010
D1	4.900	5.100	0.193	0.201
D2	4.320	4.520	0.170	0.178
E	4.900	5.100	0.193	0.201
E1	5.900	6.100	0.232	0.240
E2	3.920	4.12	0.154	0.162
e	1.27 TYP		0.050	
K	0.760		0.030	
L	0.510	0.710	0.020	0.028
θ	0.00			

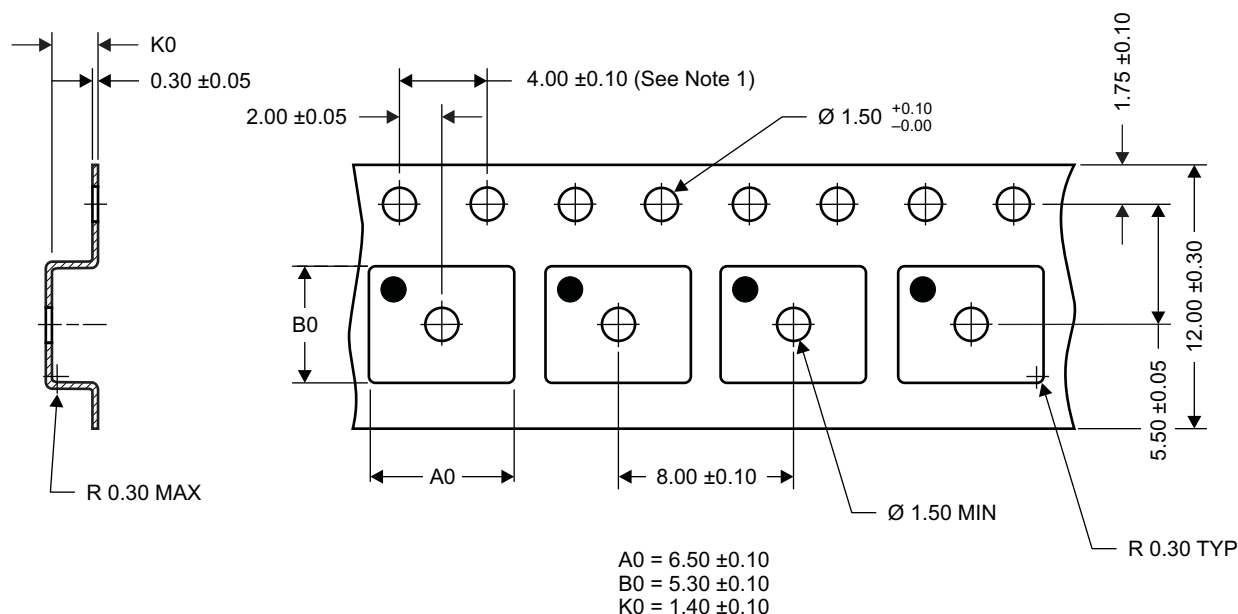
Figure 13. Recommended PCB Pattern



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F1	6.205	6.305	0.244	0.248
F2	4.460	4.560	0.176	0.180
F3	4.460	4.560	0.176	0.180
F4	0.650	0.700	0.026	0.028
F5	0.620	0.670	0.024	0.026
F6	0.630	0.680	0.025	0.027
F7	0.700	0.800	0.028	0.031
F8	0.650	0.700	0.026	0.028
F9	0.620	0.670	0.024	0.026
F10	4.900	5.000	0.193	0.197
F11	4.460	4.560	0.176	0.180

For recommended circuit layout for PCB designs, see application note [SLPA005 – Reducing Ringing Through PCB Layout Techniques](#).

Q5 Tape and Reel Information



M0138-01

Notes:

- 10 sprocket hole pitch cumulative tolerance ± 0.2
- Camber not to exceed 1 mm IN 100 mm, noncumulative over 250 mm
- Material: black static dissipative polystyrene
- All dimensions are in mm (unless otherwise specified)
- A0 and B0 measured on a plane 0.3 mm above the bottom of the pocket
- MSL1 260°C (IR and Convection) PbF Reflow Compatible

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
CSD16415Q5	ACTIVE	SON	DQH	8	2500	Pb-Free (RoHS Exempt)	CU SN	Level-1-260C-UNLIM	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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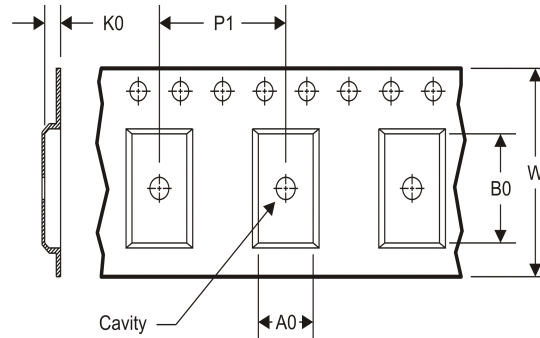
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TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD16415Q5	SON	DQH	8	2500	330.0	12.8	6.5	5.3	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

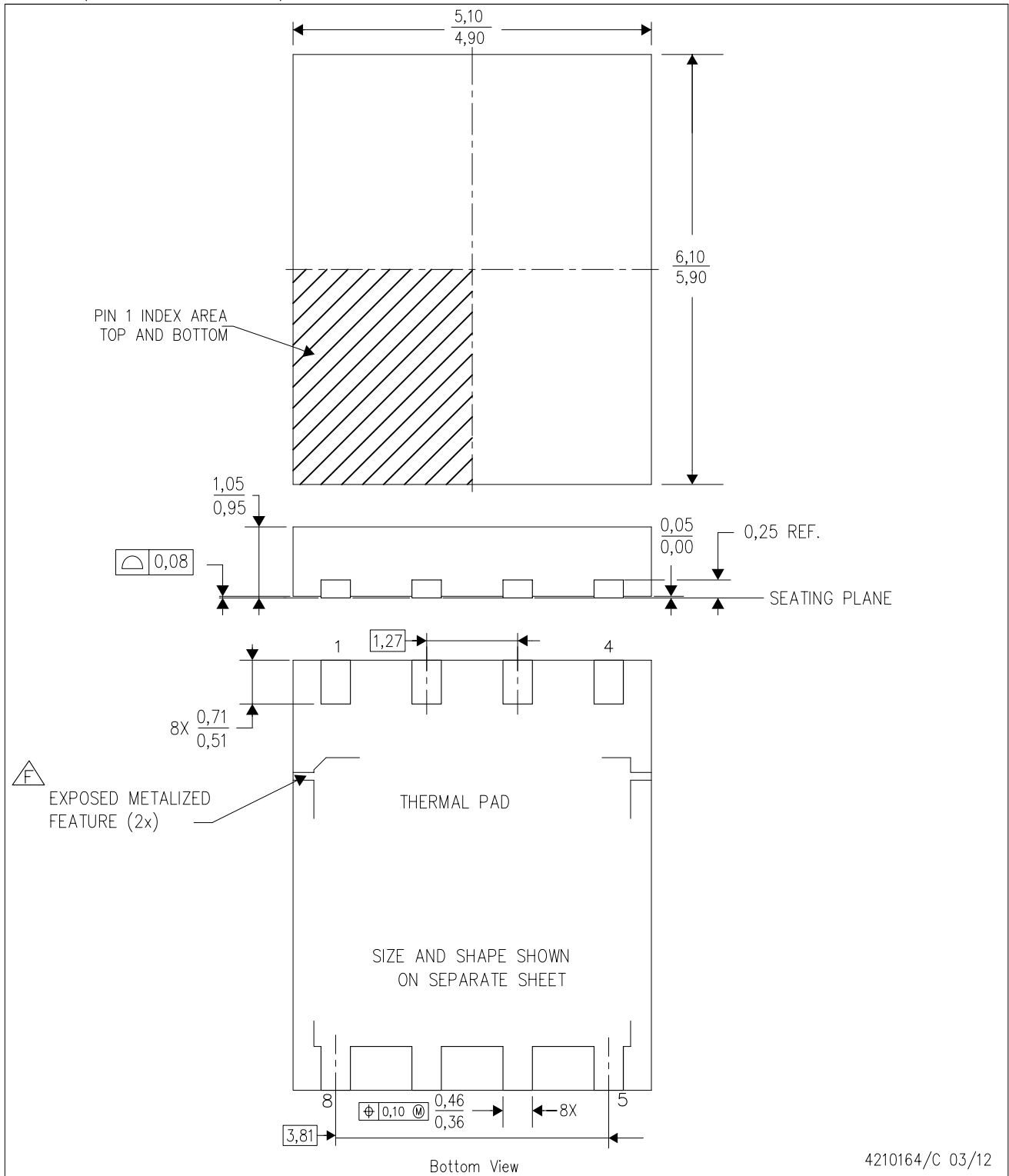



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD16415Q5	SON	DQH	8	2500	335.0	335.0	32.0

DQH (R-PVSON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Small Outline No-Lead (SON) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
-  Metalized features are supplier options and may not be on the package.

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