



## 30V, N-Channel NexFET™ Power MOSFETs

 Check for Samples: [CSD17310Q5A](#)

### FEATURES

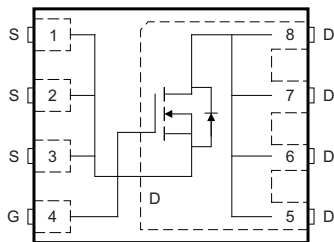
- Optimized for 5V Gate Drive
- Ultralow  $Q_g$  and  $Q_{gd}$
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5-mm × 6-mm Plastic Package

### APPLICATIONS

- Notebook Point of Load
- Point-of-Load Synchronous Buck in Networking, Telecom and Computing Systems
- Optimized for Synchronous FET Applications

### DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion applications, and optimized for 5V gate drive applications.

**Top View**


### PRODUCT SUMMARY

$V_{DS}$	Drain to Source Voltage	30	V
$Q_g$	Gate Charge Total (4.5V)	8.9	nC
$Q_{gd}$	Gate Charge Gate to Drain	2.1	nC
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 3V$	5.7 mΩ
		$V_{GS} = 4.5V$	4.5 mΩ
		$V_{GS} = 8V$	3.9 mΩ
$V_{GS(th)}$	Threshold Voltage	1.3	V

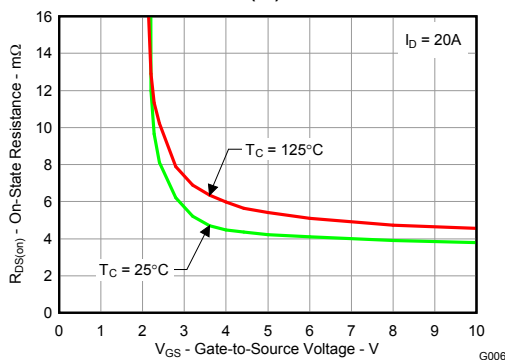
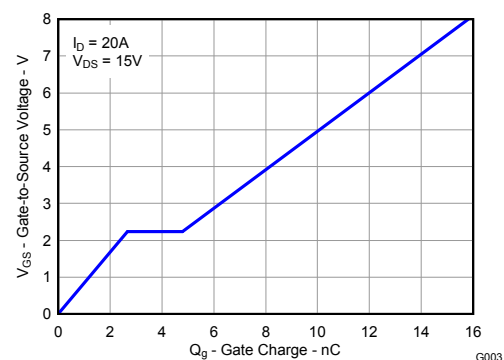
### ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD17310Q5A	SON 5-mm × 6-mm Plastic Package	13-Inch Reel	2500	Tape and Reel

### ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ unless otherwise stated		VALUE	UNIT
$V_{DS}$	Drain to Source Voltage	30	V
$V_{GS}$	Gate to Source Voltage	+10 / -8	V
$I_D$	Continuous Drain Current, $T_C = 25^\circ\text{C}$	100	A
	Continuous Drain Current <sup>(1)</sup>	21	A
$I_{DM}$	Pulsed Drain Current, $T_A = 25^\circ\text{C}$ <sup>(2)</sup>	134	A
$P_D$	Power Dissipation <sup>(1)</sup>	3.1	W
$T_J$ , $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$E_{AS}$	Avalanche Energy, single pulse $I_D = 58\text{A}$ , $L = 0.1\text{mH}$ , $R_G = 25\Omega$	168	mJ

- (1)  $R_{\theta JA} = 40^\circ\text{C/W}$  on 1-inch<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz. (0.071-mm thick) Cu pad on a 0.06-inch (1.52-mm) thick FR4 PCB.  
 (2) Pulse duration  $\leq 300\mu\text{s}$ , duty cycle  $\leq 2\%$

 **$R_{DS(on)}$  VS  $V_{GS}$** 

**GATE CHARGE**


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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ELECTRICAL CHARACTERISTICS

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Static Characteristics</b>						
$BV_{DSS}$	Drain to Source Voltage	$V_{GS} = 0V, I_D = 250\mu A$	30			V
$I_{DSS}$	Drain to Source Leakage Current	$V_{GS} = 0V, V_{DS} = 24V$			1	$\mu A$
$I_{GSS}$	Gate to Source Leakage Current	$V_{DS} = 0V, V_{GS} = +10/-8V$			100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	0.9	1.3	1.8	V
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 3V, I_D = 20A$		5.7	7.8	m $\Omega$
		$V_{GS} = 4.5V, I_D = 20A$		4.5	5.9	m $\Omega$
		$V_{GS} = 8V, I_D = 20A$		3.9	5.1	m $\Omega$
$g_{fs}$	Transconductance	$V_{DS} = 15V, I_D = 20A$		85		S
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{GS} = 0V, V_{DS} = 15V, f = 1MHz$		1200	1560	pF
$C_{oss}$	Output Capacitance			630	820	pF
$C_{rss}$	Reverse Transfer Capacitance			59	77	pF
$R_G$	Series Gate Resistance			0.9	1.8	$\Omega$
$Q_g$	Gate Charge Total (4.5V)	$V_{DS} = 15V, I_{DS} = 20A$		8.9	11.6	nC
$Q_{gd}$	Gate Charge Gate to Drain			2.1		nC
$Q_{gs}$	Gate Charge Gate to Source			2.7		nC
$Q_{g(th)}$	Gate Charge at $V_{th}$			1.4		nC
$Q_{oss}$	Output Charge	$V_{DS} = 12.8V, V_{GS} = 0V$		15.9		nC
$t_{d(on)}$	Turn On Delay Time	$V_{DS} = 15V, V_{GS} = 4.5V, I_{DS} = 20A, R_G = 2\Omega$		6.5		ns
$t_r$	Rise Time			11.6		ns
$t_{d(off)}$	Turn Off Delay Time			15		ns
$t_f$	Fall Time			5		ns
<b>Diode Characteristics</b>						
$V_{SD}$	Diode Forward Voltage	$I_{SD} = 20A, V_{GS} = 0V$		0.85	1	V
$Q_{rr}$	Reverse Recovery Charge	$V_{DD} = 12.8V, I_F = 20A, di/dt = 300A/\mu s$		21		nC
$t_{rr}$	Reverse Recovery Time			22		ns

## THERMAL CHARACTERISTICS

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

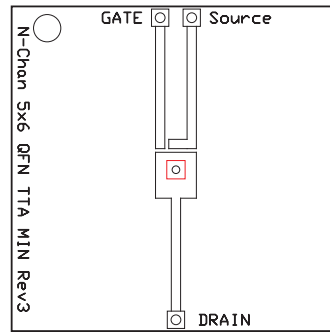
PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case <sup>(1)</sup>			1.9	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient <sup>(1)(2)</sup>			51	$^\circ\text{C/W}$

- $R_{\theta JC}$  is determined with the device mounted on a 1-inch<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch x 1.5-inch (3.81-cm x 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB.  $R_{\theta JC}$  is specified by design, whereas  $R_{\theta JA}$  is determined by the user's board design.
- Device mounted on FR4 material with 1-inch<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz. (0.071-mm thick) Cu.



M0137-01

Max  $R_{\theta JA} = 51^{\circ}\text{C/W}$   
when mounted on  
1 inch<sup>2</sup> (6.45 cm<sup>2</sup>) of  
2-oz. (0.071-mm thick)  
Cu.

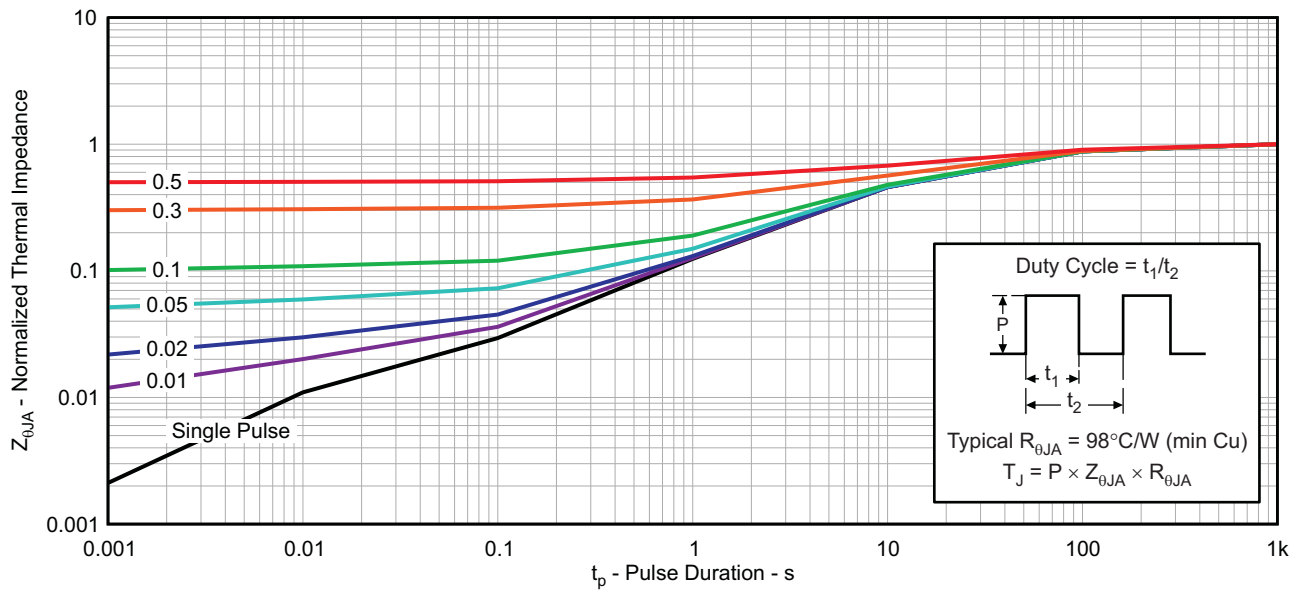


M0137-02

Max  $R_{\theta JA} = 123^{\circ}\text{C/W}$   
when mounted on a  
minimum pad area of  
2-oz. (0.071-mm thick)  
Cu.

### TYPICAL MOSFET CHARACTERISTICS

( $T_A = 25^{\circ}\text{C}$  unless otherwise stated)

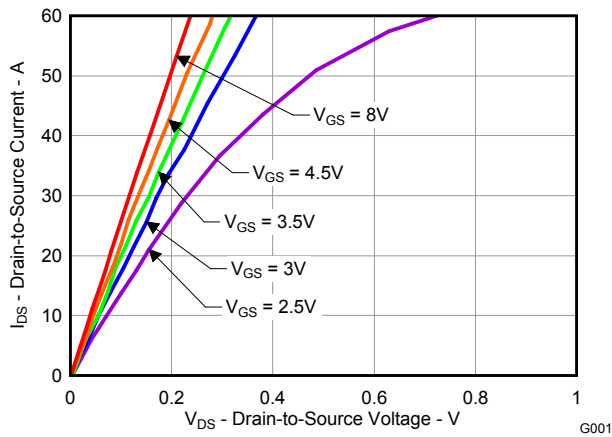


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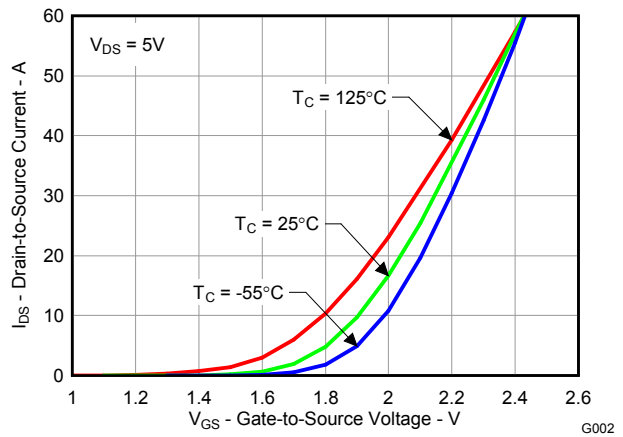
Figure 1. Transient Thermal Impedance

**TYPICAL MOSFET CHARACTERISTICS (continued)**

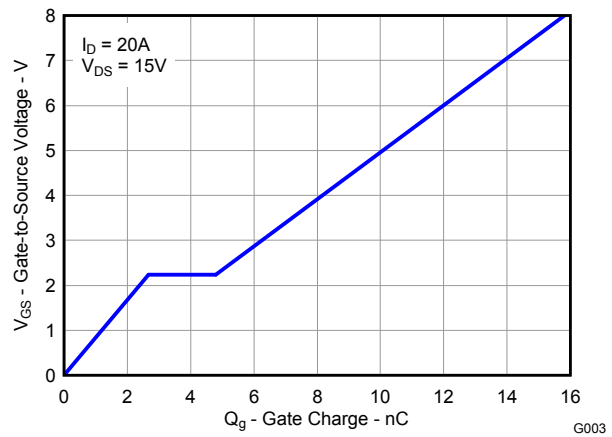
( $T_A = 25^\circ\text{C}$  unless otherwise stated)



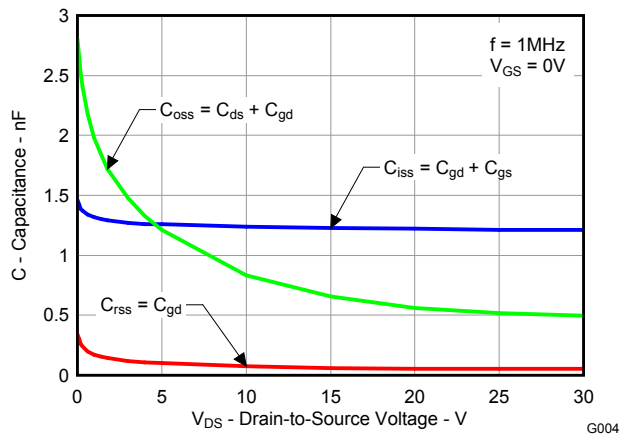
**Figure 2. Saturation Characteristics**



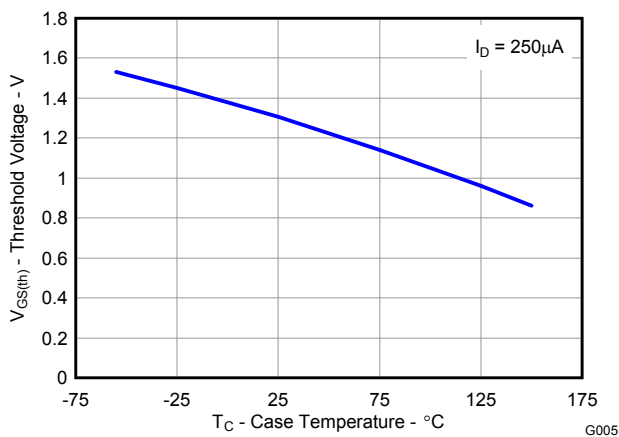
**Figure 3. Transfer Characteristics**



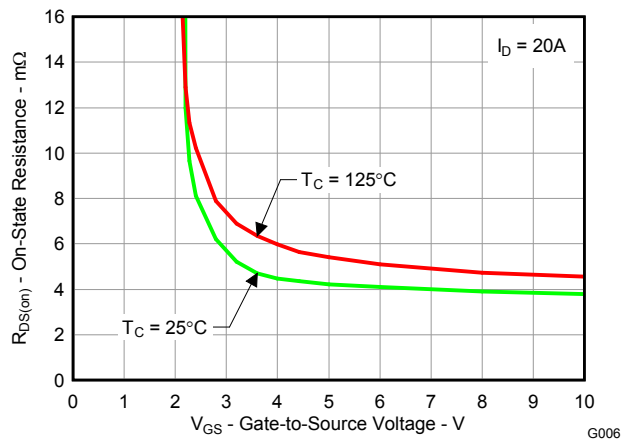
**Figure 4. Gate Charge**



**Figure 5. Capacitance**



**Figure 6. Threshold Voltage vs. Temperature**



**Figure 7. On-State Resistance vs. Gate-to-Source Voltage**

TYPICAL MOSFET CHARACTERISTICS (continued)

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

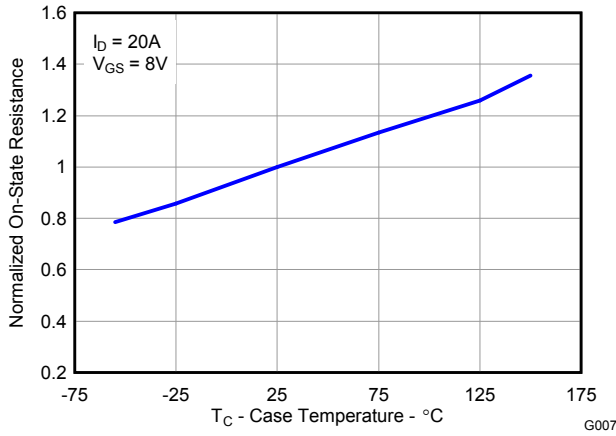


Figure 8. Normalized On-State Resistance vs. Temperature

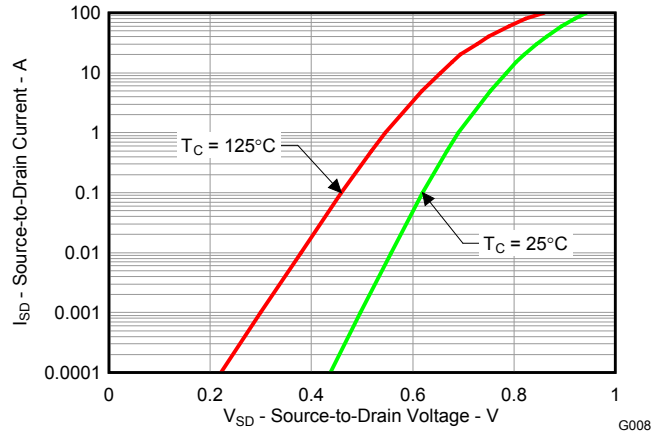


Figure 9. Typical Diode Forward Voltage

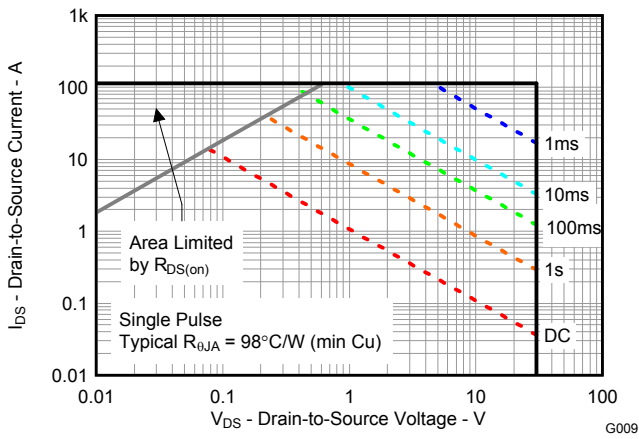


Figure 10. Maximum Safe Operating Area

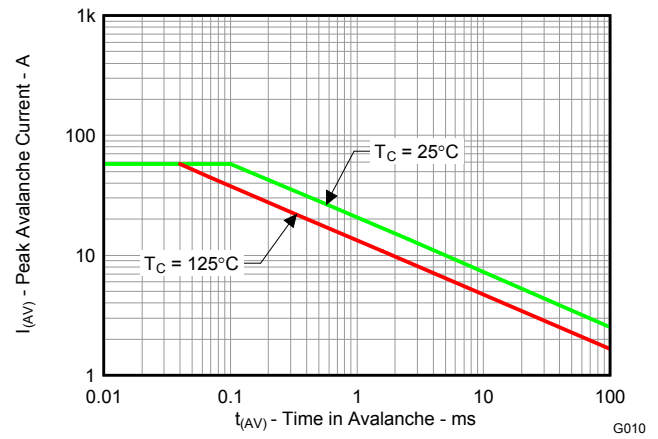


Figure 11. Single Pulse Unclamped Inductive Switching

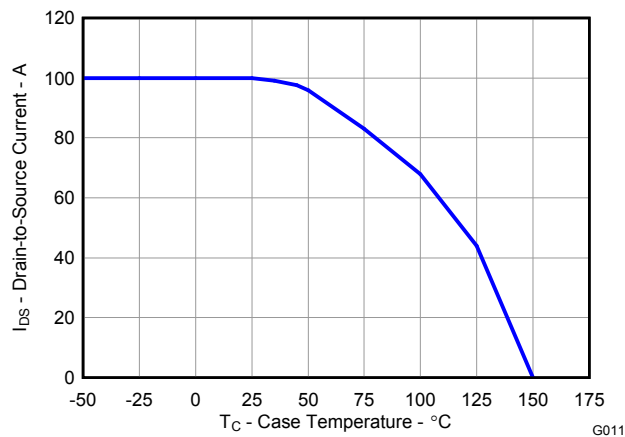


Figure 12. Maximum Drain Current vs. Temperature

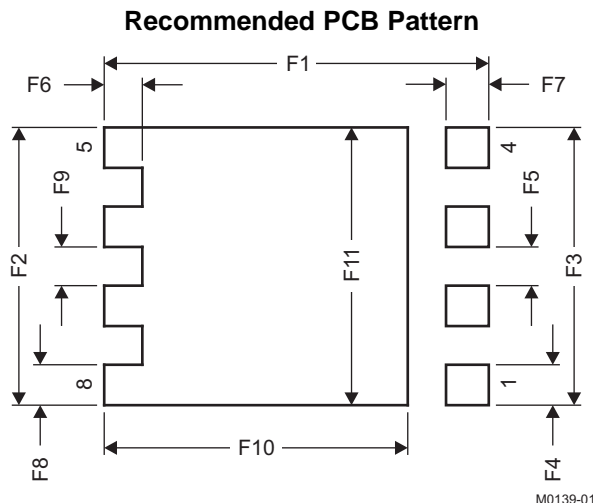
**MECHANICAL DATA**

**Q5A Package Dimensions**



M0135-01

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
b	0.33	0.41	0.51
c	0.20	0.25	0.34
D1	4.80	4.90	5.00
D2	3.61	3.81	4.02
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.17	1.27	1.37
H	0.41	0.56	0.71
K	1.10		
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
$\theta$	0°		12°



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F1	6.205	6.305	0.244	0.248
F2	4.46	4.56	0.176	0.18
F3	4.46	4.56	0.176	0.18
F4	0.65	0.7	0.026	0.028
F5	0.62	0.67	0.024	0.026
F6	0.63	0.68	0.025	0.027
F7	0.7	0.8	0.028	0.031
F8	0.65	0.7	0.026	0.028
F9	0.62	0.67	0.024	0.026
F10	4.9	5	0.193	0.197
F11	4.46	4.56	0.176	0.18

For recommended circuit layout for PCB designs, see application note [SLPA005 – Reducing Ringing Through PCB Layout Techniques](#).

### Q5A Tape and Reel Information



M0138-01

### Notes:

- 10-sprocket hole-pitch cumulative tolerance ±0.2
- Camber not to exceed 1mm in 100mm, noncumulative over 250mm
- Material: black static-dissipative polystyrene
- All dimensions are in mm (unless otherwise specified)
- A0 and B0 measured on a plane 0.3mm above the bottom of the pocket

## REVISION HISTORY

Changes from Original (February 2010) to Revision A	Page
• Updated the Q5A Package Dimensions table. DIM c MAX was 0.30, DIM D2 MAX was 3.96, DIM e MIN was blank MAX was blank, DIM H NOM was 0.51 MAX was 0.61 .....	6
• Deleted Note 6 from the Q5A Tape and Reel Information - "MSL1 260°C (IR and convection) PbF reflow compatible" .....	7
• Deleted the Package Marking Information section .....	7



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD17310Q5A	SON	DQJ	8	2500	330.0	12.4	6.3	5.3	1.2	8.0	12.0	Q1
CSD17310Q5A	SON	DQJ	8	2500	330.2	12.4	6.5	5.3	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD17310Q5A	SON	DQJ	8	2500	340.0	340.0	38.0
CSD17310Q5A	SON	DQJ	8	2500	347.0	342.0	55.0

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### Applications

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Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
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