# N-Channel NexFET™ Power MOSFET

**Check for Samples: CSD16404Q5A**

## FEATURES

- **Ultralow $Q_g$ and $Q_{gd}$**
- **Low Thermal Resistance**
- **Avalanche Rated**
- **Pb Free Terminal Plating**
- **RoHS Compliant**
- **Halogen Free**
- **SON 5-mm × 6-mm Plastic Package**

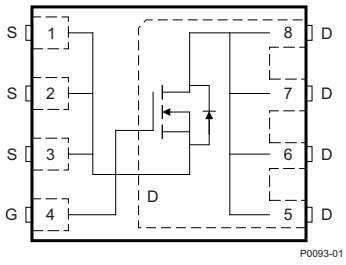
## APPLICATIONS

- **Point-of-Load Synchronous Buck Converter for Applications in Networking, Telecom and Computing Systems**
- **Optimized for Control FET Applications**

## DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion applications.

### Top View




## PRODUCT SUMMARY

| | | | | |
|---|---|---|---|---|
| $V_{DS}$ | Drain to Source Voltage | 25 | | V |
| $Q_g$ | Gate Charge Total (4.5V) | 6.5 | | nC |
| $Q_{gd}$ | Gate Charge Gate to Drain | 1.7 | | nC |
| $R_{DS(on)}$ | Drain to Source On Resistance | $V_{GS}$ = 4.5V | 5.7 | mΩ |
| | | $V_{GS}$ = 10V | 4.1 | mΩ |
| $V_{GS(th)}$ | Threshold Voltage | 1.8 | | V |

## ORDERING INFORMATION

| Device | Package | Media | Qty | Ship |
|---|---|---|---|---|
| CSD16404Q5A | SON 5-mm × 6-mm Plastic Package | 13-Inch Reel | 2500 | Tape and Reel |

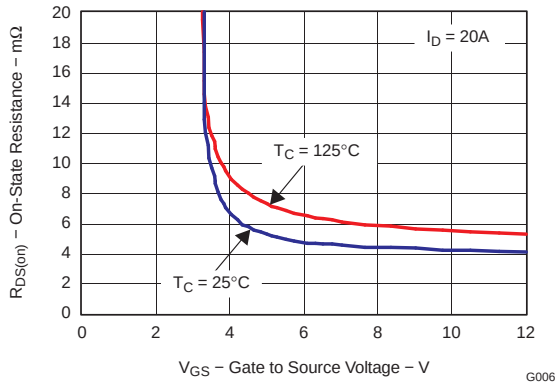
## ABSOLUTE MAXIMUM RATINGS

| $T_A$ = 25°C unless otherwise stated | | VALUE | UNIT |
|---|---|---|---|
| $V_{DS}$ | Drain to Source Voltage | 25 | V |
| $V_{GS}$ | Gate to Source Voltage | +16 / –12 | V |
| $I_D$ | Continuous Drain Current, $T_C$ = 25°C | 81 | A |
| | Continuous Drain Current(1) | 21 | A |
| $I_{DM}$ | Pulsed Drain Current, $T_A$ = 25°C(2) | 135 | A |
| $P_D$ | Power Dissipation(1) | 3 | W |
| $T_J$, $T_{STG}$ | Operating Junction and Storage Temperature Range | –55 to 150 | °C |
| $E_{AS}$ | Avalanche Energy, single pulse $I_D$ = 40A, L = 0.1mH, $R_G$ = 25Ω | 80 | mJ |

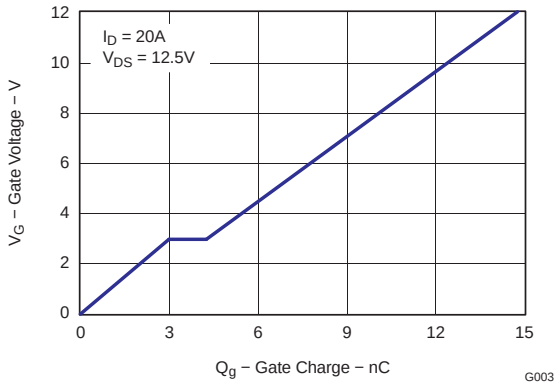
(1) $R_{\theta JA}$ = 41°C/W on 1-inch$^2$ (6.45-cm$^2$), 2-oz. (0.071-mm thick) Cu pad on a 0.06-inch (1.52-mm) thick FR4 PCB.

(2) Pulse duration ≤300μs, duty cycle ≤2%

### $R_{DS(on)}$ vs $V_{GS}$




### GATE CHARGE

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NexFET is a trademark of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ELECTRICAL CHARACTERISTICS

$T_A$ = 25°C, unless otherwise specified

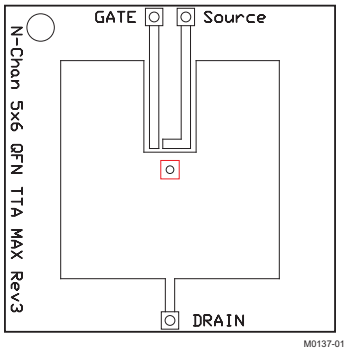
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Static Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain to Source Voltage | $V_{GS}$ = 0V, $I_D$ = 250μA | 25 | | | V |
| $I_{DSS}$ | Drain to Source Leakage Current | $V_{GS}$ = 0V, $V_{DS}$ = 20V | | | 1 | μA |
| $I_{GSS}$ | Gate to Source Leakage Current | $V_{DS}$ = 0V, $V_{GS}$ = +16/-12V | | | 100 | nA |
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250μA | 1.4 | 1.8 | 2.1 | V |
| $R_{DS(on)}$ | Drain to Source On Resistance | $V_{GS}$ = 4.5V, $I_D$ = 20A | | 5.7 | 7.2 | mΩ |
| | | $V_{GS}$ = 10V, $I_D$ = 20A | | 4.1 | 5.1 | mΩ |
| $g_{fs}$ | Transconductance | $V_{DS}$ = 15V, $I_D$ = 20A | | 57 | | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{ISS}$ | Input Capacitance | $V_{GS}$ = 0V, $V_{DS}$ = 12.5V , f = 1MHz | | 940 | 1220 | pF |
| $C_{OSS}$ | Output Capacitance | | | 810 | 1050 | pF |
| $C_{RSS}$ | Reverse Transfer Capacitance | | | 62 | 80 | pF |
| $R_g$ | Series Gate Resistance | | | 0.9 | 1.8 | Ω |
| $Q_g$ | Gate Charge Total (4.5V) | $V_{DS}$ = 12.5V, $I_D$ = 20A | | 6.5 | 8.5 | nC |
| $Q_{gd}$ | Gate Charge Gate to Drain | | | 1.7 | | nC |
| $Q_{gs}$ | Gate Charge Gate to Source | | | 3 | | nC |
| $Q_{g(th)}$ | Gate Charge at Vth | | | 1.5 | | nC |
| $Q_{OSS}$ | Output Charge | $V_{DS}$ = 13V, $V_{GS}$ = 0V | | 16 | | nC |
| $t_{d(on)}$ | Turn On Delay Time | $V_{DS}$ = 12.5V, $V_{GS}$ = 4.5V, $I_D$ = 20A, $R_G$ = 2Ω | | 7.8 | | ns |
| $t_r$ | Rise Time | | | 13.4 | | ns |
| $t_{d(off)}$ | Turn Off Delay Time | | | 8.4 | | ns |
| $t_f$ | Fall Time | | | 4.6 | | ns |
| **Diode Characteristics** | | | | | | |
| $V_{SD}$ | Diode Forward Voltage | $I_S$ = 20A, $V_{GS}$ = 0V | | 0.85 | 1 | V |
| $Q_{rr}$ | Reverse Recovery Charge | $V_{DD}$ = 13V, $I_F$ = 20A, di/dt = 300A/μs | | 20 | | nC |
| $t_{rr}$ | Reverse Recovery Time | $V_{DD}$ = 13V, $I_F$ = 20A, di/dt = 300A/μs | | 22 | | ns |

## THERMAL CHARACTERISTICS

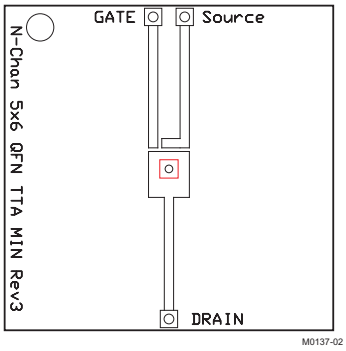
$T_A$ = 25°C, unless otherwise specified

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance Junction to Case(1) | | | 3.3 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance Junction to Ambient(1) (2) | | | 52 | °C/W |

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch$^2$ (6.45-cm$^2$), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1-inch$^2$ (6.45-cm$^2$), 2-oz. (0.071-mm thick) Cu.




Max $R_{\theta JA}$ = 52°C/W when mounted on 1 inch$^2$ (6.45 cm$^2$) of 2-oz. (0.071-mm thick) Cu.




Max $R_{\theta JA}$ = 120°C/W when mounted on minimum pad area of 2-oz. (0.071-mm thick) Cu.

## TYPICAL MOSFET CHARACTERISTICS

$T_A$ = 25°C, unless otherwise specified

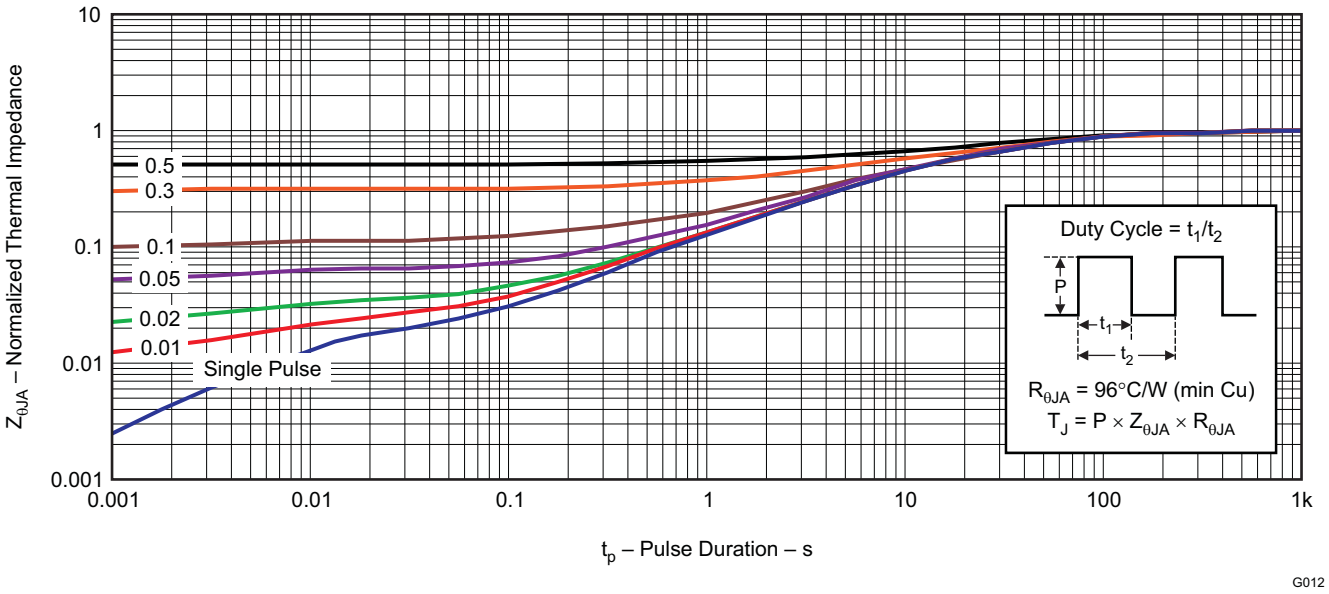



**Figure 1. Transient Thermal Impedance**

## TYPICAL MOSFET CHARACTERISTICS (continued)

$T_A$ = 25°C, unless otherwise specified

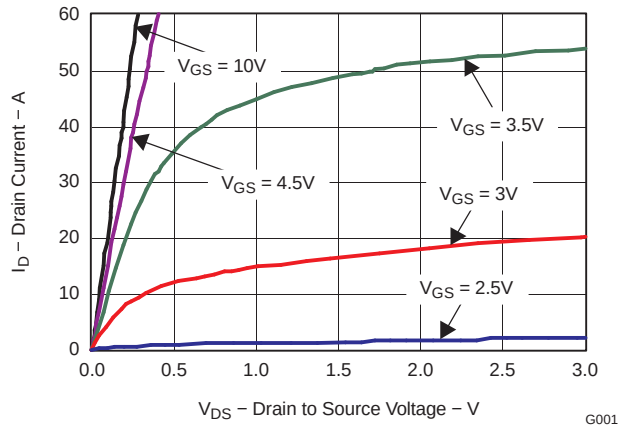



**Figure 2. Saturation Characteristics**

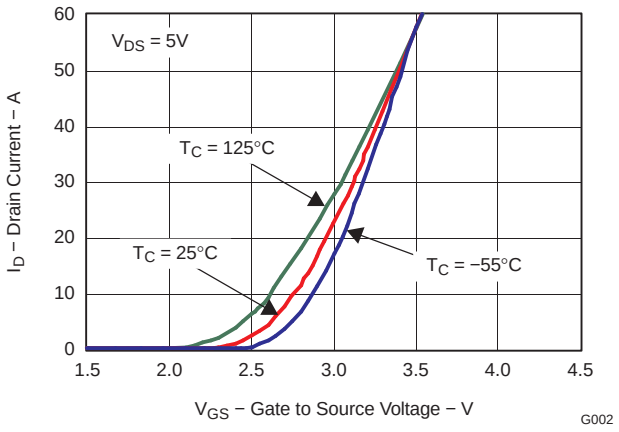



**Figure 3. Transfer Characteristics**

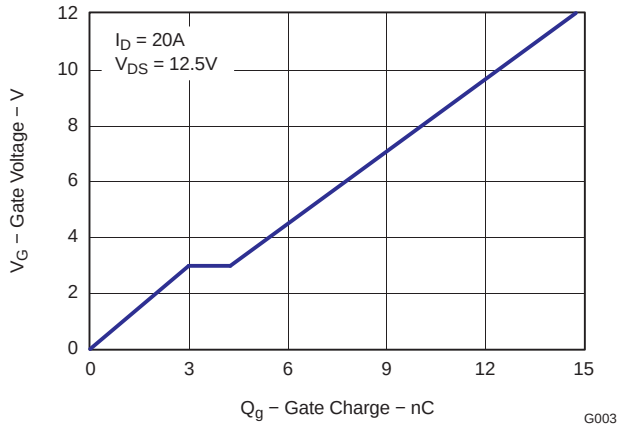



**Figure 4. Gate Charge**

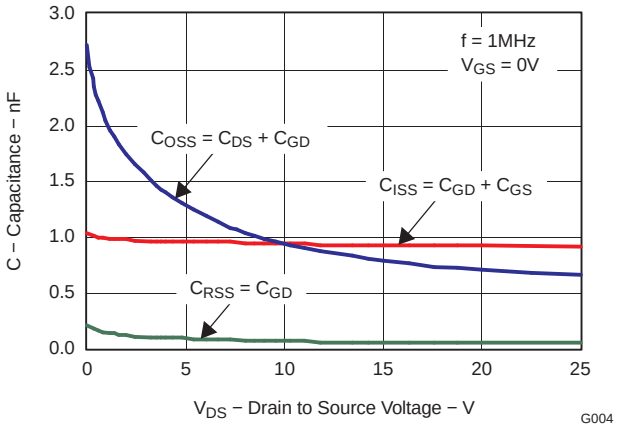



**Figure 5. Capacitance**

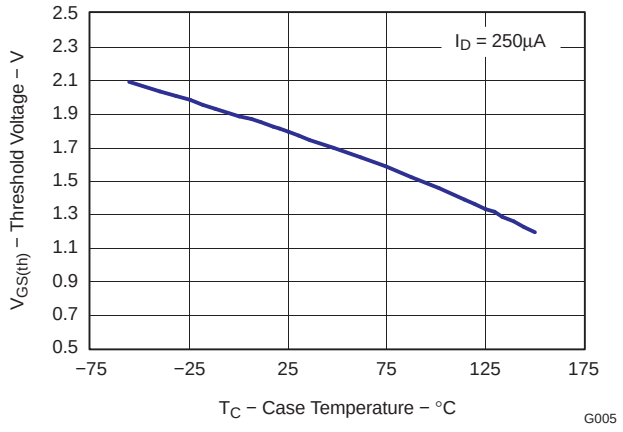



**Figure 6. Threshold Voltage vs. Temperature**

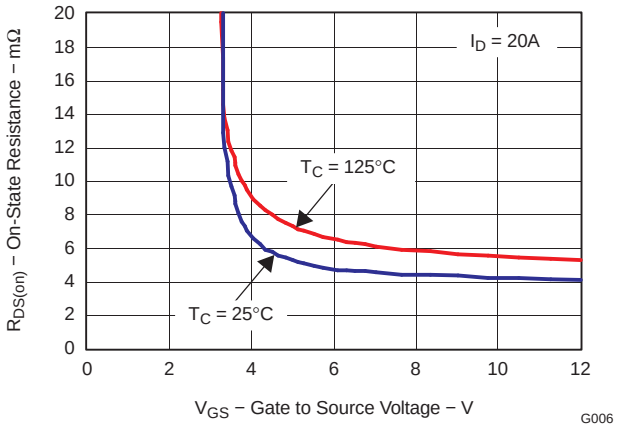



**Figure 7. On-State Resistance vs. Gate to Source Voltage**

## TYPICAL MOSFET CHARACTERISTICS (continued)

$T_A$ = 25°C, unless otherwise specified

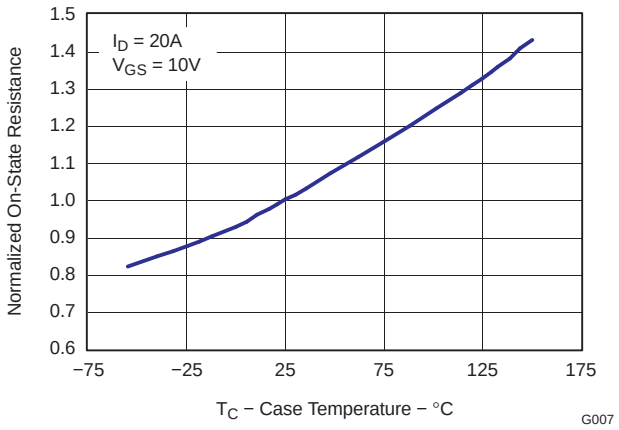



**Figure 8. Normalized On-State Resistance vs. Temperature**

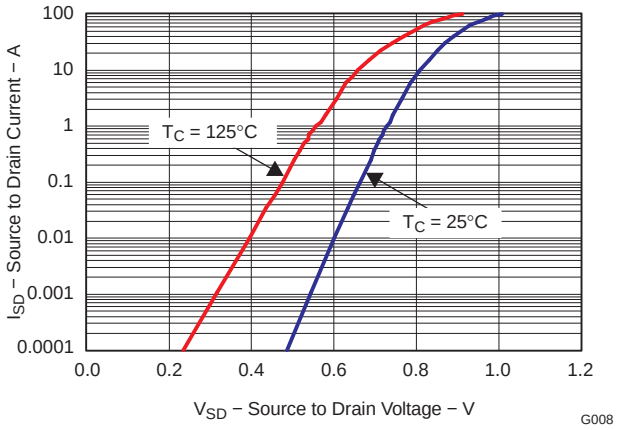



**Figure 9. Typical Diode Forward Voltage**

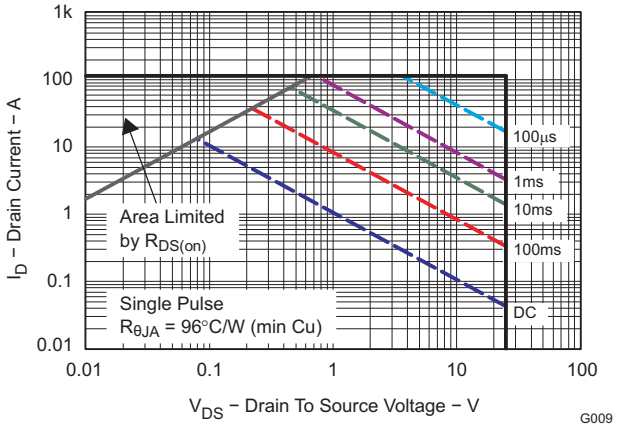



**Figure 10. Maximum Safe Operating Area**

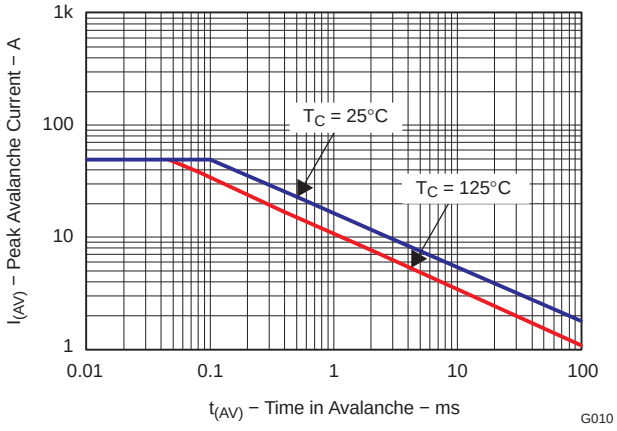



**Figure 11. Single Pulse Unclamped Inductive Switching**

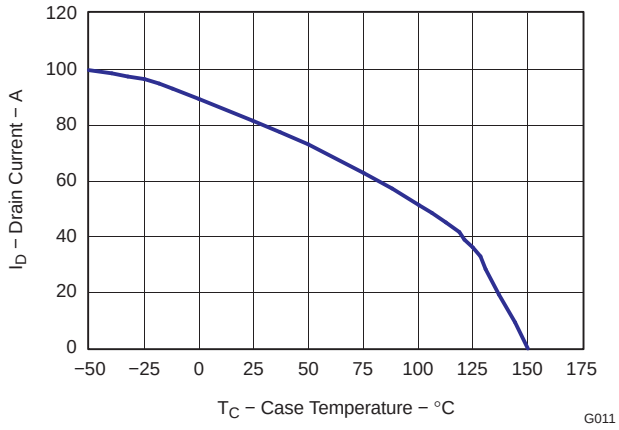
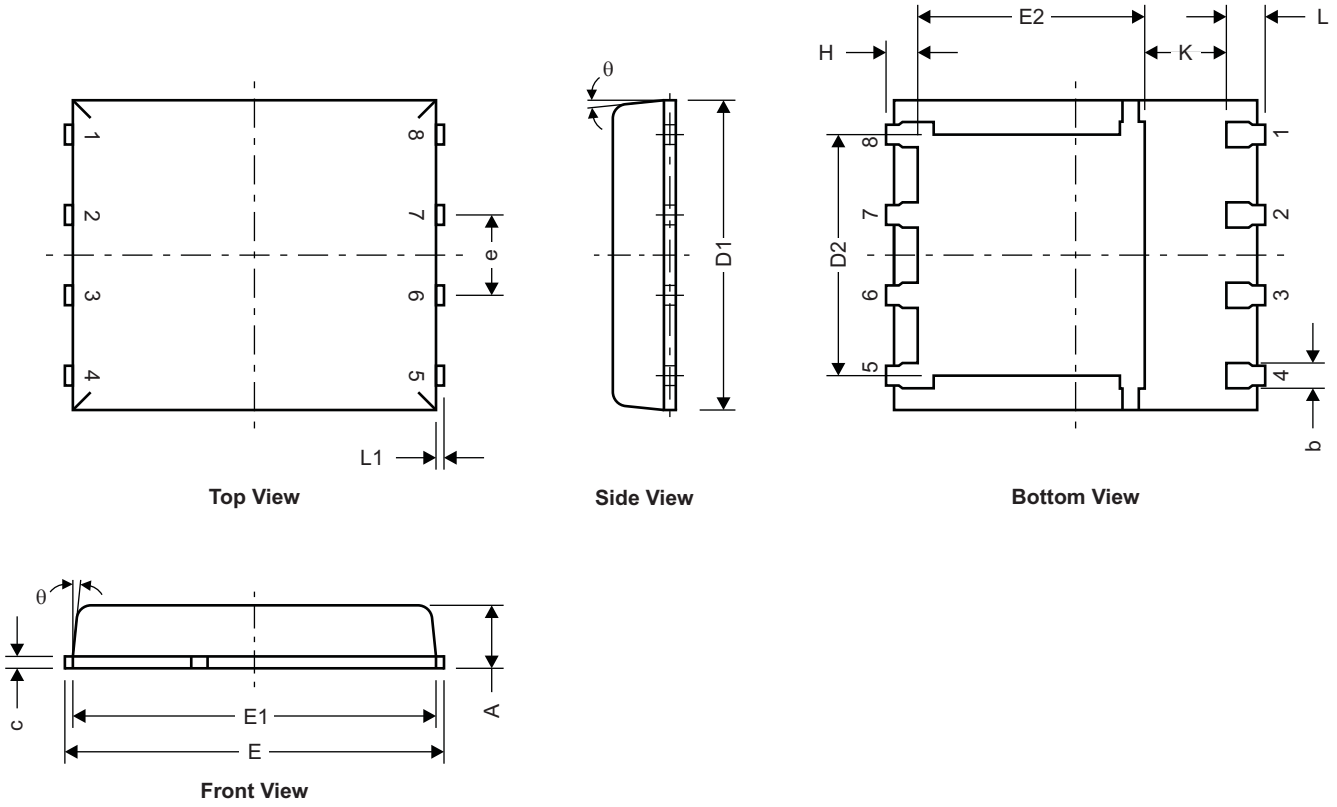



**Figure 12. Maximum Drain Current vs. Temperature**

## MECHANICAL DATA

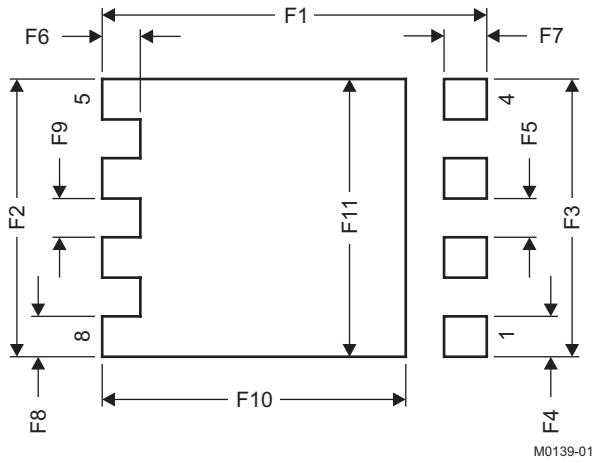
### Q5A Package Dimensions




M0135-01

| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.90 | 1.00 | 1.10 |
| b | 0.33 | 0.41 | 0.51 |
| c | 0.20 | 0.25 | 0.30 |
| D1 | 4.80 | 4.90 | 5.00 |
| D2 | 3.61 | 3.81 | 3.96 |
| E | 5.90 | 6.00 | 6.10 |
| E1 | 5.70 | 5.75 | 5.80 |
| E2 | 3.38 | 3.58 | 3.78 |
| e | | 1.27 BSC | |
| H | 0.41 | 0.51 | 0.61 |
| K | 1.10 | | |
| L | 0.51 | 0.61 | 0.71 |
| L1 | 0.06 | 0.13 | 0.20 |
| θ | 0° | | 12° |

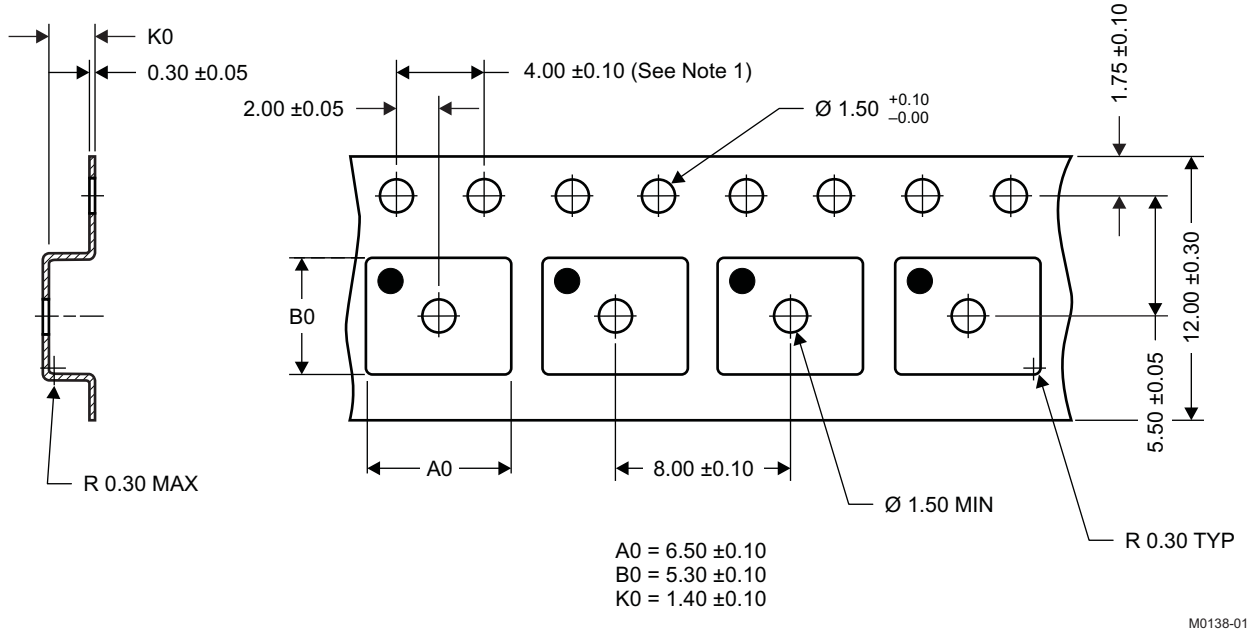
## Recommended PCB Pattern




| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| F1 | 6.205 | 6.305 | 0.244 | 0.248 |
| F2 | 4.46 | 4.56 | 0.176 | 0.18 |
| F3 | 4.46 | 4.56 | 0.176 | 0.18 |
| F4 | 0.65 | 0.7 | 0.026 | 0.028 |
| F5 | 0.62 | 0.67 | 0.024 | 0.026 |
| F6 | 0.63 | 0.68 | 0.025 | 0.027 |
| F7 | 0.7 | 0.8 | 0.028 | 0.031 |
| F8 | 0.65 | 0.7 | 0.026 | 0.028 |
| F9 | 0.62 | 0.67 | 0.024 | 0.026 |
| F10 | 4.9 | 5 | 0.193 | 0.197 |
| F11 | 4.46 | 4.56 | 0.176 | 0.18 |

For recommended circuit layout for PCB designs, see application note SLPA005 – *Reducing Ringing Through PCB Layout Techniques*.

## Q5A Tape and Reel Information




Notes:
1. 10-sprocket hole-pitch cumulative tolerance ±0.22
2. Camber not to exceed 1mm in 100mm, noncumulative over 250mm
3. Material: black static-dissipative polystyrene
4. All dimensions are in mm, unless otherwise specified.
5. A0 and B0 measured on a plane 0.3mm above the bottom of the pocket
6. MSL1 260°C (IR and convection) PbF reflow compatible

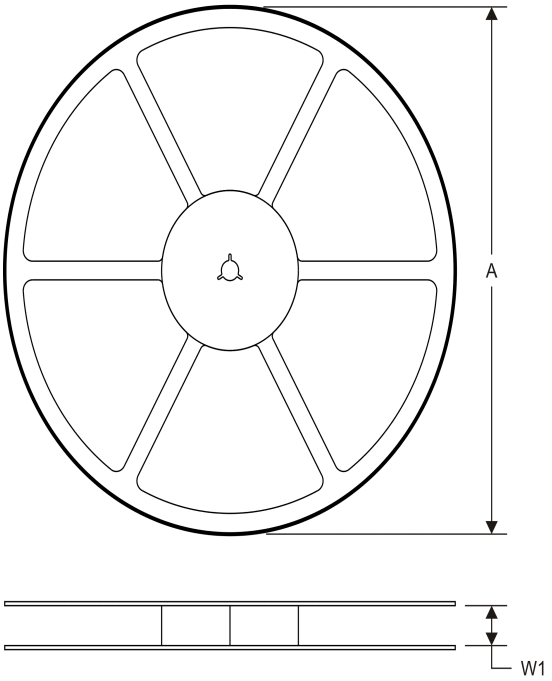
## REVISION HISTORY

| Changes from Original (August 2009) to Revision A | Page |
|---|---|
| • Changed Figure 10 - Maximum Safe Operating Area, Drain Current top scale From: 100ms To: 100µs | 5 |

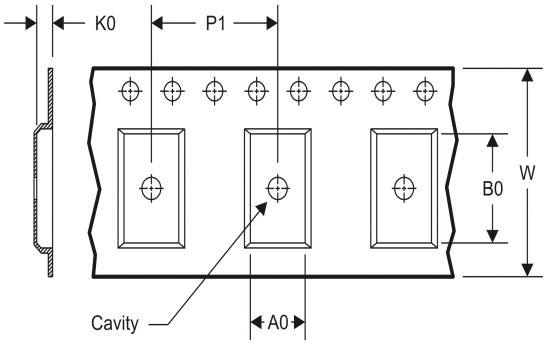
| Changes from Revision A (September 2009) to Revision B | Page |
|---|---|
| • Deleted the Package Marking Information section | 7 |

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**




**TAPE DIMENSIONS**



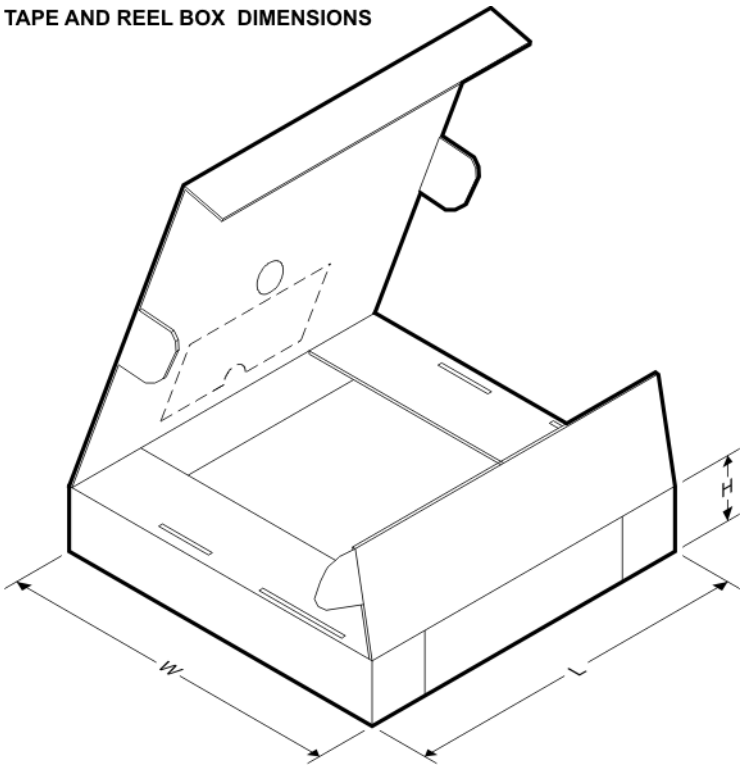

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**TAPE AND REEL INFORMATION**

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CSD16404Q5A | SON | DQJ | 8 | 2500 | 330.0 | 12.4 | 6.3 | 5.3 | 1.2 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CSD16404Q5A | SON | DQJ | 8 | 2500 | 340.0 | 340.0 | 38.0 |

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