

1.5V Drive Pch MOSFET

RT1A050ZP

●Structure

Silicon P-channel MOSFET

●Features

- 1) Low on-resistance.
- 2) High power package.
- 3) Low voltage drive. (1.5V)

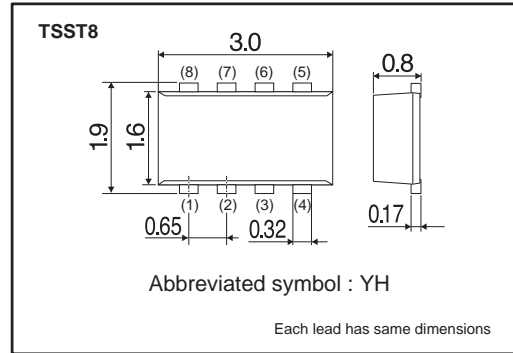
●Applications

Switching

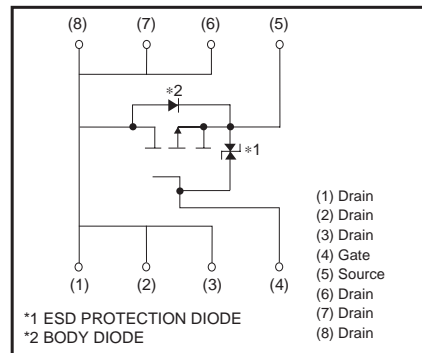
●Packaging specifications

Type	Package	Taping
	Code	TR
	Basic ordering unit(pieces)	3000
RT1A050ZP		○

●Dimensions (Unit : mm)



●Equivalent circuit



●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit	
Drain-source voltage	V _{bss}	-12	V	
Gate-source voltage	V _{gss}	±10	V	
Drain current	Continuous	I _d	±5	A
	Pulsed	I _{dP} *1	±20	A
Source current (Body diode)	Continuous	I _s	-1	A
	Pulsed	I _{sP} *1	-20	A
Total power dissipation	P _D	1.25	W *2	
Channel temperature	T _{ch}	150	°C	
Range of Storage temperature	T _{stg}	-55 to +150	°C	

*1 P_w ≤ 10μs, Duty cycle ≤ 1%
*2 When mounted on a ceramic board

●Thermal resistance

Parameter	Symbol	Limits	Unit
Channel to ambient	R _{th(ch-a)} *	100	°C / W

* When mounted on a ceramic board

●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I _{GSS}	–	–	±10	μA	V _{GS} =±10V, V _{DS} =0V
Drain-source breakdown voltage	V _{(BR) DSS}	–12	–	–	V	I _D = –1mA, V _{GS} =0V
Zero gate voltage drain current	I _{DSS}	–	–	–1	μA	V _{DS} = –12V, V _{GS} =0V
Gate threshold voltage	V _{GS(th)}	–0.3	–	–1.0	V	V _{DS} = –6V, I _D = –1mA
Static drain-source on-state resistance	R _{DS(on)} *	–	19	26	mΩ	I _D = –5A, V _{GS} = –4.5V
		–	26	36	mΩ	I _D = –2.5A, V _{GS} = –2.5V
		–	34	50	mΩ	I _D = –2.5A, V _{GS} = –1.8V
		–	48	96	mΩ	I _D = –1A, V _{GS} = –1.5V
Forward transfer admittance	Y _{fs} *	7	–	–	S	V _{DS} = –6V, I _D = –5A
Input capacitance	C _{iss}	–	2800	–	pF	V _{DS} = –6V
Output capacitance	C _{oss}	–	340	–	pF	V _{GS} =0V
Reverse transfer capacitance	C _{riss}	–	310	–	pF	f=1MHz
Turn-on delay time	t _{d(on)} *	–	12	–	ns	V _{DD} ≐ –6V I _D = –2.5A
Rise time	t _r *	–	95	–	ns	V _{GS} = –4.5V
Turn-off delay time	t _{d(off)} *	–	410	–	ns	R _L ≐ 2.4Ω
Fall time	t _f *	–	220	–	ns	R _G =10Ω
Total gate charge	Q _g *	–	34	–	nC	V _{DD} ≐ –6V R _L ≐ 1.2Ω
Gate-source charge	Q _{gs} *	–	6.0	–	nC	I _D = –5A R _G =10Ω
Gate-drain charge	Q _{gd} *	–	5.0	–	nC	V _{GS} = –4.5V

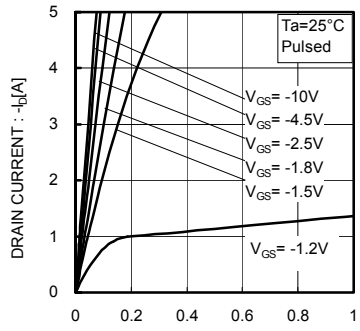
*Pulsed

●Body diode characteristics (Source -drain) (Ta=25°C)

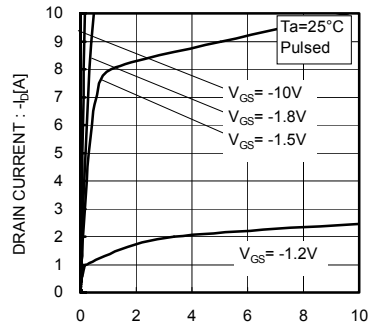
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V _{SD} *	–	–	–1.2	V	I _S = –5A, V _{GS} =0V

*Pulsed

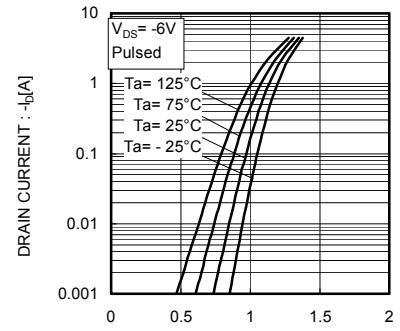
●Electrical characteristic curves



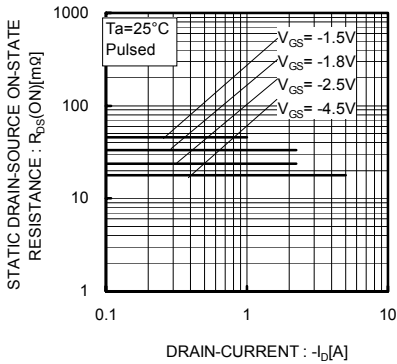
DRAIN-SOURCE VOLTAGE : -V_{DS}[V]
Fig.1 Typical Output Characteristics (I)



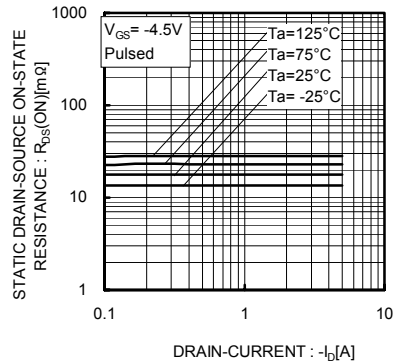
DRAIN-SOURCE VOLTAGE : -V_{DS}[V]
Fig.2 Typical Output Characteristics (II)



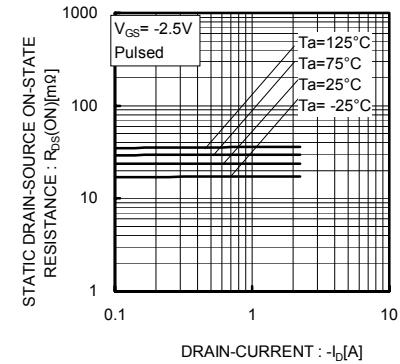
GATE-SOURCE VOLTAGE : -V_{GS}[V]
Fig.3 Typical Transfer Characteristics



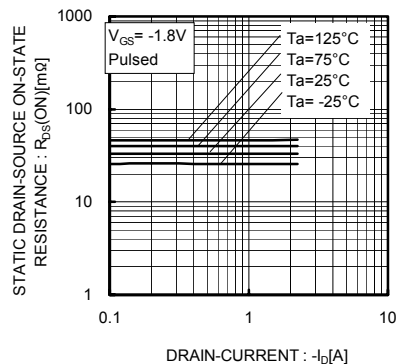
DRAIN-CURRENT : -I_b[A]
Fig.4 Static Drain-Source On-State Resistance vs. Drain Current (I)



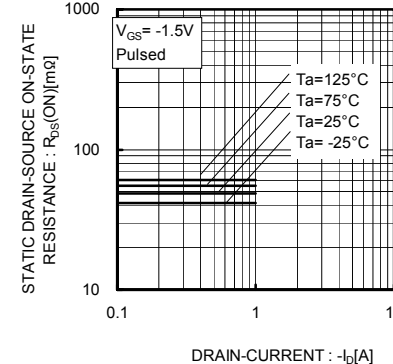
DRAIN-CURRENT : -I_b[A]
Fig.5 Static Drain-Source On-State Resistance vs. Drain Current (II)



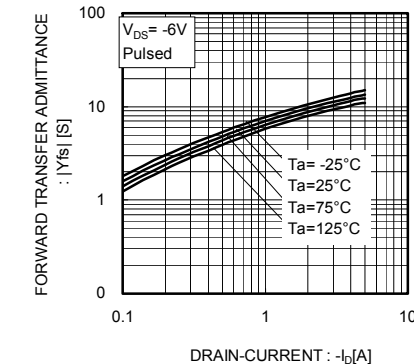
DRAIN-CURRENT : -I_b[A]
Fig.6 Static Drain-Source On-State Resistance vs. Drain Current (III)



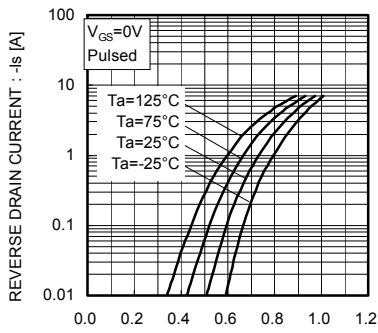
DRAIN-CURRENT : -I_b[A]
Fig.7 Static Drain-Source On-State Resistance vs. Drain Current (IV)



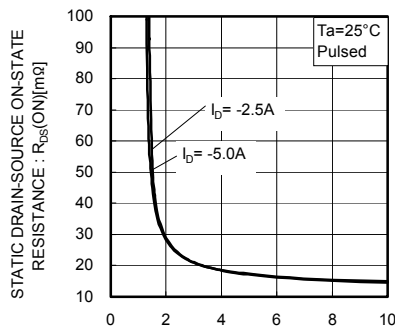
DRAIN-CURRENT : -I_b[A]
Fig.8 Static Drain-Source On-State Resistance vs. Drain Current (IV)



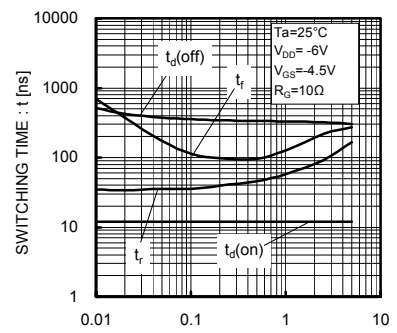
DRAIN-CURRENT : -I_b[A]
Fig.9 Forward Transfer Admittance vs. Drain Current



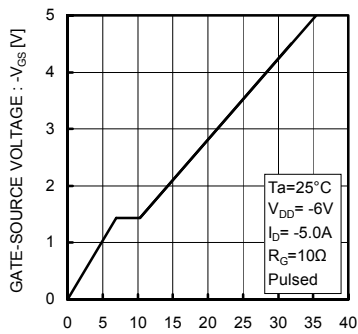
SOURCE-DRAIN VOLTAGE : $-V_{SD}$ [V]
 Fig.10 Reverse Drain Current vs. Source-Drain Voltage



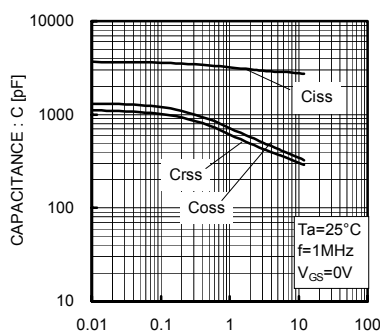
GATE-SOURCE VOLTAGE : $-V_{GS}$ [V]
 Fig.11 Static Drain-Source On-State Resistance vs. Gate Source Voltage



DRAIN-CURRENT : $-I_D$ [A]
 Fig.12 Switching Characteristics



TOTAL GATE CHARGE : Q_g [nC]
 Fig.13 Dynamic Input Characteristics



DRAIN-SOURCE VOLTAGE : $-V_{DS}$ [V]
 Fig.14 Typical Capacitance vs. Drain-Source Voltage

●Measurement circuits

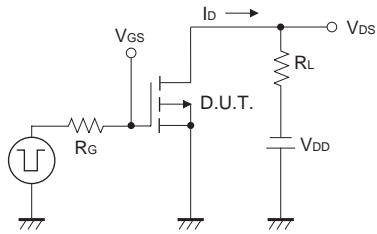


Fig.1-1 Switching Time Measurement Circuit

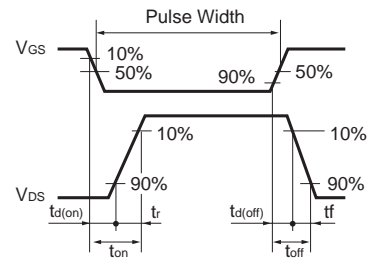


Fig.1-2 Switching Waveforms

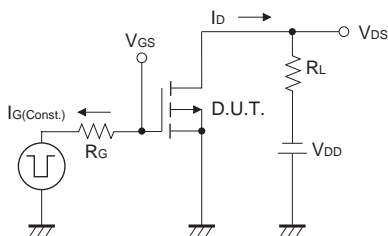


Fig.2-1 Gate Charge Measurement Circuit

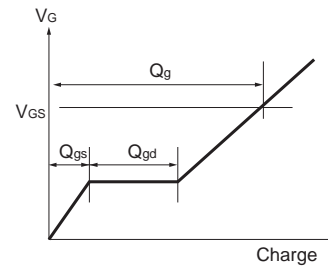


Fig.2-2 Gate Charge Waveform

●Notice

This product might cause chip aging and breakdown under the large electrified environment. Please consider to design ESD protection circuit.

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