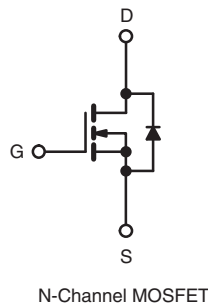


S Series Power MOSFET

PRODUCT SUMMARY		
V_{DS} at T_J max. (V)	650	
$R_{DS(on)}$ max. at 25 °C (Ω)	$V_{GS} = 10$ V	0.190
Q_g max. (nC)	98	
Q_{gs} (nC)	17	
Q_{gd} (nC)	25	
Configuration	Single	



FEATURES

- Generation One
- **Halogen-free According to IEC 61249-2-21 Definition**
- High E_{AR} Capability
- Lower Figure-of-Merit $R_{on} \times Q_g$
- 100 % Avalanche Tested
- Ultra Low R_{on}
- dV/dt Ruggedness
- Ultra Low Gate Charge (Q_g)
- Compliant to RoHS Directive 2002/95/EC



RoHS*
COMPLIANT
HALOGEN
FREE
Available

Note

* Pb containing terminations are not RoHS compliant, exemptions may apply

APPLICATIONS

- PFC Power Supply Stages
- Hard Switching Topologies
- Solar Inverters
- UPS
- Motor Control
- Lighting
- Server Telecom


ORDERING INFORMATION	
Package	TO-247AC
Lead (Pb)-free	SiHG22N60S-E3
Lead (Pb)-free and Halogen-free	SiHG22N60S-GE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)				
PARAMETER	SYMBOL		LIMIT	UNIT
Drain-Source Voltage	V_{DS}		600	V
Gate-Source Voltage	V_{GS}		± 20	
Gate-Source Voltage AC ($f > 1$ Hz)			30	
Continuous Drain Current	V_{GS} at 10 V	$T_C = 25$ °C	22	A
		$T_C = 100$ °C	13	
Pulsed Drain Current ^a			65	
Linear Derating Factor	TO-247		2	W/°C
Single Pulse Avalanche Energy ^b			690	mJ
Repetitive Avalanche Energy ^a			25	
Maximum Power Dissipation	TO-247		250	W
Drain-Source Voltage Slope	$T_J = 125$ °C		37	V/ns
Reverse Diode dV/dt^d			5.3	
Operating Junction and Storage Temperature Range	T_J, T_{stg}		- 55 to + 150	°C
Soldering Recommendations (Peak Temperature) ^c	for 10 s		300	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 50$ V, starting $T_J = 25$ °C, $L = 28.2$ mH, $R_g = 25$ Ω , $I_{AS} = 7$ A.
- 1.6 mm from case.
- $I_{SD} \leq I_D$, $dI/dt = 100$ A/ μ s, starting $T_J = 25$ °C.

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	TO-247	R_{thJA}	-	62	°C/W
Maximum Junction-to-Case (Drain)	TO-247	R_{thJC}	-	0.5	

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$		600	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$		-	0.70	-	V/°C
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$		-	-	1	μA
		$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}, T_J = 150\text{ }^\circ\text{C}$		-	-	100	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 11\text{ A}$	-	0.160	0.190	Ω
Forward Transconductance ^a	g_{fs}	$V_{DS} = 50\text{ V}, I_D = 13\text{ A}$		-	9.4	-	S
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$		-	2810	-	pF
Output Capacitance	C_{oss}			-	1480	-	
Reverse Transfer Capacitance	C_{rss}			-	33	-	
Effective Output Capacitance (Time Related)	$C_{oss\text{ eff.}}(TR)^a$	$V_{GS} = 0\text{ V}$	$V_{DS} = 0\text{ V to } 480\text{ V}$	-	155	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$	$I_D = 22\text{ A}, V_{DS} = 480\text{ V}$	-	75	110	nC
Gate-Source Charge	Q_{gs}			-	17	-	
Gate-Drain Charge	Q_{gd}			-	25	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 380\text{ V}, I_D = 22\text{ A}, R_g = 9.1\text{ }\Omega, V_{GS} = 10\text{ V}$		-	24	50	ns
Rise Time	t_r			-	68	100	
Turn-Off Delay Time	$t_{d(off)}$			-	77	115	
Fall Time	t_f			-	59	90	
Gate Input Resistance	R_g	$f = 1\text{ MHz}, \text{open drain}$		-	0.65	-	Ω
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	22	A
Pulsed Diode Forward Current	I_{SM}			-	-	88	
Diode Forward Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = 22\text{ A}, V_{GS} = 0\text{ V}$		-	-	1.2	V
Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = I_S, di/dt = 100\text{ A}/\mu\text{s}, V_R = 25\text{ V}$		-	462	690	ns
Reverse Recovery Charge	Q_{rr}			-	8.3	16	μC
Reverse Recovery Current	I_{RRM}			-	30	60	A

Note

a. $C_{oss\text{ eff.}}(TR)$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS} .

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

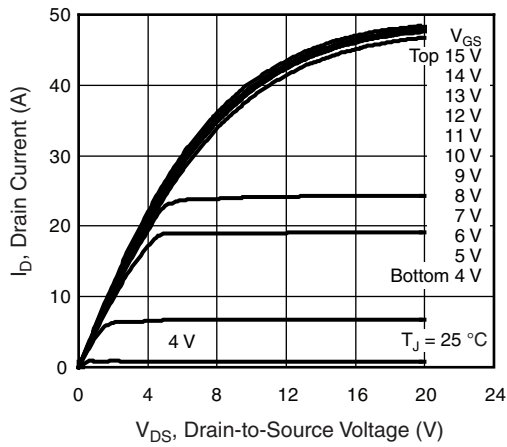


Fig. 1 - Typical Output Characteristics, $T_J = 25\text{ }^\circ\text{C}$

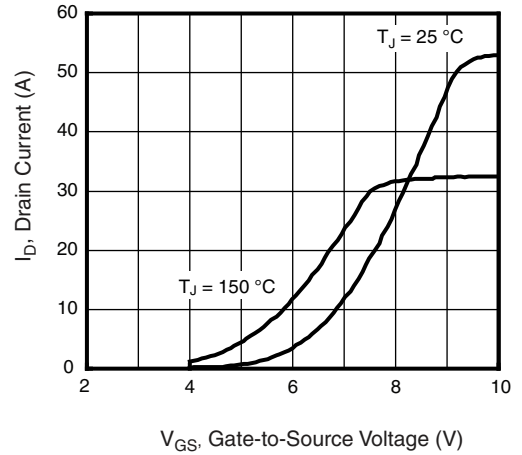


Fig. 3 - Typical Transfer Characteristics

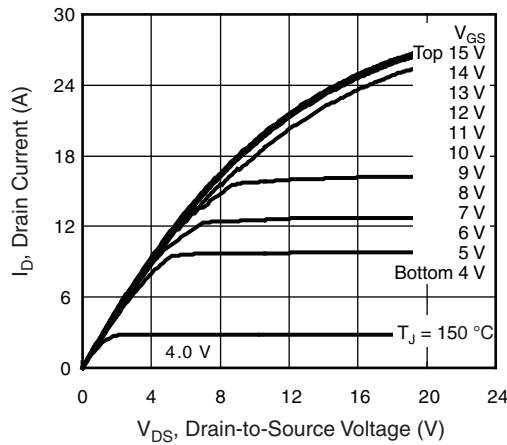


Fig. 2 - Typical Output Characteristics, $T_J = 150\text{ }^\circ\text{C}$

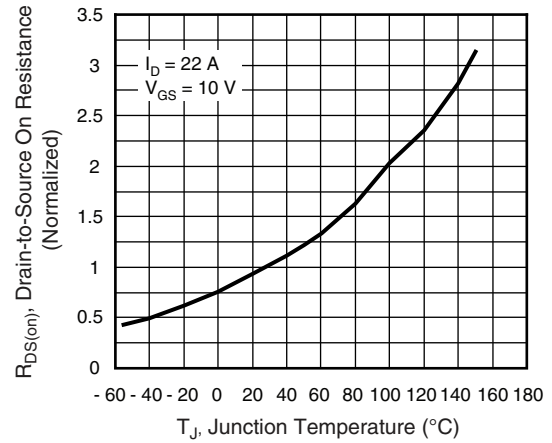


Fig. 4 - Normalized On-Resistance vs. Temperature

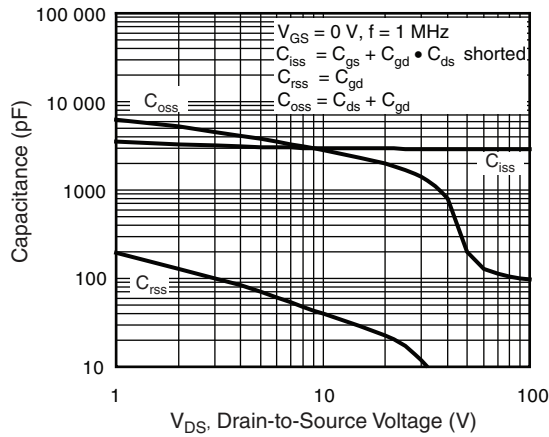


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

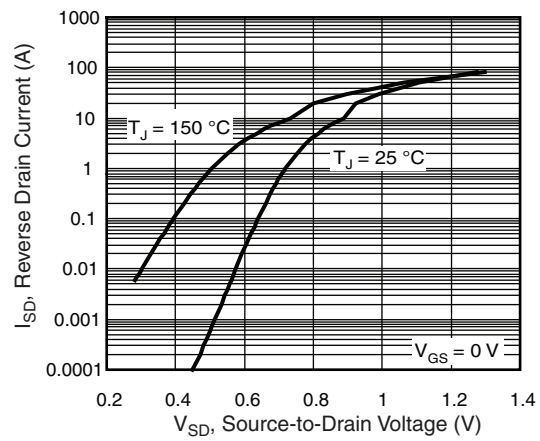


Fig. 7 - Typical Source-Drain Diode Forward Voltage

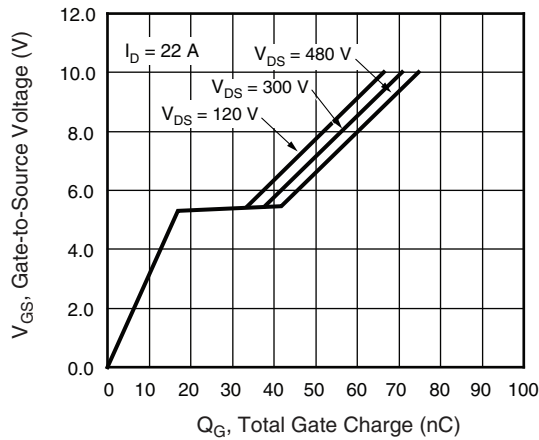


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

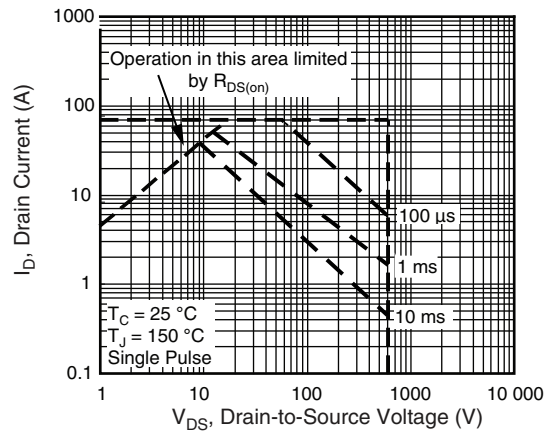


Fig. 8 - Maximum Safe Operating Area

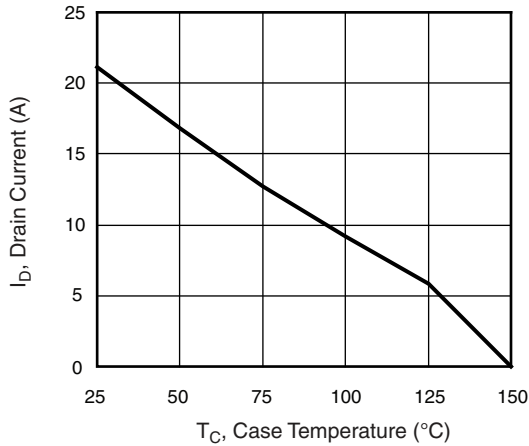


Fig. 9 - Maximum Drain Current vs. Case Temperature

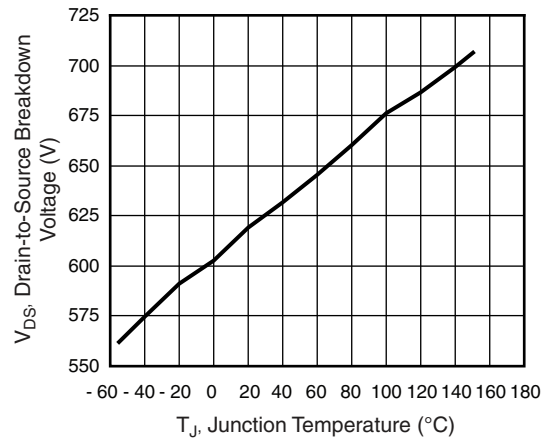


Fig. 10 - Drain-to-Source Breakdown Voltage

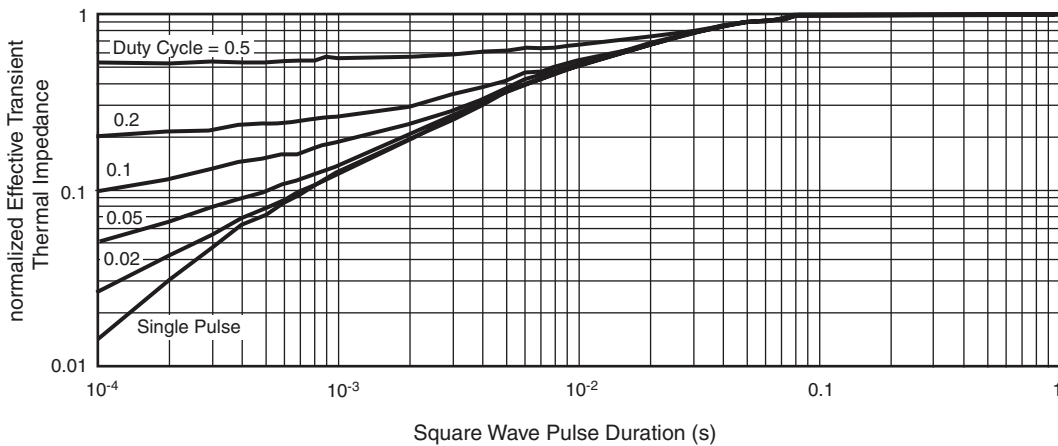


Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case

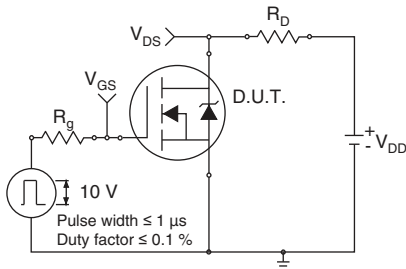


Fig. 11a - Switching Time Test Circuit

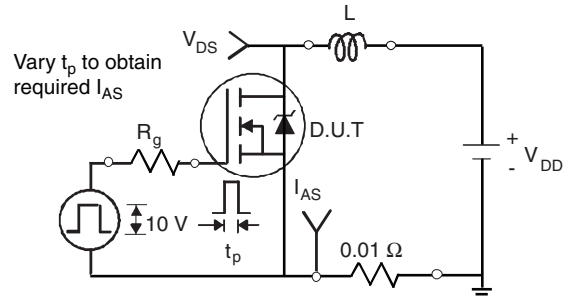


Fig. 12a - Unclamped Inductive Test Circuit

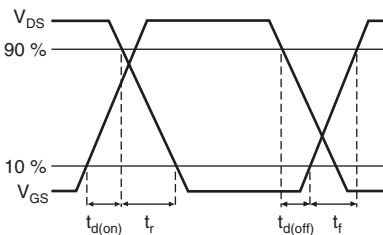


Fig. 11b - Switching Time Waveforms

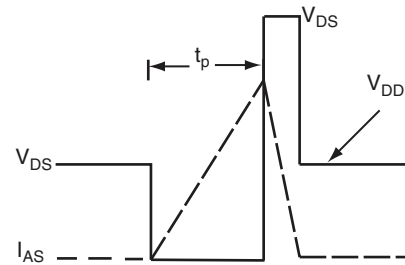


Fig. 12b - Unclamped Inductive Waveforms

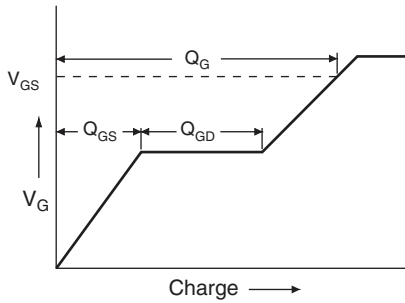


Fig. 13a - Basic Gate Charge Waveform

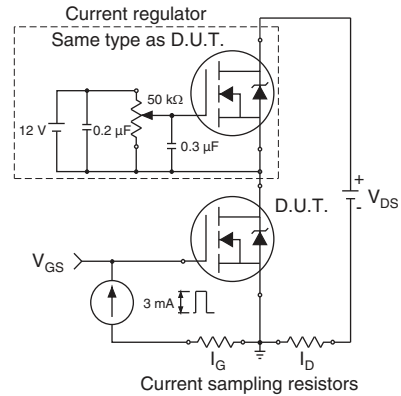
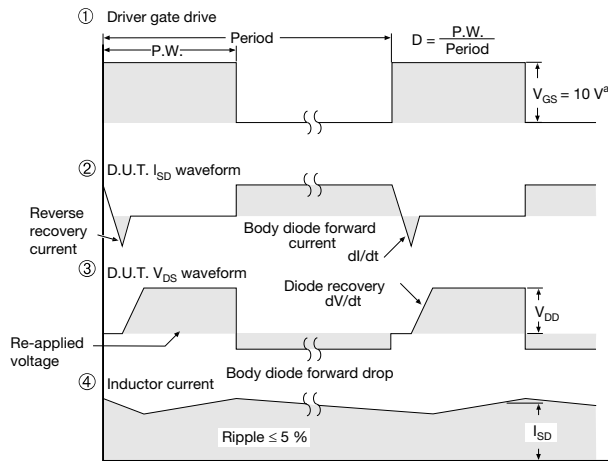
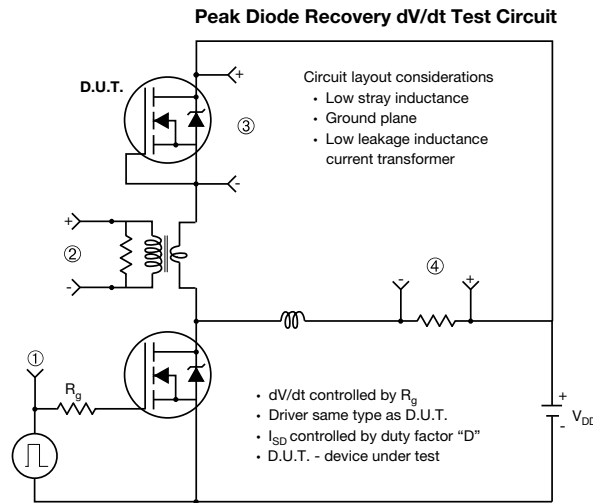


Fig. 13b - Gate Charge Test Circuit

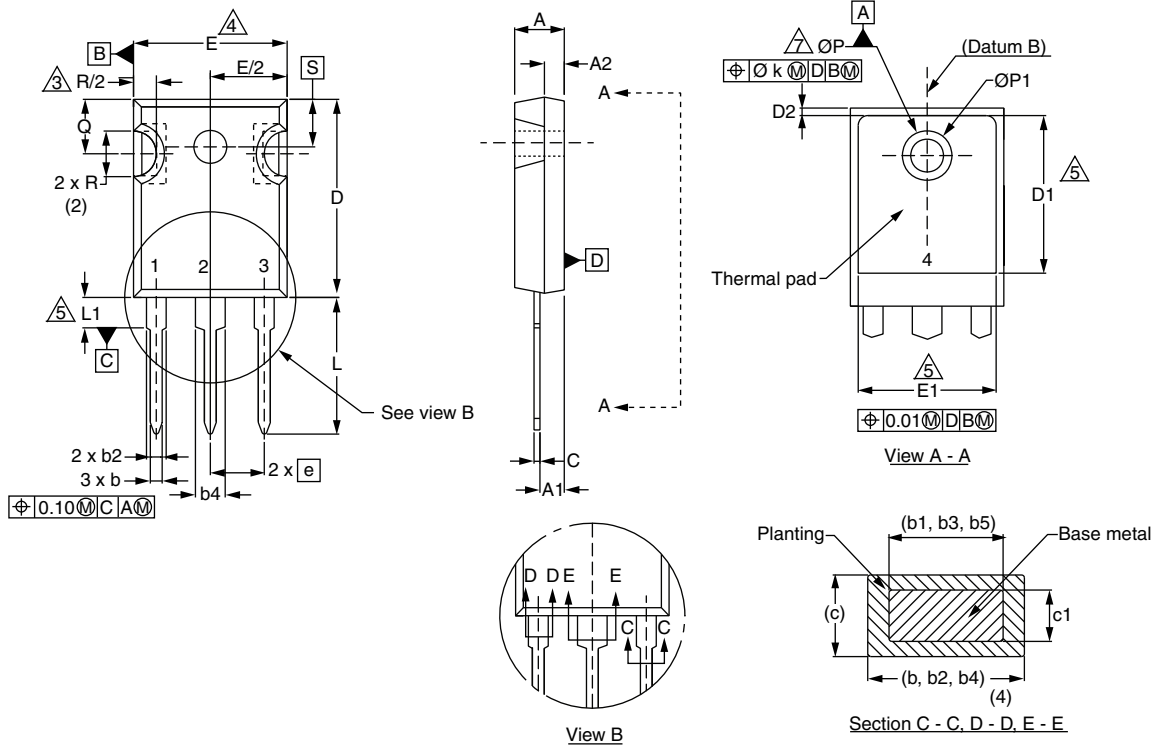


Note
a. $V_{GS} = 5V$ for logic level devices

Fig. 14 - For N-Channel

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TO-247AC (High Voltage)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.58	5.31	0.180	0.209
A1	2.21	2.59	0.087	0.102
A2	1.17	2.49	0.046	0.098
b	0.99	1.40	0.039	0.055
b1	0.99	1.35	0.039	0.053
b2	1.53	2.39	0.060	0.094
b3	1.65	2.37	0.065	0.093
b4	2.42	3.43	0.095	0.135
b5	2.59	3.38	0.102	0.133
c	0.38	0.86	0.015	0.034
c1	0.38	0.76	0.015	0.030
D	19.71	20.82	0.776	0.820
D1	13.08	-	0.515	-

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D2	0.51	1.30	0.020	0.051
E	15.29	15.87	0.602	0.625
E1	13.72	-	0.540	-
e	5.46 BSC		0.215 BSC	
ϕk	0.254		0.010	
L	14.20	16.25	0.559	0.640
L1	3.71	4.29	0.146	0.169
N	7.62 BSC		0.300 BSC	
ϕP	3.51	3.66	0.138	0.144
$\phi P1$	-	7.39	-	0.291
Q	5.31	5.69	0.209	0.224
R	4.52	5.49	0.178	0.216
S	5.51 BSC		0.217 BSC	

ECN: X12-0167-Rev. B, 24-Sep-12
DWG: 5971

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Contour of slot optional.
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body.
4. Thermal pad contour optional with dimensions D1 and E1.
5. Lead finish uncontrolled in L1.
6. ϕP to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154").
7. Outline conforms to JEDEC outline TO-247 with exception of dimension c.
8. Xian and Mingxin actually photo.





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