

Vishay Siliconix

N-Channel 75 V (D-S) MOSFET

PRODUCT SUMMARY						
V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A)	Q _g (Typ.)			
75	0.007 at V _{GS} = 10 V	110 ^d	69			

FEATURES

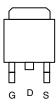
APPLICATIONS

- TrenchFET® Power MOSFETS
- 100 % $\rm R_{\rm g}$ and UIS Tested

Material categorization: For definitions of compliance please see www.vishav.com/doc?99912

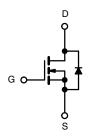






Top View

· Synchronous Rectification



N-Channel MOSFET

Ordering Information: SUM110N08-07P-E3 (Lead (Pb)-free)

Parameter	Symbol	Limit	Unit		
Drain-Source Voltage	V _{DS}	75	V		
Gate-Source Voltage	V _{GS}	± 20	7 v		
Continuous Drain Current (T _{.I} = 150 °C)	T _C = 25 °C	1-	110 ^d		
Continuous Diain Current (1j = 150 °C)	T _C = 70 °C	-	103	А	
Pulsed Drain Current		I _{DM}	180		
Avalanche Current		I _{AS}	50	1	
Single Avalanche Energy ^a	L = 0.1 mH	E _{AS}	125	mJ	
Mariana Barra Birahadi ad	T _C = 25 °C	В	208.3 ^b	w	
Maximum Power Dissipation ^a	T _A = 25 °C ^c	P _D	3.75		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Limit	Unit		
Junction-to-Ambient (PCB Mount) ^c	R _{thJA}	40	°C/W		
Junction-to-Case (Drain)	R _{thJC}	0.6	C/VV		

Notes:

- a. Duty cycle \leq 1 %.
- b. See SOA curve for voltage derating.
- c. When mounted on 1" square PCB (FR-4 material).
- d. Package limited.

SUM110N08-07P

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SPECIFICATIONS (T _J = 25	°C, unless o	otherwise noted)					
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static	•						
Drain-Source Breakdown Voltage	V_{DS}	$V_{DS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$	75			_ v	
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	2.5		4.5		
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 250	nA	
		V _{DS} = 75 V, V _{GS} = 0 V			1		
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 75 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 125 ^{\circ}\text{C}$			50	μΑ	
		V _{DS} = 75 V, V _{GS} = 0 V, T _J = 150 °C			250		
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 10 \text{ V}, V_{GS} = 10 \text{ V}$	70			Α	
D : 0	В	V _{GS} = 10 V, I _D = 20 A		0.0057	0.0070	Ω	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 20 A, T _J = 125 °C		0.0092	0.0112		
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 20 A		43		S	
Dynamic ^b	•						
Input Capacitance	C _{iss}			4250		pF	
Output Capacitance	C _{oss}	$V_{GS} = 0 \text{ V}, V_{DS} = 30 \text{ V}, f = 1 \text{ MHz}$		580			
Reverse Transfer Capacitance	C _{rss}			230			
Total Gate Charge ^c	Q_g			69	105		
Gate-Source Charge ^c	Q _{gs}	$V_{DS} = 30 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 50 \text{ A}$		23		nC	
Gate-Drain Charge ^c	Q _{gd}			21			
Gate Resistance	R _g	f = 1 MHz		1.2	2.4	Ω	
Turn-On Delay Time ^c	t _{d(on)}			17	30		
Rise Time ^c	t _r	$V_{DD} = 30 \text{ V}, R_{L} = 0.6 \Omega$		5	10	ns	
Turn-Off Delay Time ^c	t _{d(off)}	$I_D \cong 50 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		22	40		
Fall Time ^c	t _f			6	15		
Source-Drain Diode Ratings and Ch	aracteristics 7	C _C = 25 °C ^b	1				
Continuous Current	Is		1		110		
Pulsed Current	I _{SM}				180	Α	
Forward Voltage ^a	V_{SD}	$I_F = 20 \text{ A}, V_{GS} = 0 \text{ V}$		0.83	1.5	V	
Reverse Recovery Time	t _{rr}			65	100	ns	
Peak Reverse Recovery Current	I _{RM(REC)}	I _F = 75 A, dI/dt = 100 A/μs		2.5	5	Α	
Reverse Recovery Charge	Q _{rr}			85	150	nC	

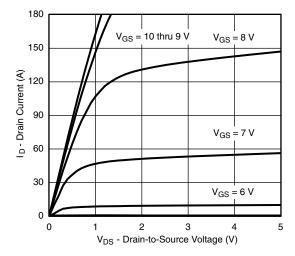
Notes:

- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

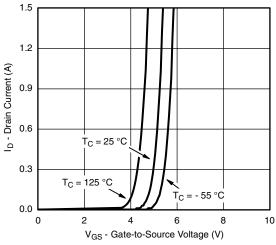
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



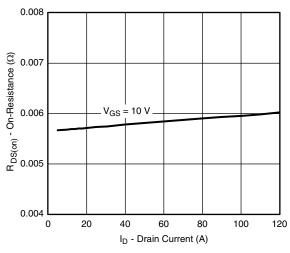
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



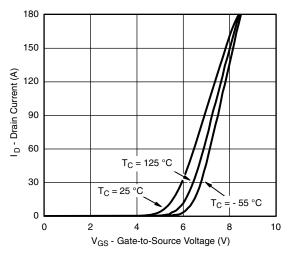
Output Characteristics



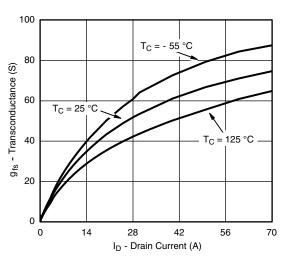
Transfer Characteristics



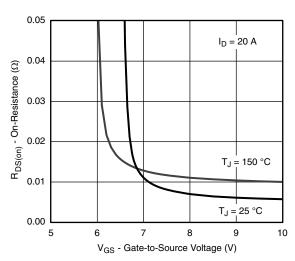
On-Resistance vs. Drain Current



Transfer Characteristics



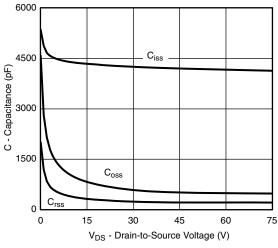
Transconductance



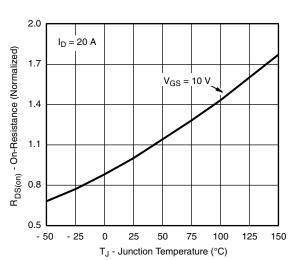
On-Resistance vs. Gate-to-Source Voltage

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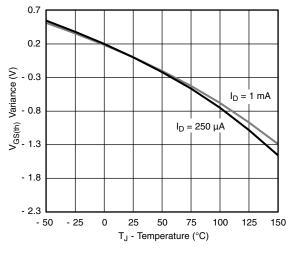
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



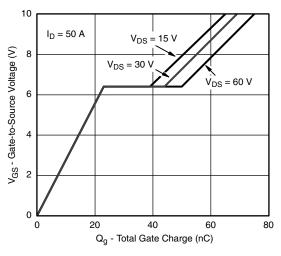




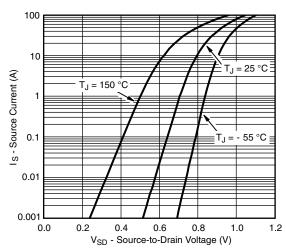
On-Resistance vs. Junction Temperature



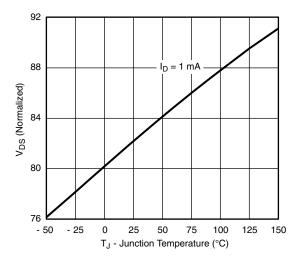
Threshold Voltage



Gate Charge



Source-Drain Diode Forward Voltage

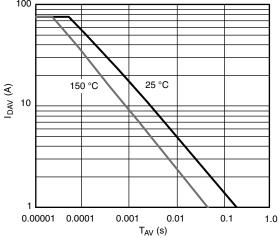


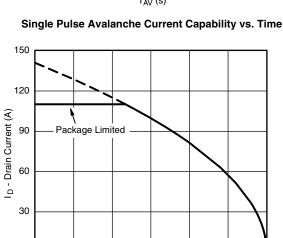
Drain Source Breakdown vs. Junction Temperature



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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)





75

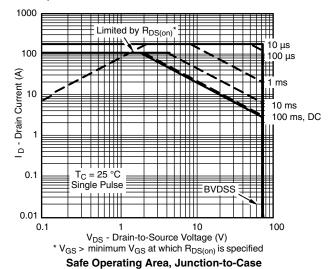
T_C - Case Temperature (°C)

Current Derating*, Junction-to-Case

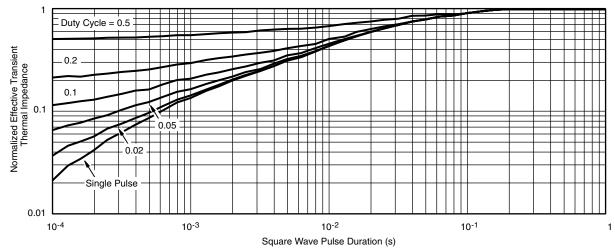
100

125

150



 $^{^{\}star}$ The power dissipation P_{D} is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see /www.vishay.com/ppg?68637.

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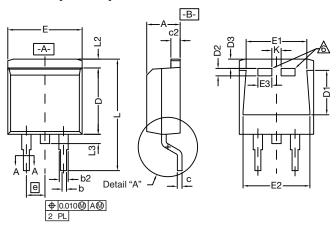
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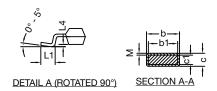
25





TO-263 (D²PAK): 3-LEAD





		INC	HES	MILLIN	METERS	
	DIM.	MIN.	MAX.	MIN. MAX		
	Α	0.160	0.190	4.064	4.826	
	b	0.020	0.039	0.508	0.990	
	b1	0.020	0.035	0.508	0.889	
	b2	0.045	0.055	1.143	1.397	
c*	Thin lead	0.013	0.018	0.330	0.457	
C	Thick lead	0.023	0.028	0.584	0.711	
c1	Thin lead	0.013	0.017	0.330	0.431	
CI	Thick lead	0.023	0.027	0.584	0.685	
	c2	0.045	0.055	1.143	1.397	
	D	0.340	0.380	8.636	9.652	
D1		0.220	0.240	5.588	6.096	
D2		0.038	0.042	0.965	1.067	
	D3	0.045	0.055	1.143	1.397	
	Е	0.380	0.410	9.652	10.414	
	E1	0.245	-	6.223	-	
	E2	0.355	0.375	9.017 9.52		
	E3	0.072	0.078	1.829	1.981	
	е	0.100	BSC	2.54	BSC	
	K	0.045	0.055	1.143	1.397	
L		0.575	0.625	14.605	15.875	
	L1	0.090	0.110	2.286	2.794	
L2		0.040	0.055	1.016	1.397	
L3		0.050	0.070	1.270	1.778	
	L4	0.010	BSC	0.254	BSC	
	М	-	0.002	-	0.050	
	N: T10-0738-Re G: 5843	ev. J, 03-Ja	n-11			

Notes

- 1. Plane B includes maximum features of heat sink tab and plastic.
- 2. No more than 25 % of L1 can fall above seating plane by max.
- 3. Pin-to-pin coplanarity max. 4 mils.
- 4. *: Thin lead is for SUB, SYB. Thick lead is for SUM, SYM, SQM.





RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads Dimensions in Inches/(mm)

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Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

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