



P-Channel 30 V (D-S) MOSFET

PRODUCT SUMMARY						
V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A)	Q _g (Typ.)			
	0.167 at V _{GS} = - 10 V	0.96				
- 30	0.188 at V _{GS} = - 4.5 V	0.90	3.25			
	0.244 at V _{GS} = - 2.5 V	0.79				

FEATURES

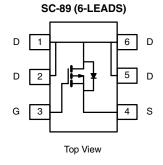
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFET
- 100 % R_g Tested
- Compliant to RoHS Directive 2002/95/EC

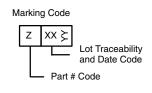


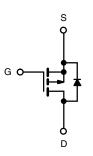
ROHS COMPLIANT HALOGEN FREE

APPLICATIONS

• Load Switch for Portable Devices







Ordering Information: Si1071X-T1-GE3 (Lead (Pb)-free and Halogen-free)

P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)						
Parameter		Symbol	Limit	Unit		
Drain-Source Voltage		V _{DS}	- 30	V		
Gate-Source Voltage		V _{GS}	± 12	v		
Continuous Drain Current (T _J = 150 °C)	T _A = 25 °C	1-	- 0.96 ^{b, c}			
	T _A = 70 °C	I _D	- 0.76 ^{b, c}			
Pulsed Drain Current		I _{DM}	- 8	A		
Continuous Source-Drain Diode Current	T _A = 25 °C	I _S	- 0.2 ^{b, c}			
M ·	T _A = 25 °C	D.	0.236 ^{b, c}	w		
Maximum Power Dissipation ^a	T _A = 70 °C	- P _D —	0.151 ^{b, c}	VV		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150	°C		

THERMAL RESISTANCE RATINGS						
Parameter	Symbol	Typical	Maximum	Unit		
Manipulation to Applicate h	t ≤ 5 s	B	440	530	°C/W	
Maximum Junction-to-Ambient ^{a, b}	Steady State	R_{thJA}	540	650	C/VV	

Notes:

- a. Maximum under steady state conditions is 650 °C/W.
- b. Surface mounted on 1" x 1" FR4 board.
- c. t = 5 s.

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static				'			
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V, I}_{D} = -250 \mu\text{A}$	- 30			V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	J 050 A		- 32.07		mV/°C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	- I _D = - 250 μA		3.02		mv/°C	
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = -250 \mu A$	- 0.7		- 1.45	V	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$			± 100	nA	
Zava Cata Valtaga Dvain Current	1	V _{DS} = - 30 V, V _{GS} = 0 V			- 1	nA	
Zero Gate Voltage Drain Current	$V_{DS} = -30 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 85 ^{\circ}$	V _{DS} = - 30 V, V _{GS} = 0 V, T _J = 85 °C			- 10	μΑ	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} = \ge 5 \text{ V}, V_{GS} = -10 \text{ V}$	- 8			Α	
		V _{GS} = - 10 V, I _D = - 0.96 A		0.139	0.167		
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 4.5 V, I _D = - 0.9 A		0.147	0.177		
		V _{GS} = - 2.5 V, I _D = - 0.79 A		0.195	0.244		
Forward Transconductance	9 _{fs}	V _{DS} = - 15 V, I _D = - 0.96 A		4.25		S	
Dynamic ^b				'			
Input Capacitance	C _{iss}			315			
Output Capacitance	C _{oss}	$V_{DS} = -15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		60		pF	
Reverse Transfer Capacitance	C _{rss}			45			
Total Cata Charge	0	$V_{DS} = -15 \text{ V}, V_{GS} = -4.5 \text{ V}, I_{D} = -0.96 \text{ A}$		4.43	6.64	nC	
Total Gate Charge	Q_g			8.87	13.3		
Gate-Source Charge	Q_{gs}	$V_{DS} = -15 \text{ V}, V_{GS} = -10 \text{ V}, I_{D} = -0.96 \text{ A}$		0.83			
Gate-Drain Charge	Q_{gd}			1.57			
Gate Resistance	R_g	f = 1 MHz		9.8	14.7	Ω	
Turn-On Delay Time	t _{d(on)}			3.8	5.7		
Rise Time	t _r	$V_{DD} = -15 \text{ V}, R_{L} = 19.74 \Omega$		12	18		
Turn-Off DelayTime	t _{d(off)}	$I_D \cong -0.76 \text{ A}, V_{GEN} = -10 \text{ V}, R_g = 1 \text{ G}$		18	27	1	
Fall Time	t _f			7	10.5		
Turn-On Delay Time	t _{d(on)}			13	20	ns	
Rise Time	t _r	$V_{DD} = -15 \text{ V}, R_{L} = 20.27 \Omega$		25	38		
Turn-Off DelayTime	t _{d(off)}	$I_D \cong$ - 0.74 A, V_{GEN} = - 4.5 V, R_g = 1 Ω		36	54		
Fall Time	t _f			14	21		
Drain-Source Body Diode Character	istics						
Pulse Diode Forward Current ^a	I _{SM}				8	Α	
Body Diode Voltage	V_{SD}	I _S = - 0.63 A		0.8	1.2	V	
Body Diode Reverse Recovery Time	t _{rr}			12.7	19.05	nC	
Body Diode Reverse Recovery	rse Recovery Q			5.7	8.6		
Reverse Recovery Fall Time	t _a	$I_F = -0.7 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}$		8.9		ns	

Notes:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

a. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2 %.

b. Guaranteed by design, not subject to production testing.





TYPICAL CHARACTERISTICS ($T_A = 25$ °C, unless otherwise noted)

6

Q_q - Total Gate Charge (nC)

Gate Charge

10

- 50

- 25

0

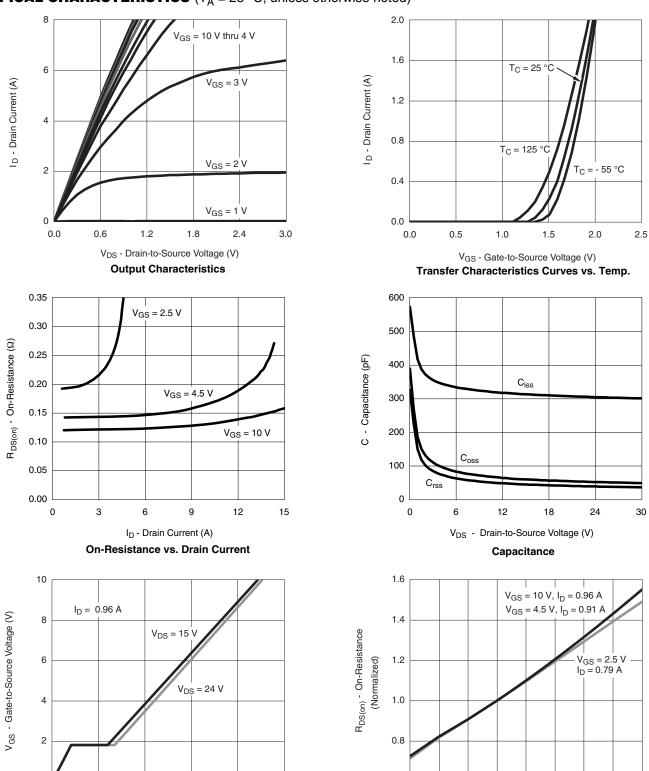
25

50

 T_J - Junction Temperature (°C)

On-Resistance vs. Junction Temperature

75



0

125

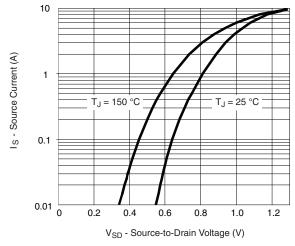
100

150

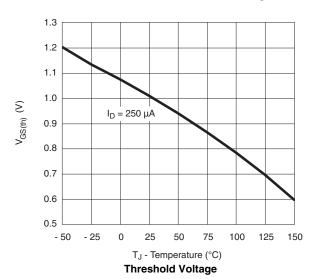
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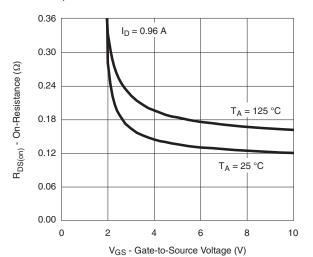
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TYPICAL CHARACTERISTICS ($T_A = 25$ °C, unless otherwise noted)

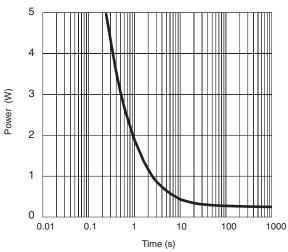


Source-Drain Diode Forward Voltage

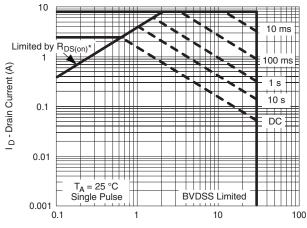




On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power



V_{DS} - Drain-to-Source Voltage (V)

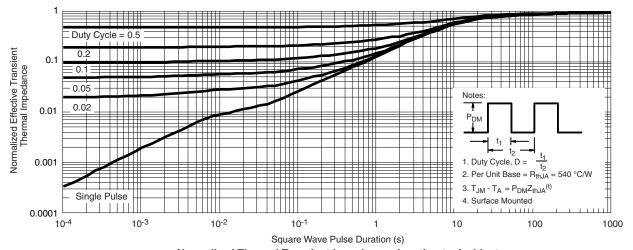
 * V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient





TYPICAL CHARACTERISTICS ($T_A = 25$ °C, unless otherwise noted)

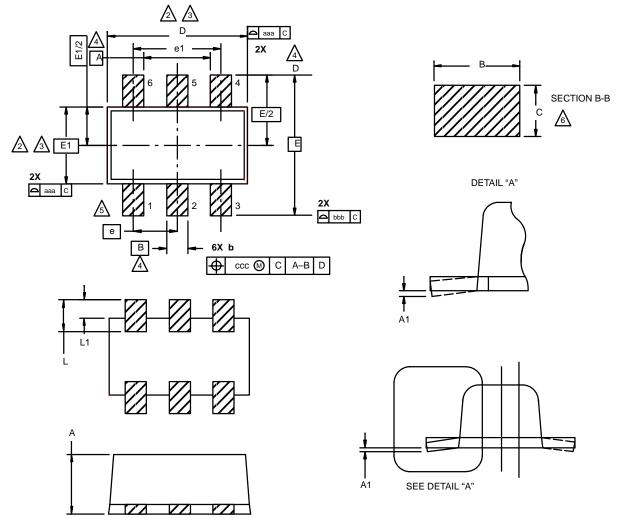


Normalized Thermal Transient Impedance, Junction-to-Ambient

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?74321.



SC89: 6- LEADS (SOT-563F)



NOTES:

1. Dimensions in millimeters.



Dimension D does not include mold flash, protrusions or gate burrs. Mold flush, protrusions or gate burrs shall not exceed 0.15 mm per dimension E1 does not include interlead flash or protrusion, interlead flash or protrusion shall not exceed 0.15 mm per side.



Dimensions D and E1 are determined at the outmost extremes of the plastic body exclusive of mold flash, the bar burrs, gate burrs and interlead flash, but including any mismatch between the top and the bottom of the plastic body.



Datums A, B and D to be determined 0.10 mm from the lead tip.



Terminal numbers are shown for reference only.



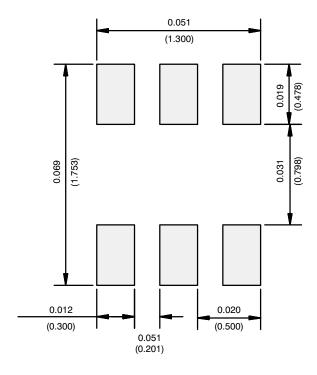
These dimensions apply to the flat section of the lead between 0.08 mm and 0.15 mm from the lead tip.

	MILLIM	ETERS		ote Symbol	Tolerance Of Form A		
Dim	Min	Max	Note		Position		
Α	0.56	0.60		aaa	0.10		
A1	0.00	0.10		bbb	0.10		
b	0.15	0.30		ccc	0.10		
С	0.10	0.18					
D	1.50	1.70	2, 3				
E	1.55	1.70					
E1	1.20 BSC		2, 3				
е	0.50 BSC						
e1	1.00 BSC						
L	0.35 BSC						
L1	0.20 BSC						

DWG: 5880



RECOMMENDED MINIMUM PADS FOR SC-89: 6-Lead



Recommended Minimum Pads Dimensions in Inches/(mm)

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APPLICATION NOTE



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