



# N-Channel 30 V (D-S) MOSFET

PRODUCT SUMMARY					
V <sub>DS</sub> (V)	$R_{DS(on)}(\Omega)$	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ.)		
30	0.099 at V <sub>GS</sub> = 4.5 V	1.2 <sup>a</sup>	3.5		
30	0.140 at V <sub>GS</sub> = 2.5 V	1.0	3.5		

## **FEATURES**

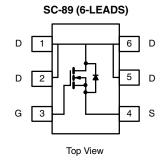
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- 100 % R<sub>q</sub> and UIS Tested
- Compliant to RoHS Directive 2002/95/EC

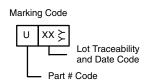


ROHS COMPLIANT HALOGEN FREE

### **APPLICATIONS**

· Load Switch for Portable Devices





Ordering Information: Si1070X-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C, unless otherwise noted)					
Parameter	Symbol	Limit	Unit		
Drain-Source Voltage	$V_{DS}$	30	V		
Gate-Source Voltage	$V_{GS}$	± 12	V		
Continuous Drain Current (T <sub>.I</sub> = 150 °C) <sup>a</sup>	T <sub>A</sub> = 25 °C	I_	1.2 <sup>b, c</sup>	Α	
	T <sub>A</sub> = 70 °C	l <sub>D</sub>	1 <sup>b, c</sup>		
Pulsed Drain Current		I <sub>DM</sub>	6	1	
Avalanche Current L = 0.1 mH		I <sub>AS</sub>	9		
Repetitive Avalanche Energy	L = 0.1 11111	E <sub>AS</sub>	4.01	mJ	
Continuous Source-Drain Diode Current	T <sub>A</sub> = 25 °C	I <sub>S</sub>	0.2 <sup>b, c</sup>	Α	
Marrian Danier Dissipation	T <sub>A</sub> = 25 °C	P <sub>D</sub>	0.236 <sup>b, c</sup>	- w	
Maximum Power Dissipation <sup>a</sup>	T <sub>A</sub> = 70 °C	] 'D	0.151 <sup>b, c</sup>		
Operating Junction and Storage Temperature Rar	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C		

THERMAL RESISTANCE RATINGS						
Parameter	Symbol	Typical	Maximum	Unit		
Adamiana kanadian ta Anakian ta d	t ≤ 5 s	B	440	530	°C/W	
Maximum Junction-to-Ambient <sup>b, d</sup>	Steady State	$R_{thJA}$	540	650		

#### Notes:

- a. Based on  $T_C = 25$  °C.
- b. Surface mounted on 1" x 1" FR4 board.
- c. t = 5 s.
- d. Maximum under steady state conditions is 650  $^{\circ}\text{C/W}.$

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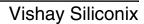


Parameter Symbol Te		Test Conditions	Min.	Min. Typ.	Max.	Unit
Static			•			•
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	30			V
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I <sub>D</sub> = 250 μA		24.5		mV/°C
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	η <sub>D</sub> = 250 μΑ		- 3.81		mv/°C
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	0.7		1.55	V
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$			± 100	nA
Zovo Coto Voltogo Dvoin Current		V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V			1	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 85 °C			10	μΑ
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} = \ge 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	6			Α
Drain-Source On-State Resistance <sup>a</sup>	<b>D</b>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 1.2 A	0.082 0.09		0.099	
	R <sub>DS(on)</sub>	V <sub>GS</sub> = 2.5 V, I <sub>D</sub> = 1.0 A		0.116	0.140	Ω
Forward Transconductance	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 1.2 A		5		S
Dynamic <sup>b</sup>						
Input Capacitance	C <sub>iss</sub>			385		
Output Capacitance	C <sub>oss</sub>	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		55		pF
Reverse Transfer Capacitance	C <sub>rss</sub>			30		
Total Cata Charge	0	Vpc = 15 V Vcc = 5 V lp = 1 2 A		3.8	8.3	
Total Gate Charge	Q <sub>g</sub>			3.5	4.1	nC
Gate-Source Charge	Q <sub>gs</sub>	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 4.6 \text{ A}$		1.1		
Gate-Drain Charge	Q <sub>gd</sub>			0.98		
Gate Resistance	R <sub>g</sub>	f = 1 MHz		4.7	6.2	Ω
Turn-On Delay Time	t <sub>d(on)</sub>			10	15	
Rise Time	t <sub>r</sub>	$V_{DD} = 15 \text{ V}, R_{L} = 15 \Omega$		22	33	ns
Turn-Off DelayTime	t <sub>d(off)</sub>	$I_D \cong 1.0 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$		14	21	
Fall Time	t <sub>f</sub>			6	9	1
Drain-Source Body Diode Characterist	ics					
Pulse Diode Forward Current <sup>a</sup>	I <sub>SM</sub>				6	Α
Body Diode Voltage	$V_{SD}$	I <sub>S</sub> = 1.2 A		0.8	1.2	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>			19.4	29.5	nC
Body Diode Reverse Recovery Charge	$Q_{rr}$	L_ = 3.9.4. dl/dt = 100.4/us		18.43	27.5	
Reverse Recovery Fall Time	ta	$I_F = 3.8 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}$		16.4		ns
Reverse Recovery Rise Time	t <sub>b</sub>			3		

### Notes:

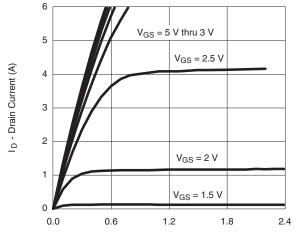
- a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



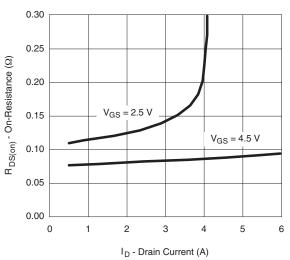


## **TYPICAL CHARACTERISTICS** ( $T_A = 25$ °C, unless otherwise noted)

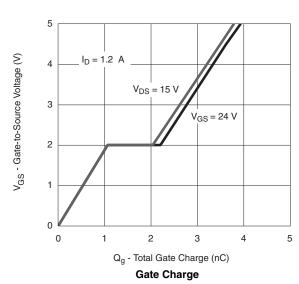


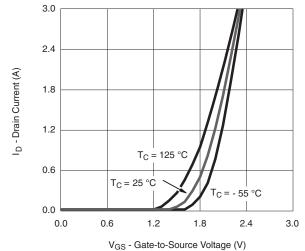
 $V_{\text{DS}}$  - Drain-to-Source Voltage (V)

### **Output Characteristics**

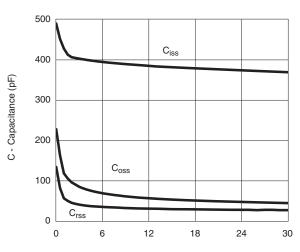


On-Resistance vs. Drain Current



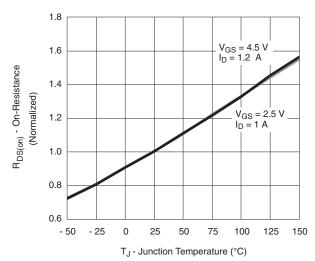


Transfer Characteristics Curves vs. Temp.



V<sub>DS</sub> - Drain-to-Source Voltage (V)

### Capacitance

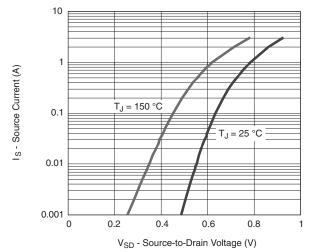


On-Resistance vs. Junction Temperature

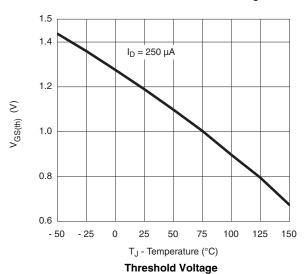
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## **TYPICAL CHARACTERISTICS** ( $T_A = 25$ °C, unless otherwise noted)

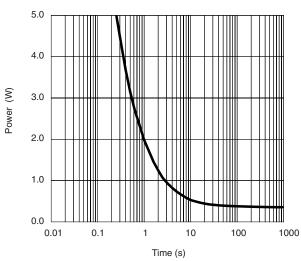


### Source-Drain Diode Forward Voltage

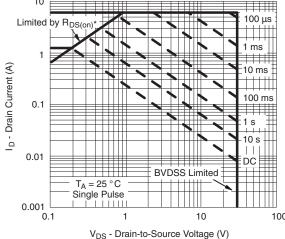


 $C_{\text{SO}}$  0.18  $C_{\text{D}}$  0.18  $C_{\text{D}}$  0.12  $C_{\text{D}}$  0.12  $C_{\text{D}}$  0.00  $C_{\text{D}}$  0

R<sub>DS(on)</sub> vs. V<sub>GS</sub> vs. Temperature



Single Pulse Power



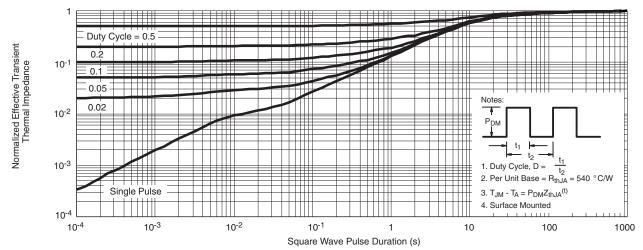
\*  $V_{GS}$  > minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

Safe Operating Area, Junction-to-Ambient





## **TYPICAL CHARACTERISTICS** ( $T_A = 25$ °C, unless otherwise noted)

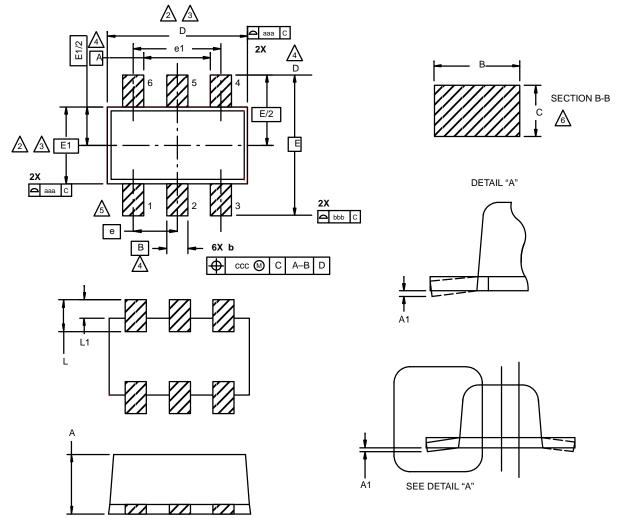


Normalized Thermal Transient Impedance, Junction-to-Ambient

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="https://www.vishay.com/ppg?73893">www.vishay.com/ppg?73893</a>.



## SC89: 6- LEADS (SOT-563F)



### NOTES:

1. Dimensions in millimeters.



Dimension D does not include mold flash, protrusions or gate burrs. Mold flush, protrusions or gate burrs shall not exceed 0.15 mm per dimension E1 does not include interlead flash or protrusion, interlead flash or protrusion shall not exceed 0.15 mm per side.



Dimensions D and E1 are determined at the outmost extremes of the plastic body exclusive of mold flash, the bar burrs, gate burrs and interlead flash, but including any mismatch between the top and the bottom of the plastic body.



Datums A, B and D to be determined 0.10 mm from the lead tip.



Terminal numbers are shown for reference only.



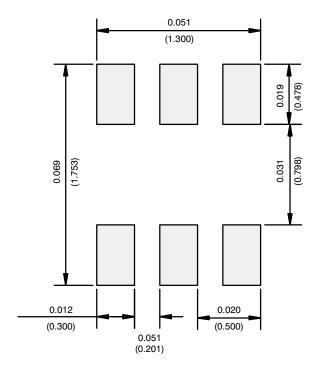
These dimensions apply to the flat section of the lead between 0.08 mm and 0.15 mm from the lead tip.

	MILLIM	ETERS			Tolerances Of Form And			
Dim	Min	Max	Note	Symbol	Position			
Α	0.56	0.60		aaa	0.10			
A1	0.00	0.10		bbb	0.10			
b	0.15	0.30		ccc	0.10			
С	0.10	0.18						
D	1.50	1.70	2, 3					
E	1.55	1.70						
E1	1.20 BSC		2, 3					
е	0.50 BSC							
e1	1.00 BSC							
L	0.35 BSC							
L1	0.20 BSC							

DWG: 5880



## **RECOMMENDED MINIMUM PADS FOR SC-89: 6-Lead**



Recommended Minimum Pads Dimensions in Inches/(mm)

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APPLICATION NOTE



## **Legal Disclaimer Notice**

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Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

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