

# FDC638APZ

## P-Channel 2.5V PowerTrench® Specified MOSFET

-20V, -4.5A, 43mΩ

### Features

- Max  $r_{DS(on)}$  = 43mΩ at  $V_{GS} = -4.5V$ ,  $I_D = -4.5A$
- Max  $r_{DS(on)}$  = 68mΩ at  $V_{GS} = -2.5V$ ,  $I_D = -3.8A$
- Low gate charge (8nC typical).
- High performance trench technology for extremely low  $r_{DS(on)}$ .
- SuperSOT™ -6 package: small footprint (72% smaller than standard SO-8) low profile (1mm thick).
- RoHS Compliant



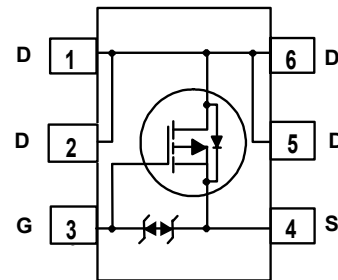
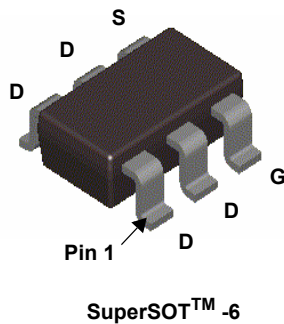
### General Description

This P-Channel 2.5V specified MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance

These devices are well suited for battery power applications: load switching and power management, battery charging circuits, and DC/DC conversion.

### Application

- DC - DC Conversion



### MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	-20	V
$V_{GS}$	Gate to Source Voltage	±12	V
$I_D$	Drain Current -Continuous (Note 1a)	-4.5	A
	-Pulsed	-20	
$P_D$	Power Dissipation (Note 1a)	1.6	W
	Power Dissipation (Note 1b)	0.8	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	78	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	156	

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity
.638Z	FDC638APZ	7"	8mm	3000 units

## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = -250\mu\text{A}, V_{GS} = 0\text{V}$	-20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\mu\text{A}$ , referenced to $25^\circ\text{C}$		-9.4		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -16\text{V},$ $V_{GS} = 0\text{V}$ $T_J = 55^\circ\text{C}$			-1 -10	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 12\text{V}, V_{DS} = 0\text{V}$			$\pm 10$	$\mu\text{A}$

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = -250\mu\text{A}$	-0.4	-0.8	-1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250\mu\text{A}$ , referenced to $25^\circ\text{C}$		2.9		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = -4.5\text{V}, I_D = -4.5\text{A}$		37	43	m $\Omega$
		$V_{GS} = -2.5\text{V}, I_D = -3.8\text{A}$		52	68	
		$V_{GS} = -4.5\text{V}, I_D = -4.5\text{A}, T_J = 125^\circ\text{C}$		50	72	
$I_{D(on)}$	On-State Drain Current	$V_{GS} = -10\text{V}, V_{DS} = -4.5\text{A}$	-20			A
$g_{FS}$	Forward Transconductance	$V_{DS} = -10\text{V}, I_D = -4.5\text{A}$		18		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = -10\text{V}, V_{GS} = 0\text{V},$ $f = 1\text{MHz}$		750	1000	pF
$C_{oss}$	Output Capacitance			155	210	pF
$C_{rss}$	Reverse Transfer Capacitance			130	195	pF

### Switching Characteristics (Note 2)

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -5\text{V}, I_D = -4.5\text{A}$ $V_{GS} = -4.5\text{V}, R_{GEN} = 6\Omega$		6	12	ns
$t_r$	Rise Time			20	31	ns
$t_{d(off)}$	Turn-Off Delay Time			48	77	ns
$t_f$	Fall Time			47	72	ns
$Q_{g(TOT)}$	Total Gate Charge		$V_{GS} = 0\text{V}$ to $-4.5\text{V}$ $V_{DD} = -5\text{V}$ $I_D = -4.5\text{A}$		8	12
$Q_{gs}$	Gate to Source Gate Charge			2		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			2		nC

### Drain-Source Diode Characteristics

$I_S$	Maximum Continuous Drain-Source Diode Forward Current				-1.3	A
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = -1.3\text{A}$ (Note 2)		-0.8	-1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = -4.5\text{A}, di/dt = 100\text{A}/\mu\text{s}$		24	36	ns
$Q_{rr}$	Reverse Recovery Charge			13	20	nC

#### Notes:

1:  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by user's board design.



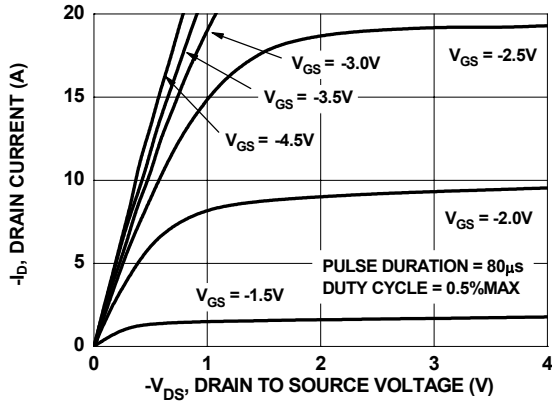
a.  $78^\circ\text{C}/\text{W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper on FR-4 board.



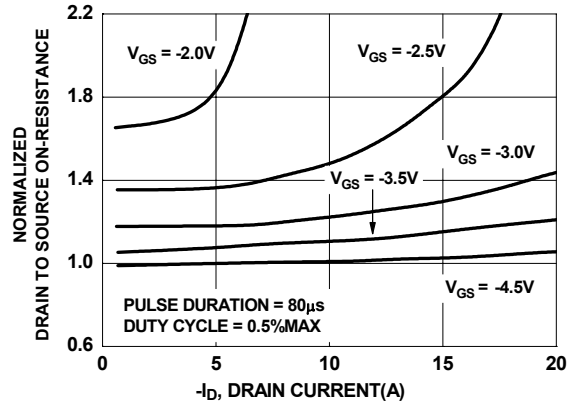
b.  $156^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper.

2: Pulse Test: Pulse Width <  $300\mu\text{s}$ , Duty cycle < 2.0%.

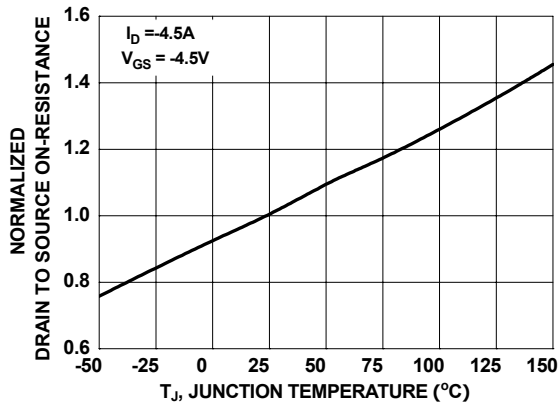
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



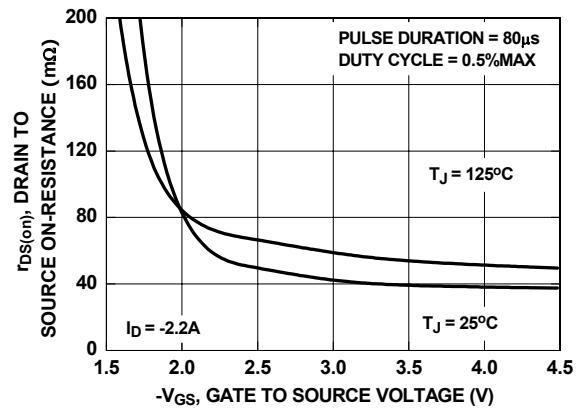
**Figure 1. On-Region Characteristics**



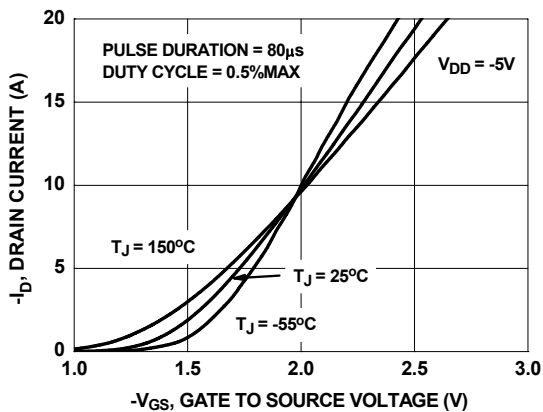
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



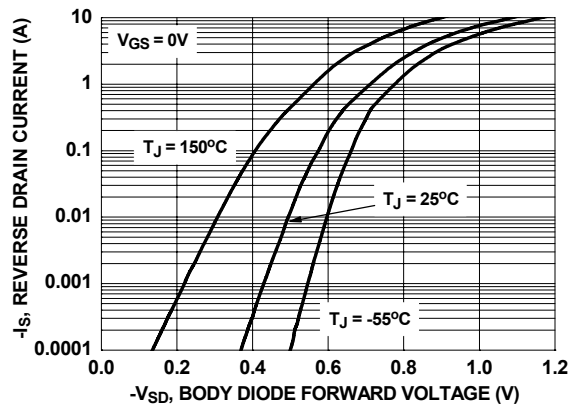
**Figure 3. Normalized On-Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**



**Figure 5. Transfer Characteristics**



**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

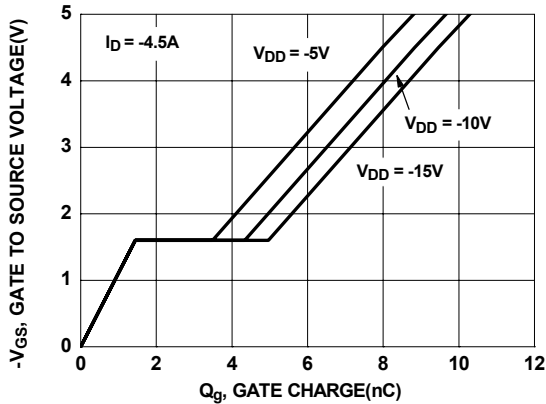


Figure 7. Gate Charge Characteristics

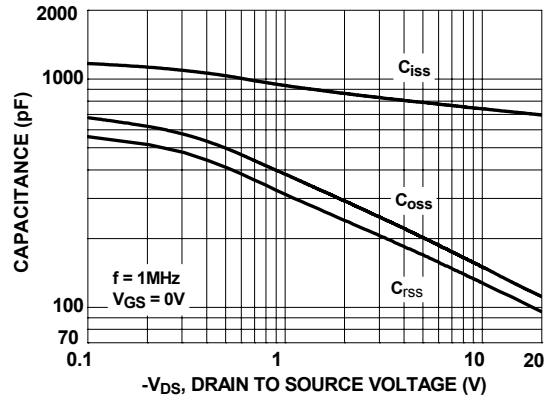


Figure 8. Capacitance vs Drain to Source Voltage

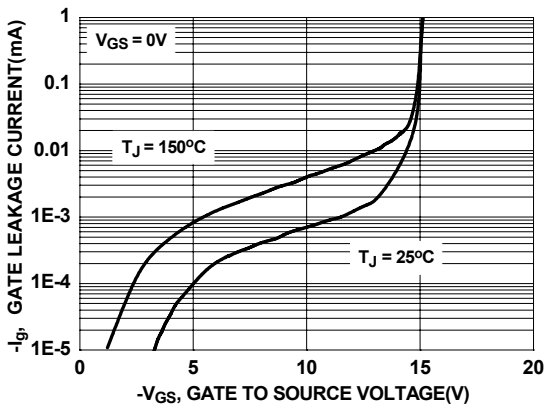


Figure 9. Gate Leakage Current vs Gate to Source Voltage

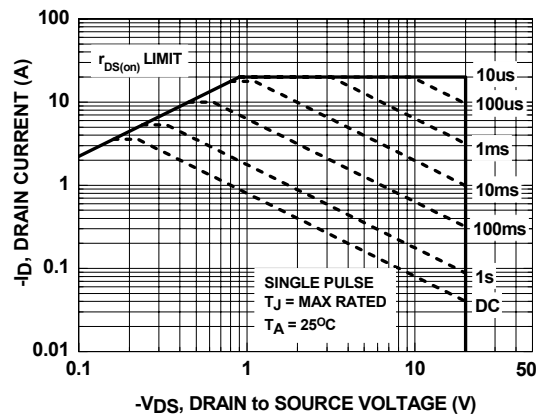


Figure 10. Forward Bias Safe Operating Area

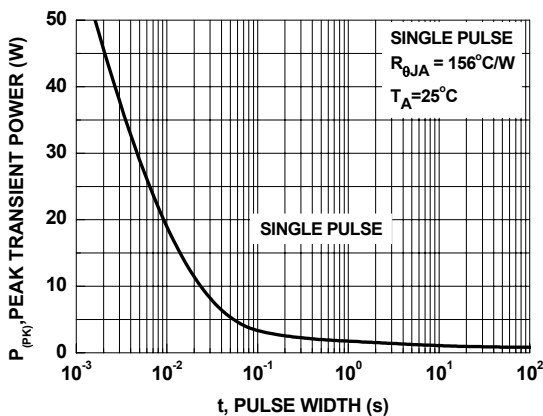


Figure 11. Single Pulse Maximum Power Dissipation

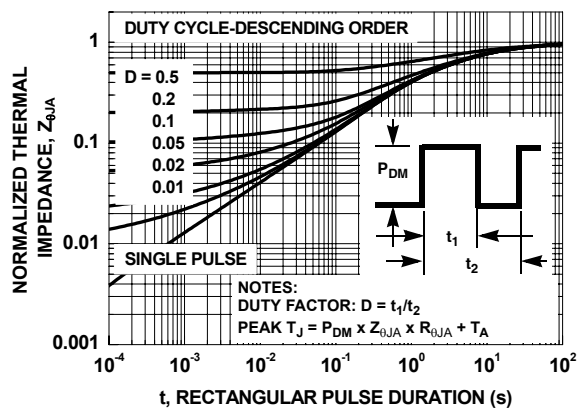


Figure 12. Transient Thermal Response Curve

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