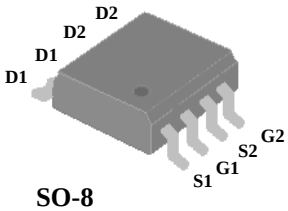
Advanced Power Electronics Corp.

N AND P-CHANNEL ENHANCEMENT MODE POWER MOSFET

- ▼ **Simple Drive Requirement**
- ▼ **Low Gate Charge**
- ▼ **Fast Switching Performance**
- ▼ **RoHS Compliant & Halogen-Free**



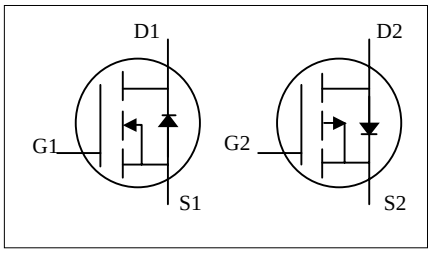
SO-8

N-CH	BV_{DSS}	30V
	$R_{DS(ON)}$	10mΩ
	I_D	11.2A
P-CH	BV_{DSS}	-30V
	$R_{DS(ON)}$	21mΩ
	I_D	-8A

Description

Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SO-8 package is widely preferred for commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.



Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		N-channel	P-channel	
V_{DS}	Drain-Source Voltage	30	-30	V
V_{GS}	Gate-Source Voltage	±20	±20	V
I_D@T_A=25℃	Continuous Drain Current[3]	11.2	-8.0	A
I_D@T_A=70℃	Continuous Drain Current[3]	9.0	-6.4	A
I_{DM}	Pulsed Drain Current[1]	40	-30	A
P_D@T_A=25℃	Total Power Dissipation	2		W
T_{STG}	Storage Temperature Range	-55 to 150		℃
T_J	Operating Junction Temperature Range	-55 to 150		℃

Thermal Data

Symbol	Parameter	Value	Unit
Rthj-a	Maximum Thermal Resistance, Junction-ambient[3]	62.5	℃/W

N-CH Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	30	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V, I_D=10A	-	-	10	mΩ
		V_{GS}=4.5V, I_D=7A	-	-	16	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	1	-	3	V
g_{fs}	Forward Transconductance	V_{DS}=10V, I_D=10A	-	20	-	S
I_{DSS}	Drain-Source Leakage Current	V_{DS}=24V, V_{GS}=0V	-	-	10	uA
I_{GSS}	Gate-Source Leakage	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Q_g	Total Gate Charge[2]	I_D=10A	-	12	19.2	nC
Q_{gs}	Gate-Source Charge	V_{DS}=15V	-	2.5	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	V_{GS}=4.5V	-	7.5	-	nC
$t_{d(on)}$	Turn-on Delay Time[2]	V_{DS}=15V	-	9	-	ns
t_r	Rise Time	I_D=1A	-	6.5	-	ns
$t_{d(off)}$	Turn-off Delay Time	R_G=3.3Ω,V_{GS}=10V	-	23	-	ns
t_f	Fall Time	R_D=15Ω	-	9.5	-	ns
C_{iss}	Input Capacitance	V_{GS}=0V	-	715	1140	pF
C_{oss}	Output Capacitance	V_{DS}=25V	-	220	-	pF
C_{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	160	-	pF
R_g	Gate Resistance	f=1.0MHz	-	2.2	-	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage[2]	I_S=1.7A, V_{GS}=0V	-	-	1.2	V
t_{rr}	Reverse Recovery Time[2]	I_S=10A, V_{GS}=0V,	-	27	-	ns
Q_{rr}	Reverse Recovery Charge	dI/dt=100A/μs	-	18	-	nC

P-CH Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250uA	-30	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=-10V, I_D=-7A	-	-	21	mΩ
		V_{GS}=-4.5V, I_D=-5A	-	-	32	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250uA	-1	-	-3	V
g_{fs}	Forward Transconductance	V_{DS}=-10V, I_D=-7A	-	15	-	S
I_{DSS}	Drain-Source Leakage Current	V_{DS}=-24V, V_{GS}=0V	-	-	-10	uA
I_{GSS}	Gate-Source Leakage	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Q_g	Total Gate Charge[2]	I_D=-7A	-	15	24	nC
Q_{gs}	Gate-Source Charge	V_{DS}=-15V	-	3	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	V_{GS}=-4.5V	-	8	-	nC
$t_{d(on)}$	Turn-on Delay Time[2]	V_{DS}=-15V	-	10.5	-	ns
t_r	Rise Time	I_D=-1A	-	6.5	-	ns
$t_{d(off)}$	Turn-off Delay Time	R_G=3.3Ω,V_{GS}=-10V	-	40	-	ns
t_f	Fall Time	R_D=15Ω	-	29	-	ns
C_{iss}	Input Capacitance	V_{GS}=0V	-	1260	2000	pF
C_{oss}	Output Capacitance	V_{DS}=-25V	-	210	-	pF
C_{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	185	-	pF
R_g	Gate Resistance	f=1.0MHz	-	5.6	-	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage[2]	I_S=-1.7A, V_{GS}=0V	-	-	-1.2	V
t_{rr}	Reverse Recovery Time[2]	I_S=-7A, V_{GS}=0V,	-	22	-	ns
Q_{rr}	Reverse Recovery Charge	dI/dt=100A/μs	-	12	-	nC

Notes:

1.Pulse width limited by Max. junction temperature.

2.Pulse test

3.Surface mounted on 1 in^2 copper pad of FR4 board ; 135 ℃/W when mounted on Min. copper pad.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.
USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.
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APEC RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN.

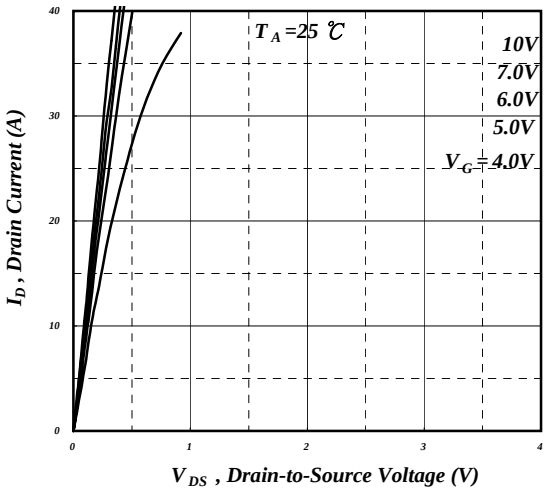


Fig 1. Typical Output Characteristics

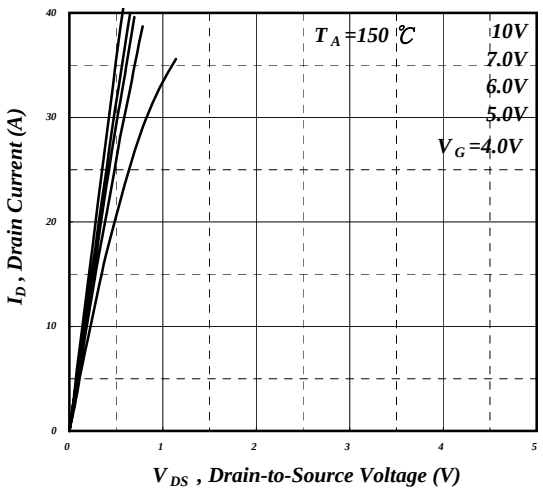


Fig 2. Typical Output Characteristics

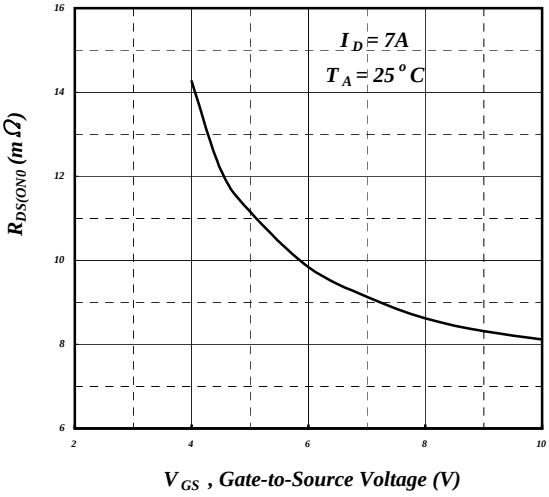


Fig 3. On-Resistance v.s. Gate Voltage

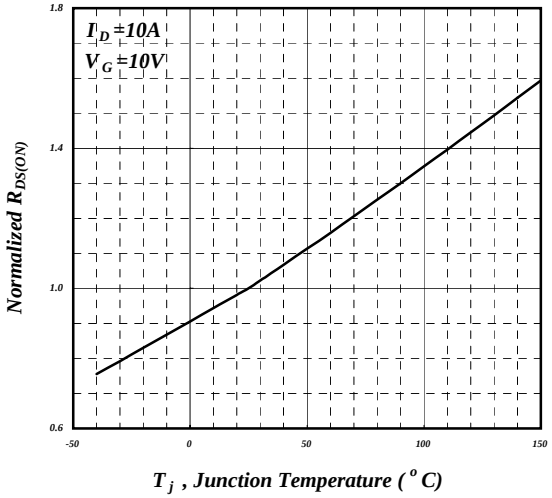


Fig 4. Normalized On-Resistance v.s. Junction Temperature

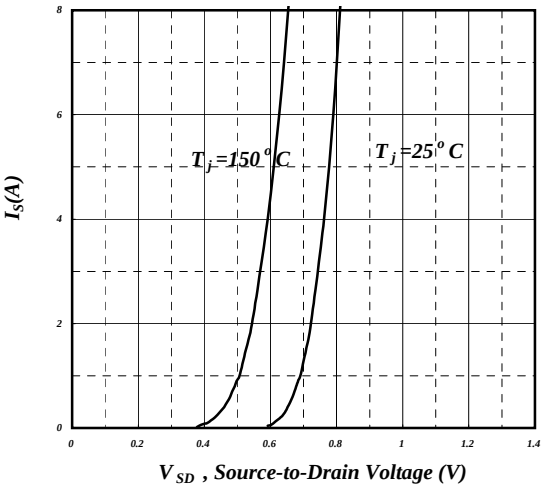


Fig 5. Forward Characteristic of Reverse Diode

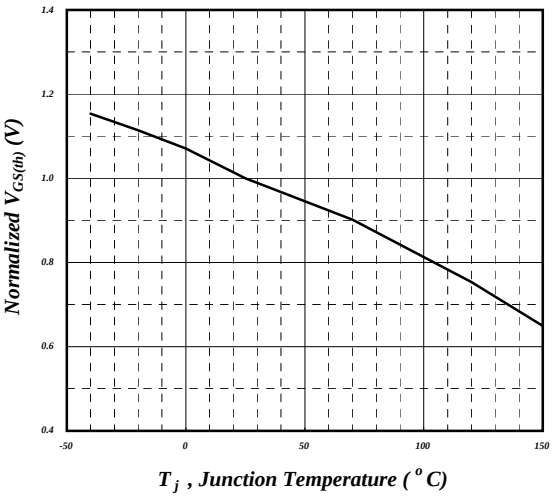


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

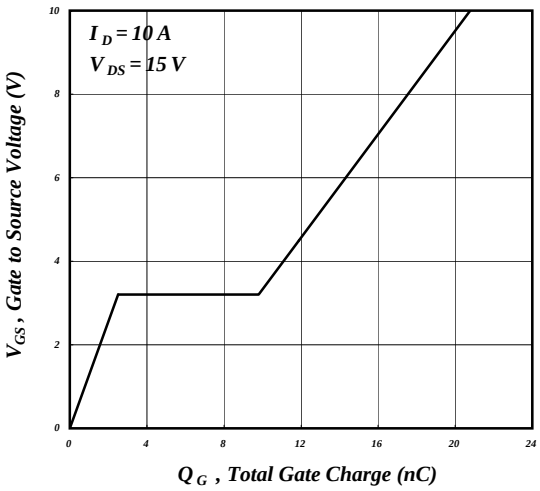


Fig 7. Gate Charge Characteristics

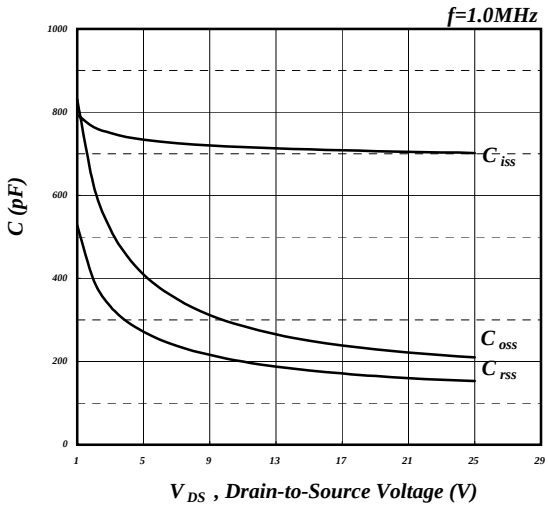


Fig 8. Typical Capacitance Characteristics

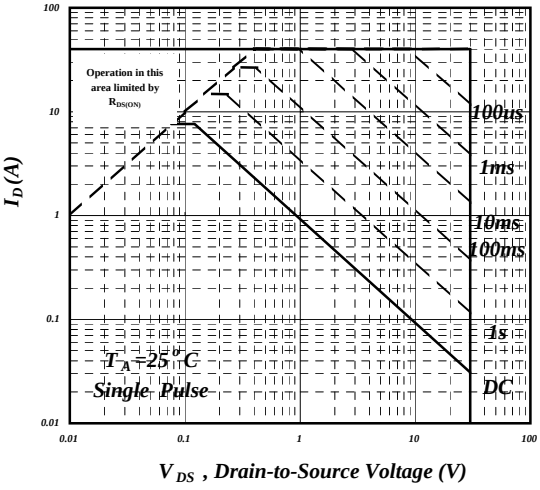


Fig 9. Maximum Safe Operating Area

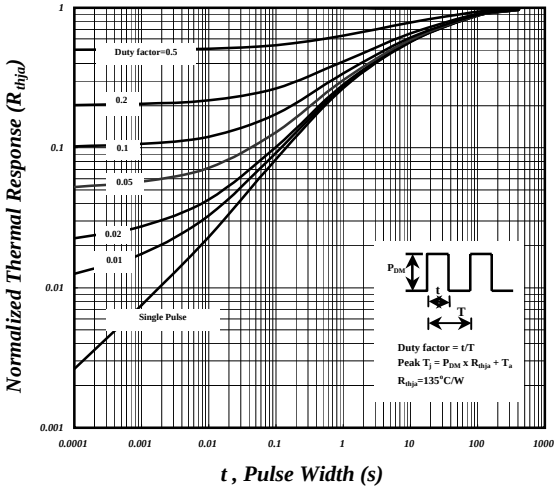


Fig 10. Effective Transient Thermal Impedance

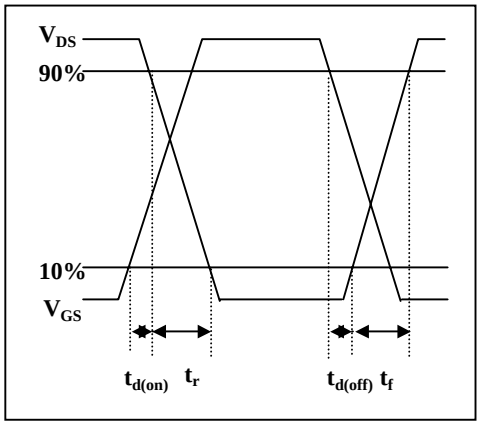


Fig 11. Switching Time Waveform

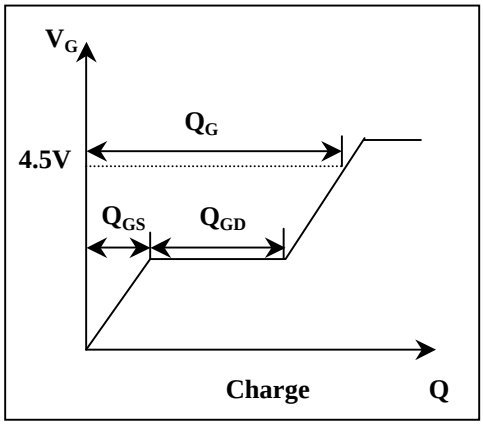
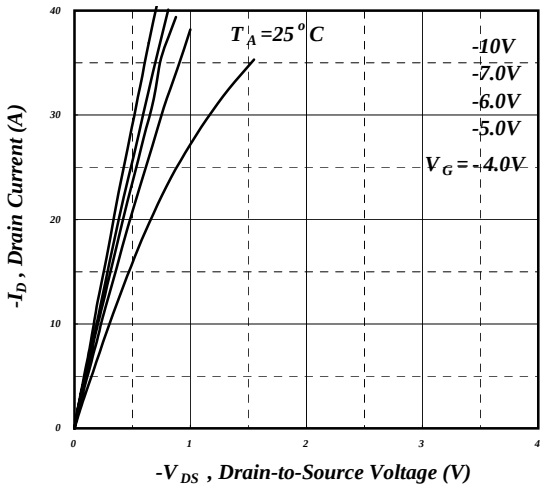


Fig 12. Gate Charge Waveform



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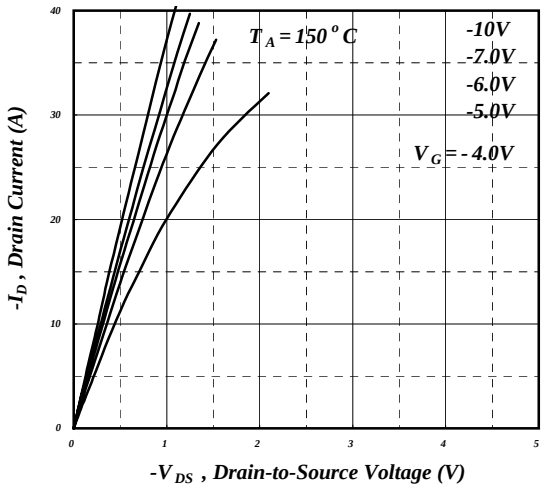
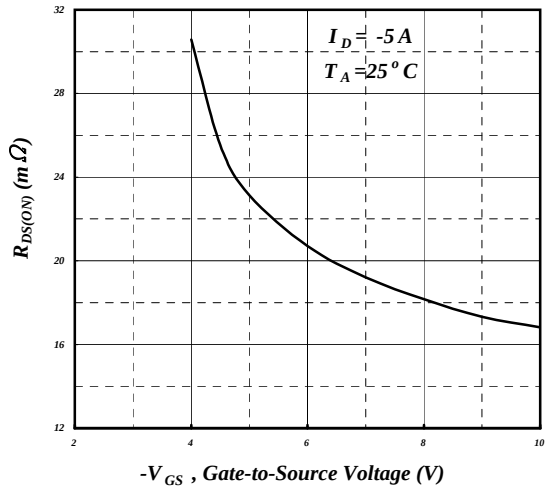


Fig 2. Typical Output Characteristics



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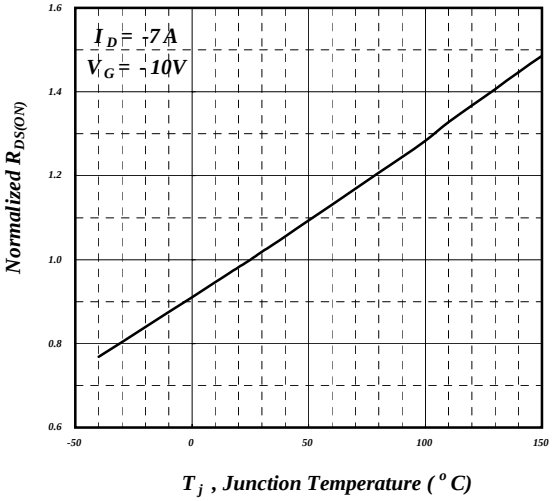
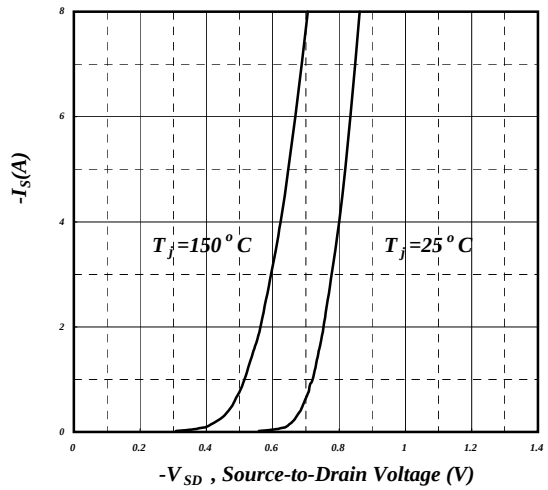


Fig 4. Normalized On-Resistance v.s. Junction Temperature



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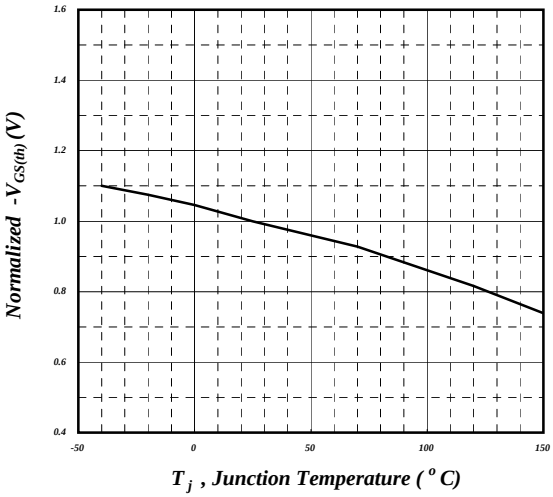
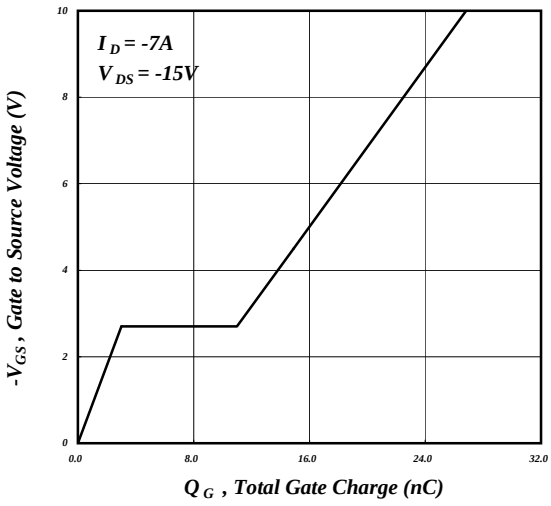


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

P-Channel



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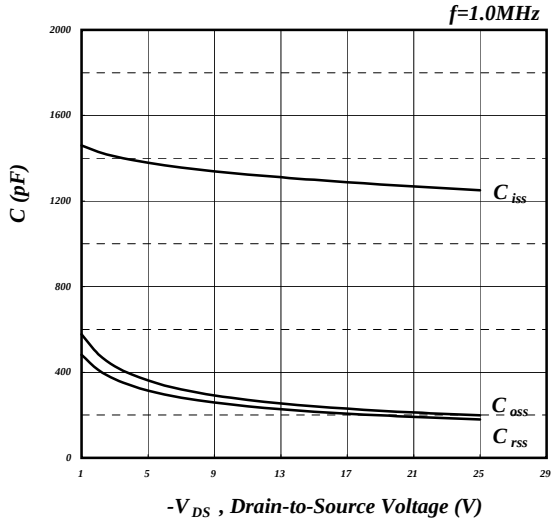

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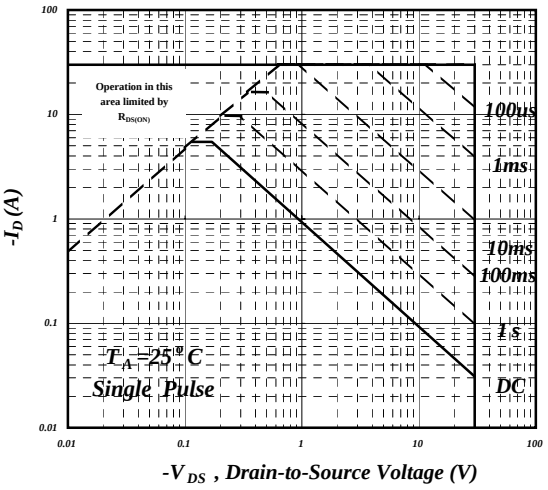

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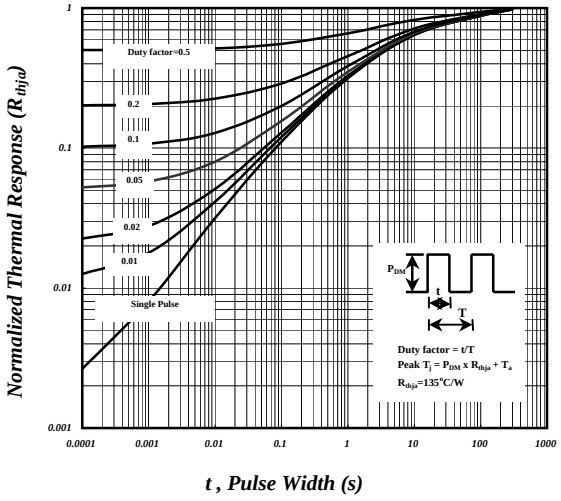

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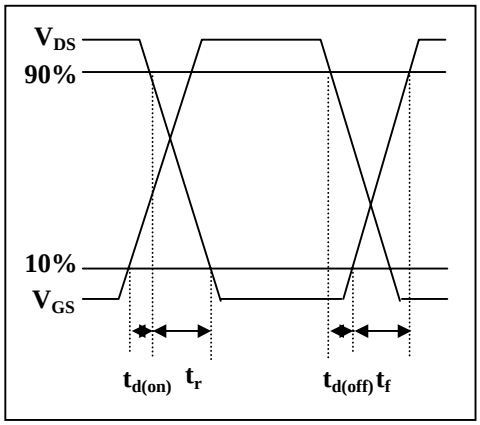

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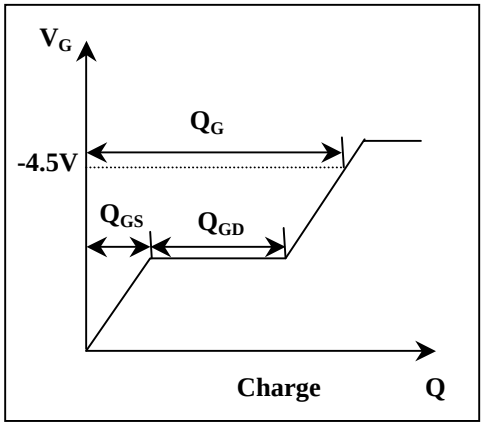

Fig 12. Gate Charge Waveform