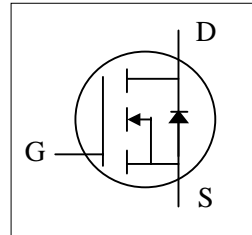


- ▼ Ultra-low Forward Diode
- ▼ Low Conductance Loss
- ▼ Low Profile (< 0.7mm)
- ▼ Compatible with DirectFET® Package MX Footprint and Outline

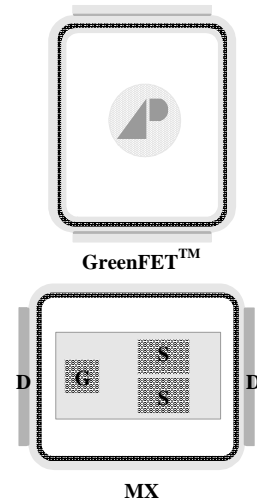


BV_{DSS}	30V
$R_{DS(ON)}$	1.8mΩ
I_D	32A

Description

The AP1004CMX used the latest APEC Power MOSFET silicon technology with the advanced technology packaging to provide the lowest on-resistance loss, low profile and dual sided cooling compatible.

The GreenFET™(A) package is compatible with existing soldering techniques and is ideal for power application, especially for high frequency / high efficiency DC-DC converters.



(A) GreenFET™ products use DirectFET® technology licensed from International Rectifier Corporation. DirectFET® is a registered trademark of International Rectifier Corporation.

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	30	V
V_{GS}	Gate-Source Voltage	+20	V
$I_D@T_A=25^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V^3$	32	A
$I_D@T_A=70^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V^3$	25	A
$I_D@T_C=25^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V^4$	160	A
I_{DM}	Pulsed Drain Current ¹	250	A
$P_D@T_A=25^{\circ}C$	Total Power Dissipation ³	2.8	W
$P_D@T_A=70^{\circ}C$	Total Power Dissipation ³	1.8	W
$P_D@T_C=25^{\circ}C$	Total Power Dissipation ⁴	73.5	W
E_{AS}	Single Pulse Avalanche Energy ⁵	28.8	mJ
I_{AR}	Avalanche Current ¹	24	A
T_{STG}	Storage Temperature Range	-40 to 150	°C
T_J	Operating Junction Temperature Range	-40 to 150	°C

Thermal Data

Rthj-c	Maximum Thermal Resistance, Junction-case ⁴	1.7	°C/W
Rthj-a	Maximum Thermal Resistance, Junction-ambient ³	45	°C/W



Electrical Characteristics @T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	30	-	-	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =32A	-	1.3	1.8	mΩ
		V _{GS} =4.5V, I _D =25A	-	1.9	3.2	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	1	-	3	V
g _{fs}	Forward Transconductance	V _{DS} =10V, I _D =25A	45	80	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =20V, V _{GS} =0V	-	-	500	uA
I _{GSS}	Gate-Source Leakage	V _{GS} = +20V, V _{DS} =0V	-	-	+100	nA
Q _g	Total Gate Charge ²	I _D =25A V _{DS} =13V V _{GS} =4.5V	-	31.5	50	nC
Q _{gs1}	Pre-V _{th} Gate-Source Charge		-	5.3	-	nC
Q _{gs2}	Post-V _{th} Gate-Source Charge		-	1.7	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge		-	15.3	-	nC
Q _{godr}			-	9.2	-	nC
Q _{sw}			-	17	-	nC
t _{d(on)}	Turn-on Delay Time ²	V _{DS} =13V	-	20	-	ns
t _r	Rise Time	I _D =25A	-	130	-	ns
t _{d(off)}	Turn-off Delay Time	R _G = 1.8 Ω	-	25	-	ns
t _f	Fall Time	V _{GS} = 5 V	-	110	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	3300	5280	pF
C _{oss}	Output Capacitance	V _{DS} =25V	-	1600	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	350	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I _S	Continuous Source Current (Body Diode)		-	-	32	A
I _{SM}	Pulsed Source Current (Body Diode) ¹		-	-	250	A
V _{SD}	Forward On Voltage ²	I _S =10A, V _{GS} =0V	-	-	0.75	V
t _{rr}	Reverse Recovery Time ²	I _S =25A, V _{GS} =0V,	-	60	90	ns
Q _{rr}	Reverse Recovery Charge	dI/dt=100A/μs	-	75	113	nC

Notes:

- 1.Pulse width limited by Max junction temperature.
- 2.Pulse test
- 3.Surface mounted on 1 in² copper pad of FR4 board.
- 4.T_C measured with thermocouple mounted to top (Drain) of part.
- 5.Starting T_j=25°C , L=0.1mH , R_G=25Ω

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

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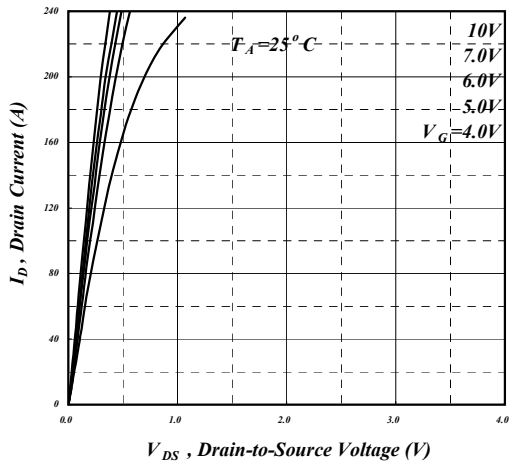


Fig 1. Typical Output Characteristics

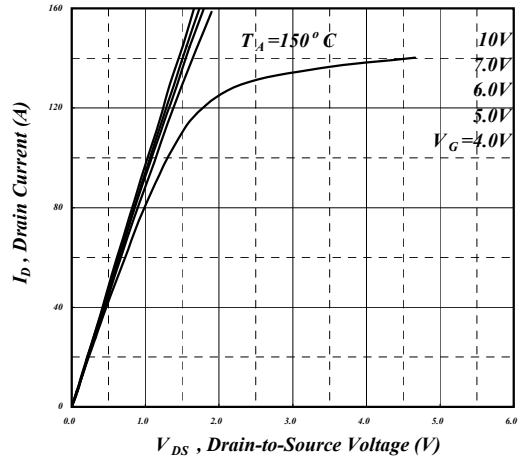


Fig 2. Typical Output Characteristics

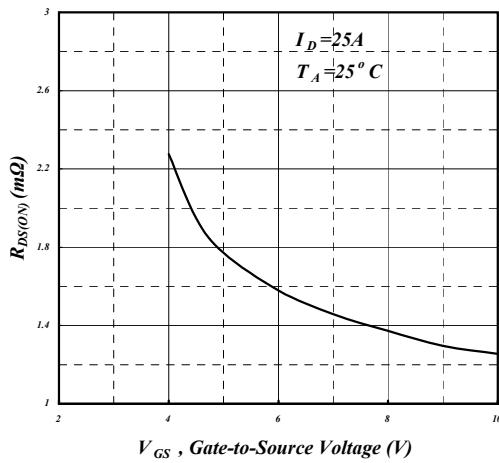


Fig 3. On-Resistance v.s. Gate Voltage

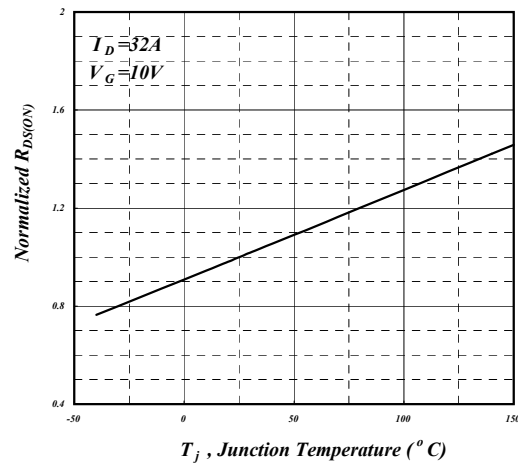


Fig 4. Normalized On-Resistance v.s. Junction Temperature

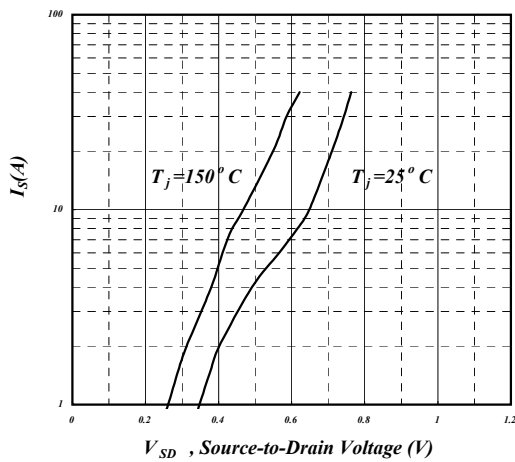


Fig 5. Forward Characteristic of Reverse Diode

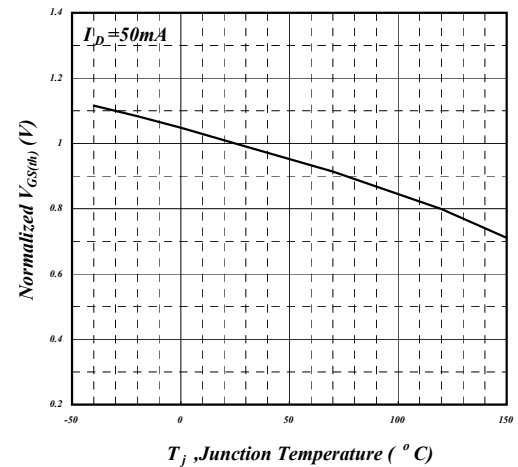


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

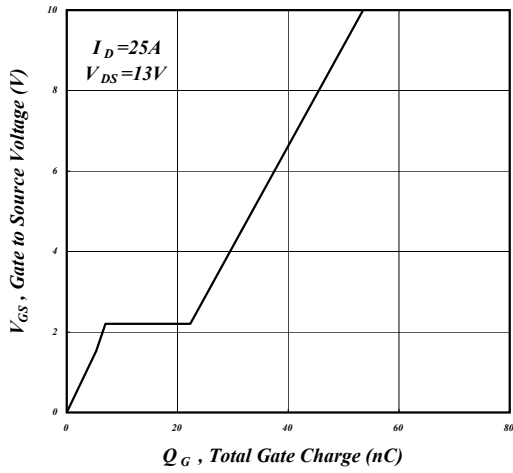


Fig 7. Gate Charge Characteristics

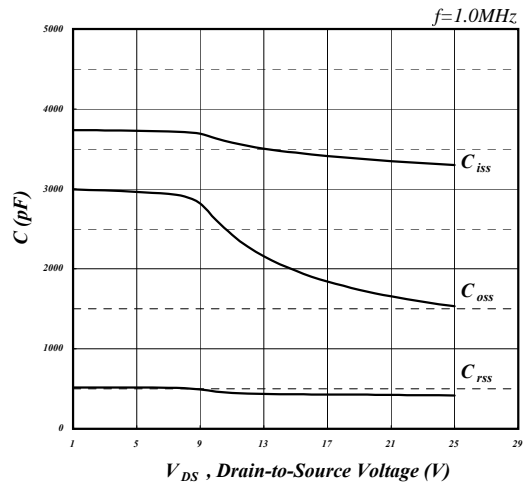


Fig 8. Typical Capacitance Characteristics

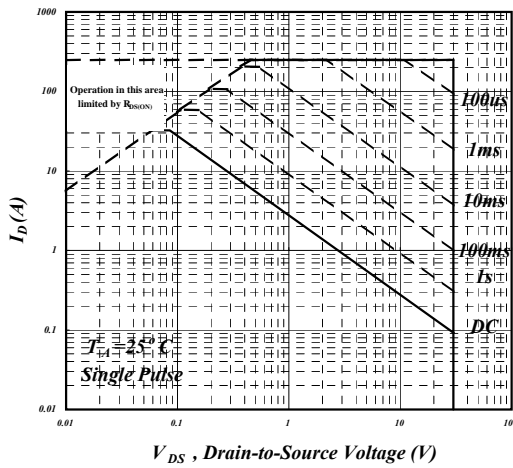


Fig 9. Maximum Safe Operating Area

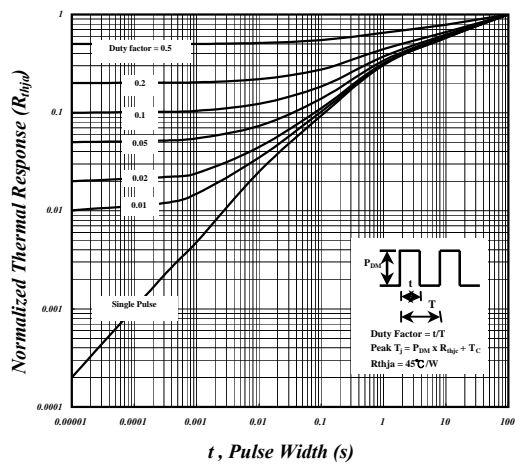


Fig 10. Effective Transient Thermal Impedance

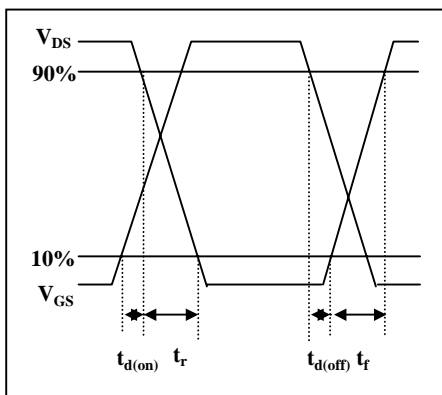


Fig 11. Switching Time Waveform

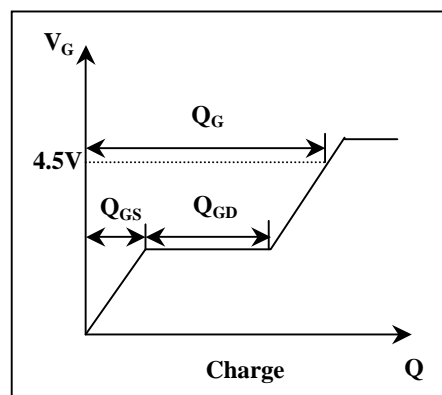


Fig 12. Gate Charge Waveform