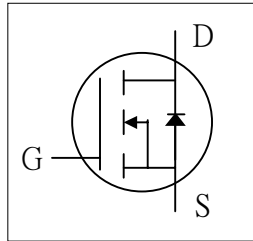




- ▼ 100% Avalanche Test
- ▼ Fast Switching Characteristic
- ▼ Simple Drive Requirement

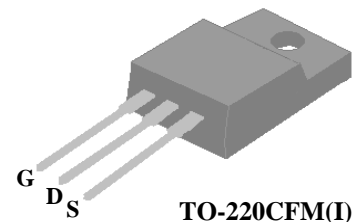


BV_{DSS}	650V
$R_{DS(ON)}$	2.4 Ω
I_D	4A

Description

Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220CFM isolation package is widely preferred for all commercial-industrial through hole applications.



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	650	V
V_{GS}	Gate-Source Voltage	+30	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, V_{GS} @ 10V	4	A
$I_D@T_C=100^\circ C$	Continuous Drain Current, V_{GS} @ 10V	2.5	A
I_{DM}	Pulsed Drain Current ¹	15	A
$P_D@T_C=25^\circ C$	Total Power Dissipation	33	W
	Linear Derating Factor	0.26	W/ $^\circ C$
E_{AS}	Single Pulse Avalanche Energy ²	8	mJ
I_{AR}	Avalanche Current	4	A
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$

Thermal Data

Symbol	Parameter	Value	Unit
Rthj-c	Maximum Thermal Resistance, Junction-case	3.8	$^\circ C/W$
Rthj-a	Maximum Thermal Resistance, Junction-ambient	65	$^\circ C/W$


Electrical Characteristics @ $T_j=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=1mA$	650	-	-	V
$\Delta BV_{DSS}/\Delta T_j$	Breakdown Voltage Temperature Coefficient	Reference to 25°C , $I_D=1mA$	-	0.6	-	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ³	$V_{GS}=10V, I_D=2A$	-	-	2.4	Ω
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2	-	4	V
g_{fs}	Forward Transconductance	$V_{DS}=10V, I_D=2A$	-	2.5	-	S
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=600V, V_{GS}=0V$	-	-	10	μA
	Drain-Source Leakage Current ($T_j=125^\circ\text{C}$)	$V_{DS}=480V, V_{GS}=0V$	-	-	500	μA
I_{GSS}	Gate-Source Leakage	$V_{GS}=\pm 30V, V_{DS}=0V$	-	-	± 100	nA
Q_g	Total Gate Charge ³	$I_D=4A$	-	16.7	-	nC
Q_{gs}	Gate-Source Charge	$V_{DS}=480V$	-	4.1	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	$V_{GS}=10V$	-	4.9	-	nC
$t_{d(on)}$	Turn-on Delay Time ³	$V_{DD}=300V$	-	11	-	ns
t_r	Rise Time	$I_D=4A$	-	8.3	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=10\Omega, V_{GS}=10V$	-	23.8	-	ns
t_f	Fall Time	$R_D=75\Omega$	-	8.2	-	ns
C_{iss}	Input Capacitance	$V_{GS}=0V$	-	950	-	pF
C_{oss}	Output Capacitance	$V_{DS}=25V$	-	65	-	pF
C_{rss}	Reverse Transfer Capacitance	$f=1.0MHz$	-	6	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I_S	Continuous Source Current (Body Diode)	$V_D=V_G=0V, V_S=1.5V$	-	-	4	A
I_{SM}	Pulsed Source Current (Body Diode) ¹		-	-	15	A
V_{SD}	Forward On Voltage ³	$T_j=25^\circ\text{C}, I_S=4A, V_{GS}=0V$	-	-	1.5	V

Notes:

1. Pulse width limited by max. junction temperature.
2. Starting $T_j=25^\circ\text{C}$, $V_{DD}=50V$, $L=1mH$, $R_G=25\Omega$, $I_{AS}=4A$.
3. Pulse test

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

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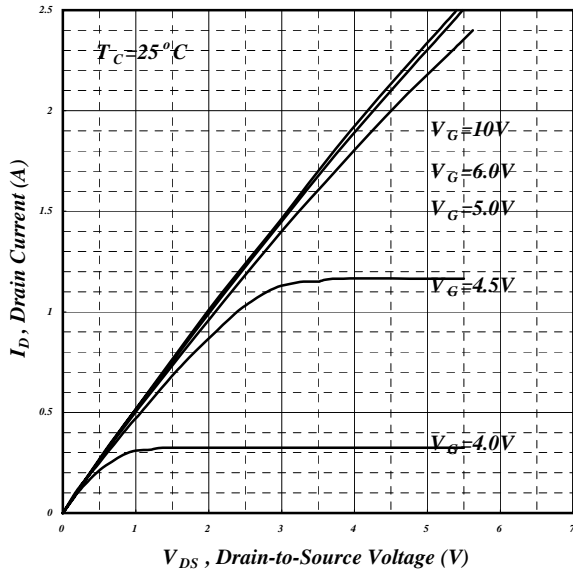


Fig 1. Typical Output Characteristics

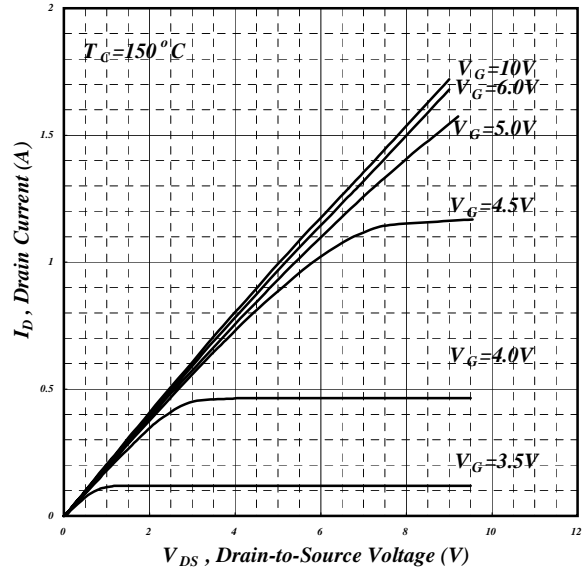


Fig 2. Typical Output Characteristics

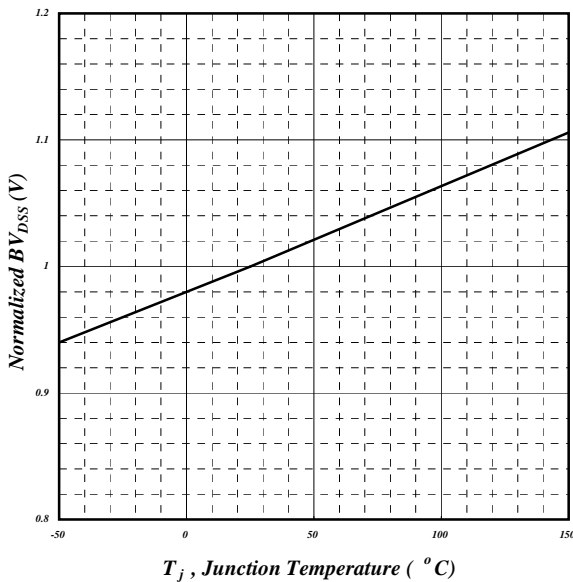


Fig 3. Normalized BV_{DSS} v.s. Junction Temperature

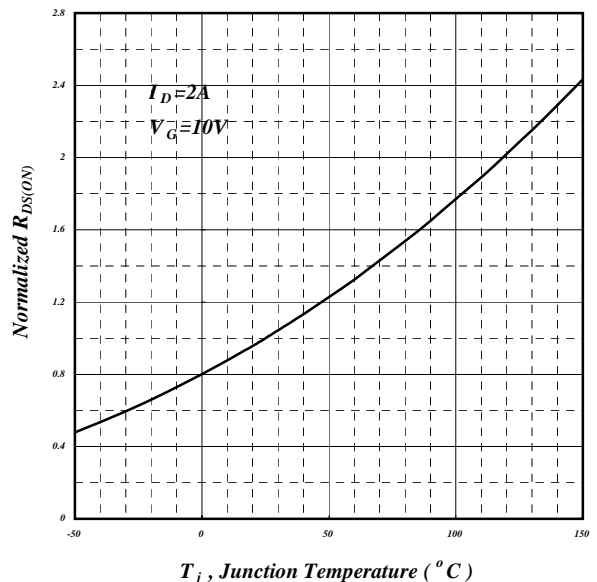


Fig 4. Normalized On-Resistance v.s. Junction Temperature

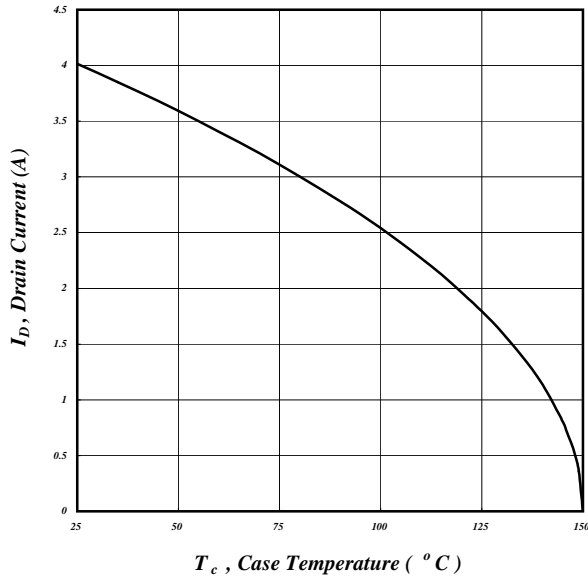


Fig 5. Maximum Drain Current v.s. Case Temperature

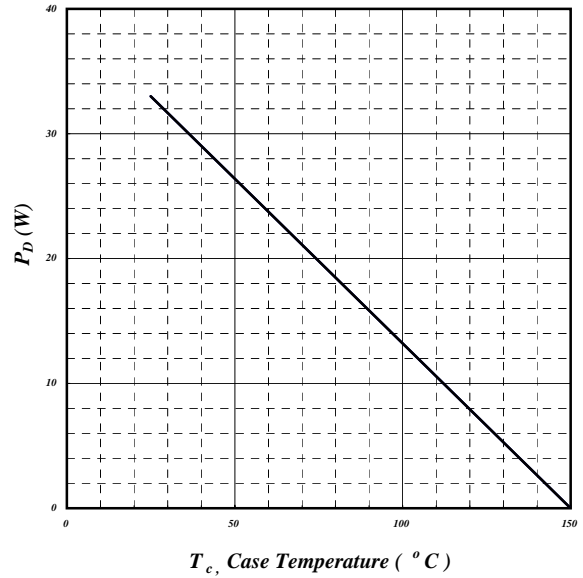


Fig 6. Typical Power Dissipation

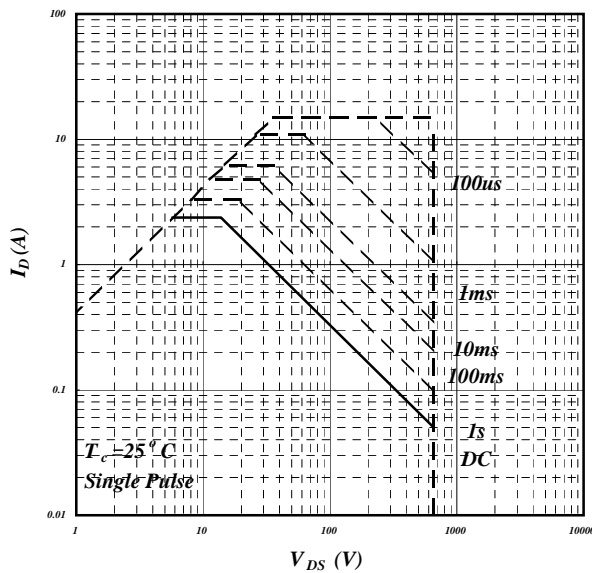


Fig 7. Maximum Safe Operating Area

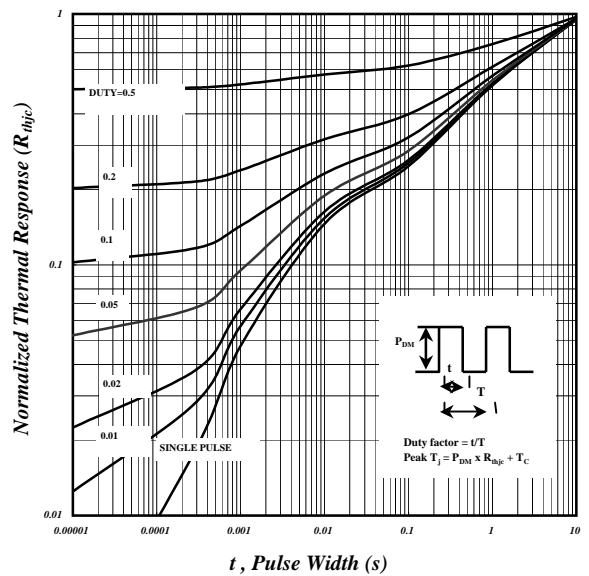


Fig 8. Effective Transient Thermal Impedance

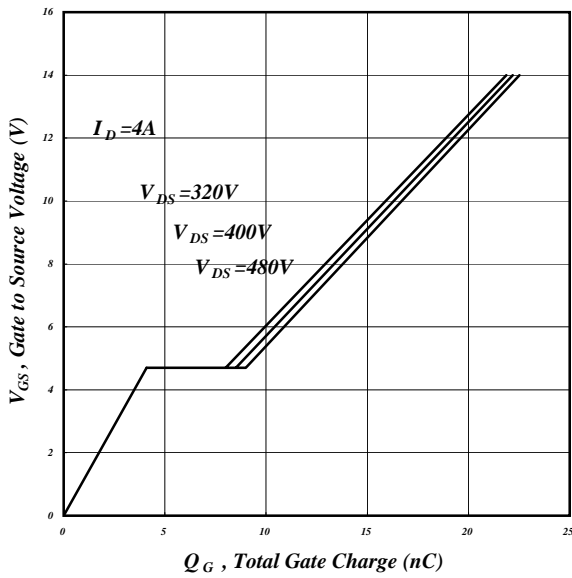


Fig 9. Gate Charge Characteristics

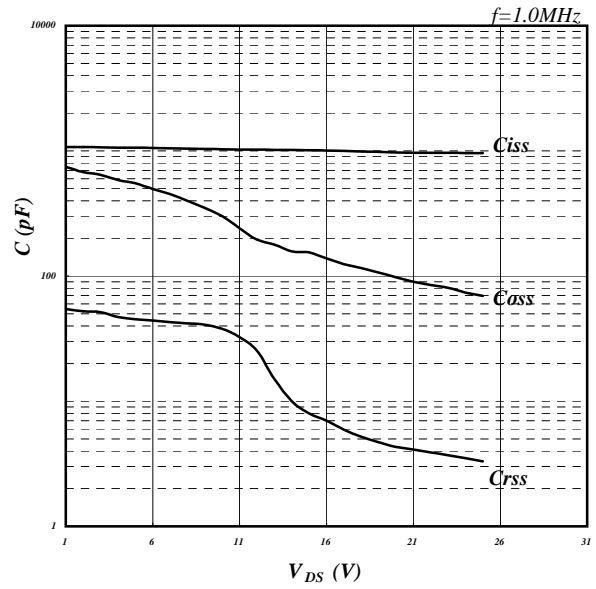


Fig 10. Typical Capacitance Characteristics

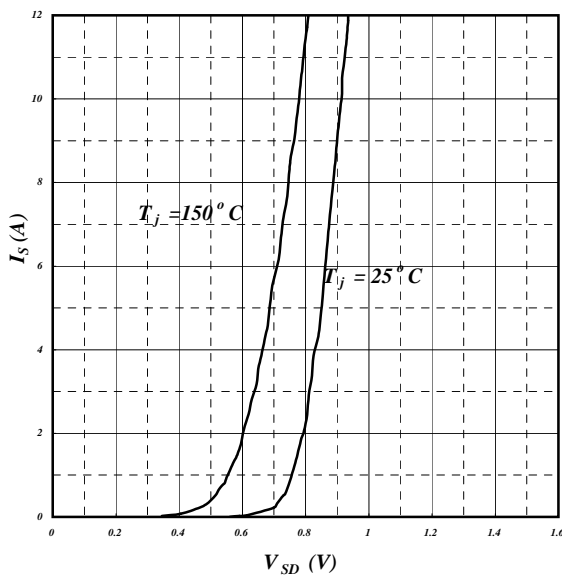


Fig 11. Forward Characteristic of Reverse Diode

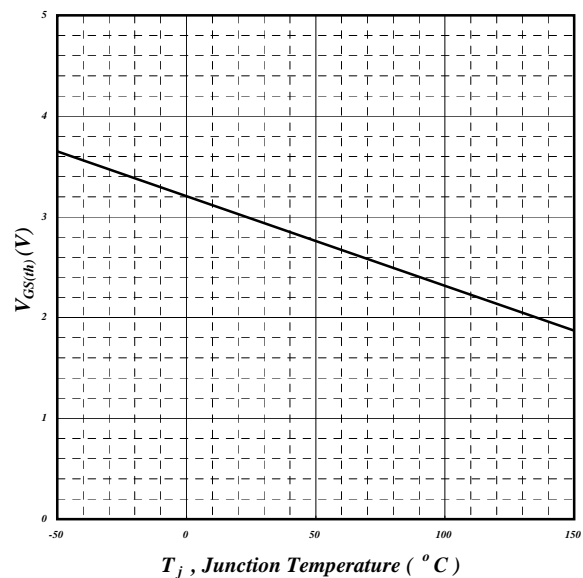


Fig 12. Gate Threshold Voltage v.s. Junction Temperature



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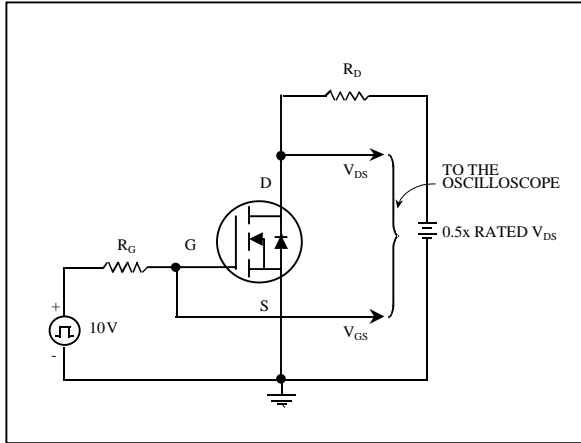


Fig 13. Switching Time Circuit

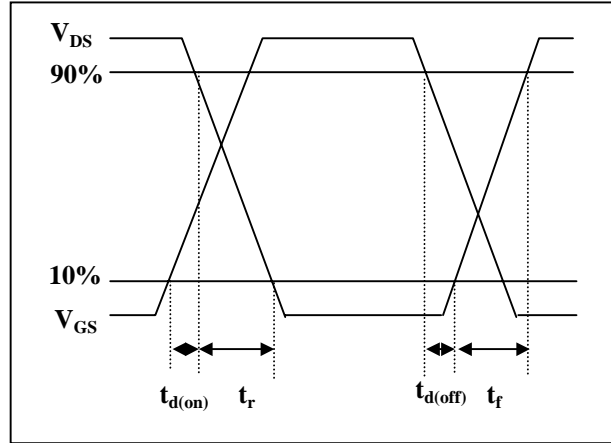


Fig 14. Switching Time Waveform

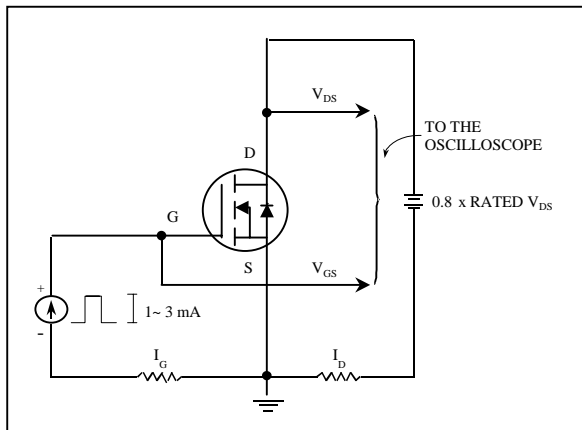


Fig 15. Gate Charge Circuit

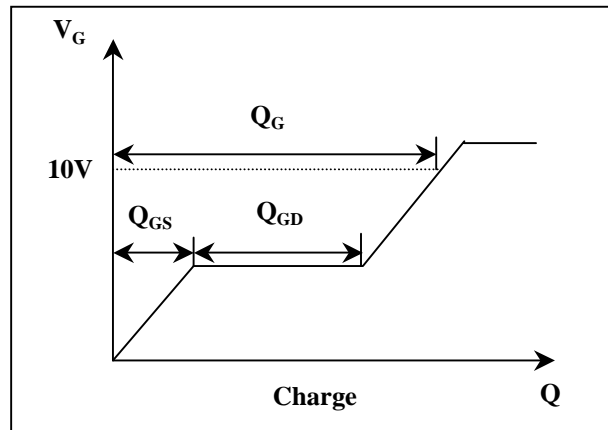


Fig 16. Gate Charge Waveform