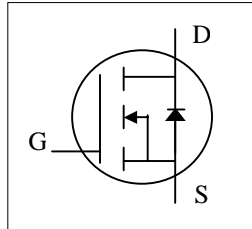




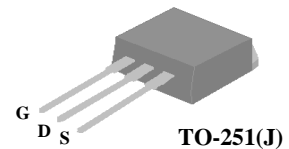
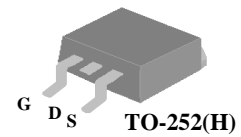
- ▼ 100% Avalanche Test
- ▼ Fast Switching Characteristics
- ▼ Simple Drive Requirement
- ▼ RoHS Compliant & Halogen-Free



BV_{DSS}	600V
$R_{DS(ON)}$	8 Ω
I_D	1.6A

Description

The TO-252 package is widely preferred for all commercial-industrial surface mount applications and suited for AC/DC converters. The through-hole version (AP01N60J) is available for low-profile applications.



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	600	V
V_{GS}	Gate-Source Voltage	± 30	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, V_{GS} @ 10V	1.6	A
$I_D@T_C=100^\circ C$	Continuous Drain Current, V_{GS} @ 10V	1	A
I_{DM}	Pulsed Drain Current ¹	6	A
$P_D@T_C=25^\circ C$	Total Power Dissipation	39	W
	Linear Derating Factor	0.31	W/ $^\circ C$
E_{AS}	Single Pulse Avalanche Energy ²	13	mJ
I_{AR}	Avalanche Current	1.6	A
E_{AR}	Repetitive Avalanche Energy	0.5	mJ
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$

Thermal Data

Symbol	Parameter	Value	Units
Rthj-c	Maximum Thermal Resistance, Junction-case	3.2	$^\circ C/W$
Rthj-a	Maximum Thermal Resistance, Junction-ambient (PCB mount) ⁴	62.5	$^\circ C/W$
Rthj-a	Maximum Thermal Resistance, Junction-ambient	110	$^\circ C/W$



AP01N60H/J-HF

Electrical Characteristics @ $T_j=25^{\circ}\text{C}$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	600	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ³	$V_{GS}=10V, I_D=0.8A$	-	-	8	Ω
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2	-	4	V
g_{fs}	Forward Transconductance	$V_{DS}=50V, I_D=0.8A$	-	0.8	-	S
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=600V, V_{GS}=0V$	-	-	10	μA
	Drain-Source Leakage Current ($T_j=125^{\circ}\text{C}$)	$V_{DS}=480V, V_{GS}=0V$	-	-	100	μA
I_{GSS}	Gate-Source Leakage	$V_{GS}=\pm 30V, V_{DS}=0V$	-	-	± 100	nA
Q_g	Total Gate Charge ³	$I_D=1.6A$	-	7.7	-	nC
Q_{gs}	Gate-Source Charge	$V_{DS}=480V$	-	1.5	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	$V_{GS}=10V$	-	2.6	-	nC
$t_{d(on)}$	Turn-on Delay Time ³	$V_{DD}=300V$	-	8	-	ns
t_r	Rise Time	$I_D=1.6A$	-	5	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=10\Omega, V_{GS}=10V$	-	14	-	ns
t_f	Fall Time	$R_D=187.5\Omega$	-	7	-	ns
C_{iss}	Input Capacitance	$V_{GS}=0V$	-	286	-	pF
C_{oss}	Output Capacitance	$V_{DS}=25V$	-	25	-	pF
C_{rss}	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	5	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I_S	Continuous Source Current (Body Diode)	$V_D=V_G=0V, V_S=1.5V$	-	-	1.6	A
I_{SM}	Pulsed Source Current (Body Diode) ¹		-	-	6	A
V_{SD}	Forward On Voltage ³	$T_j=25^{\circ}\text{C}, I_S=1.6A, V_{GS}=0V$	-	-	1.5	V

Notes:

1. Pulse width limited by max. junction.
2. Starting $T_j=25^{\circ}\text{C}$, $V_{DD}=50V$, $L=10\text{mH}$, $R_G=25\Omega$, $I_{AS}=1.6A$.
3. Pulse test
4. Surface mounted on 1 in² copper pad of FR4 board

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

APEC RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN.

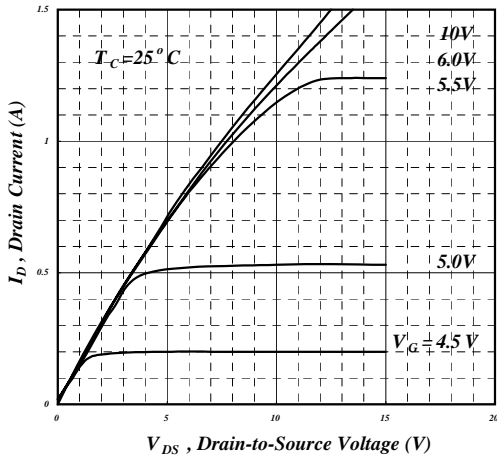


Fig 1. Typical Output Characteristics

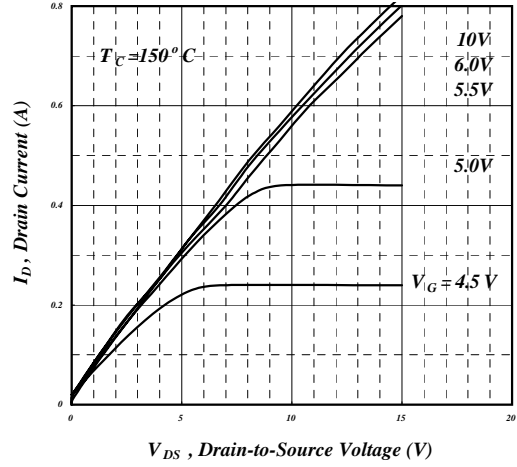


Fig 2. Typical Output Characteristics

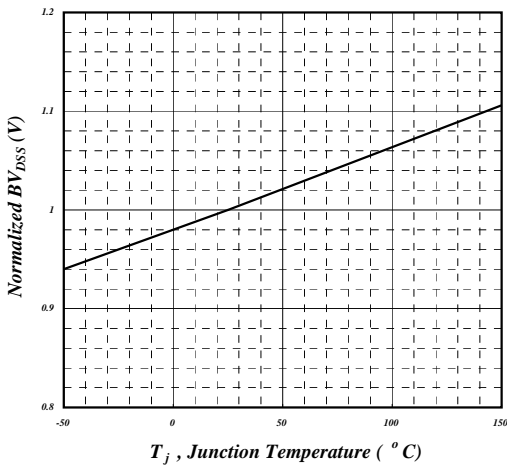


Fig 3. Normalized BV_{DSS} v.s. Junction Temperature

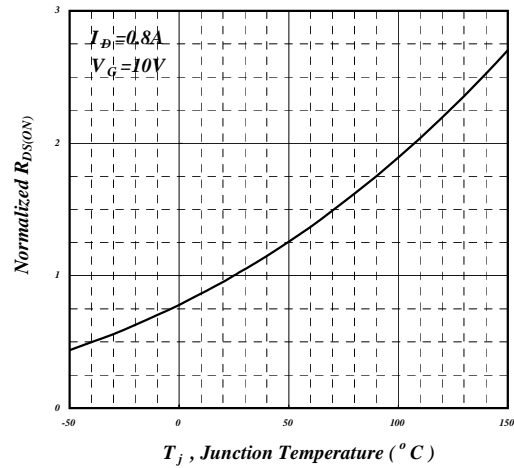


Fig 4. Normalized On-Resistance v.s. Junction Temperature

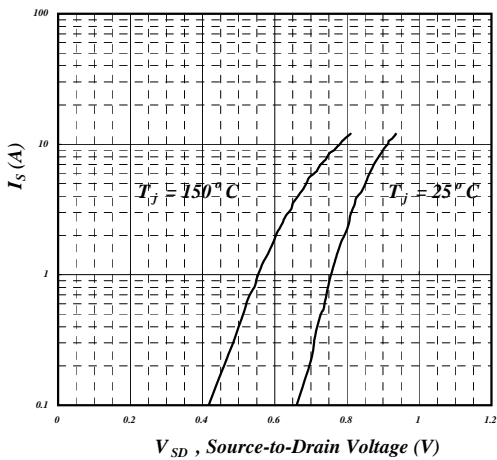


Fig 5. Forward Characteristic of Reverse Diode

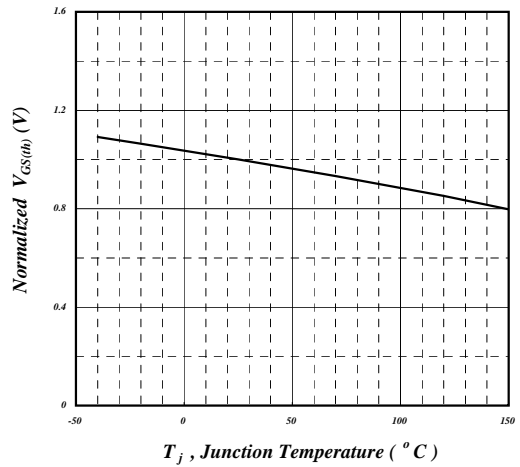


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

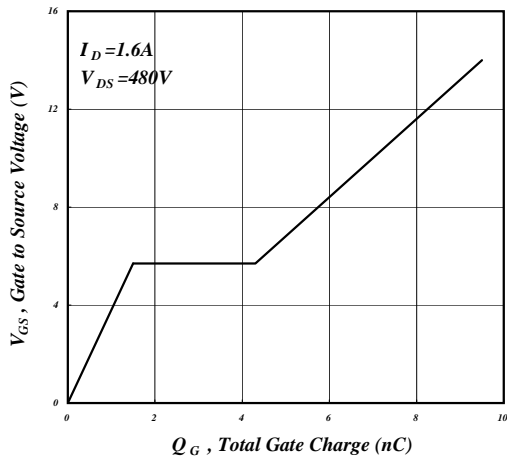


Fig 7. Gate Charge Characteristics

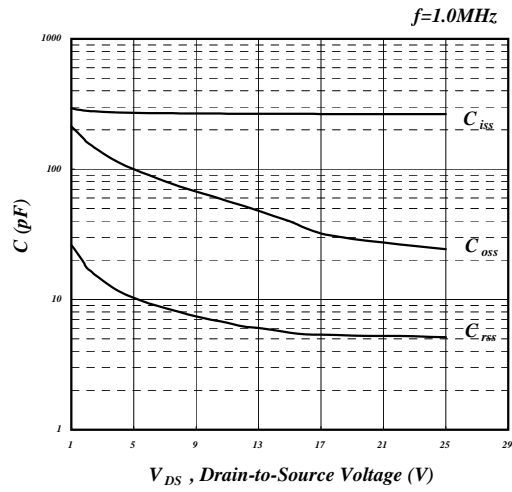


Fig 8. Typical Capacitance Characteristics

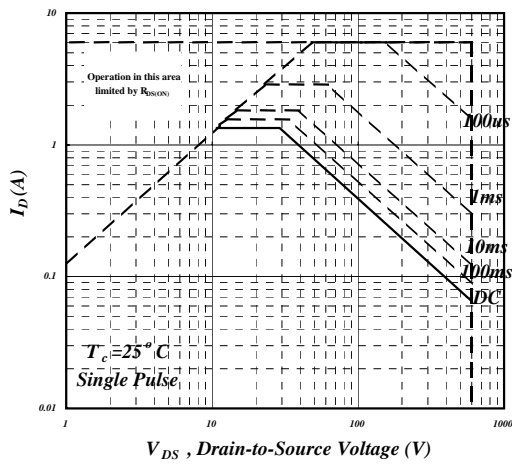


Fig 9. Maximum Safe Operating Area

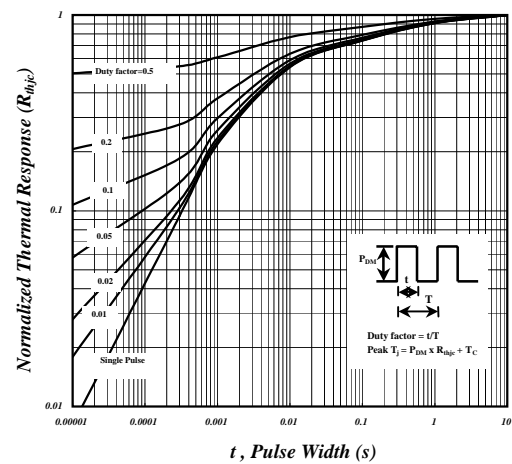


Fig 10. Effective Transient Thermal Impedance



Fig 11. Switching Time Waveform

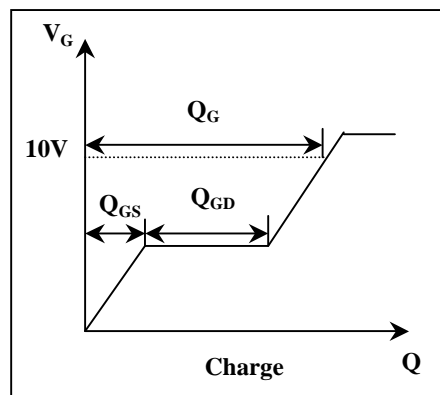


Fig 12. Gate Charge Waveform