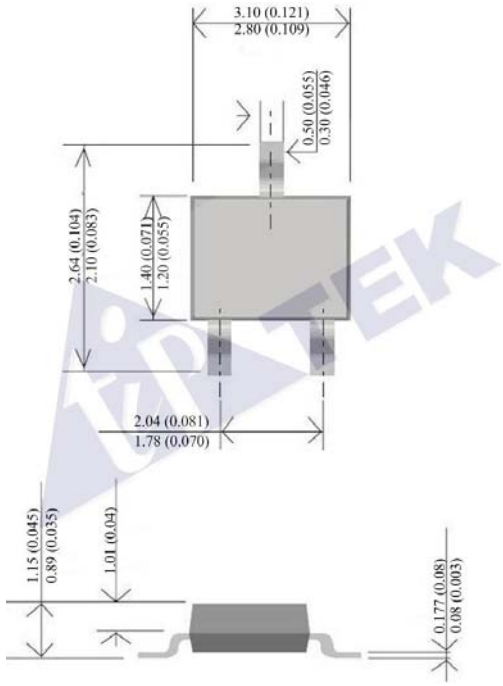
N-CHANNEL ENHANCEMENT MODE FIELD EFFECT TRANSISTOR



CASE：SOT-23

DIMENSIONS IN MILLIMETERS AND (INCHES)

FEATURES

- HIGH DENSITY CELL DESIGN FOR ULTRA LOW ON-RESISTANCE
- IMPROVED SHOOT-THROUGH FOM
- BOTH NORMAL AND PB FREE PRODUCT
  ARE AVAILABLE :NORMAL : 80~95% SN, 5~20% PB
  PB FREE: 99% SN ABOVE

MECHANICAL DATA

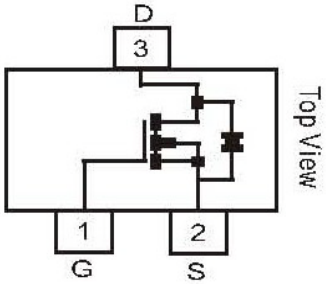
- WE DECLARE THAT THE MATERIAL OF PRODUCT COMPLIANCE WITH ROHS REUIREMENTS.
- Pb Free: TP2302NR
  Halogen Free: TP2302NR -H

ABSOLUTE MAXIMUM RATINGS

RATINGS AT 25°C AMBIENT TEMPERATURE UNLESS OTHERWISE SPECIFIED.

PATING	SYMBOL	TP2302NR	UNITS
DRAIN-SOURCE VOLTAGE	V_{DSS}	20	V
GATE-SOURCE VOLTAGE	V_{GSS}	±8	V
MAXIMUM DRAIN CURRENT-CONTINUE	I_D	2.3	A
MAXIMUM POWER DISSIPATION DERATING @ T_A = 25°C	P_D	0.9	W
OPERATING AND STORAGE JUNCTION TEMPERATURE RANGE	T_J;T_{STG}	- 55 TO +150	℃
THERMAL RESISTANCE, JUNCTION−TO−AMBIENT (NOTE1)	$R_{\theta JA}$	145	℃/W

NOTE:1. 1-in^2 2oz Cu PCB board



ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
STATIC						
DRAIN-SOURCE BREAKDOWN VOLTAGE	BV_{DSS}	V_{GS}=0V,I_D=-10uA	20	-	-	V
DRAIN-SOURCE ON-STATE RESISTANCE	$R_{DS(on)}$	V_{GS}=4.5V,I_D=2.8A	-	40	60	mΩ
DRAIN-SOURCE ON-STATE RESISTANCE	$R_{DS(on)}$	V_{GS}=2.5V,I_D=2.0A	-	50	115	
GATE THRESHOLD VOLTAGE	$V_{GS(th)}$	V_{DS}= V_{GS},I_D=250uA	0.65	0.95	1.20	V
ZERO GATE VOLTAGE DRAIN CURRENT	I_{DSS}	V_{DS}= 9.6V, V_{GS} =0V	-	-	-1	uA
GATE BODY LEAKAGE	I_{GSS}	V_{GS}=±8V, V_{DS}=0V	-	-	±100	nA
FORWARD TRANSCONDUCTANCE	g_{fs}	V_{DS}=5V, I_D=4.0A	-	6.5	-	S
DYNAMIC						
TOTAL GATE CHARGE	Q_g	V_{DS}=6V, I_D=2.8A V_{GS}=4.5V	-	3.69	-	nC
GATE-SOURCE CHARGE	Q_{gS}		-	0.70	-	
GATE-DRAIN CHARGE	Q_{gd}		-	1.06	-	
TURN-ON DELAY TIME	$t_{d(on)}$	V_{DD}=6V,R_L=6Ω I_D=1A,V_{GEN}=4.5V R_G=6Ω	-	6.16	-	ns
TURN-ON RISE TIME	t_r		-	7.56	-	
TURN-OFF DELAY TIME	$t_{d(off)}$		-	16.61	-	
TURN-OFF FALL TIME	t_f		-	4.07	-	
INPUT CAPACITANCE	C_{iss}	V_{DS}=6V, V_{GS}=0V f=1.0MHz	-	427.12	-	pF
OUTPUT CAPACITANCE	C_{oss}		-	80.56	-	
REVERSE TRANSFER CAPACITANCE	C_{rss}		-	57.00	-	
SOURCE-DRAIN DIODE						
DIODE FORWARD VOLTAGE	V_{SD}	I_S=-1.6A, V_{GS}=0V	-	-	-	V

NOTE: Pulse Test: Pulse Width≦300 us, Duty Cycle≦2.0%.

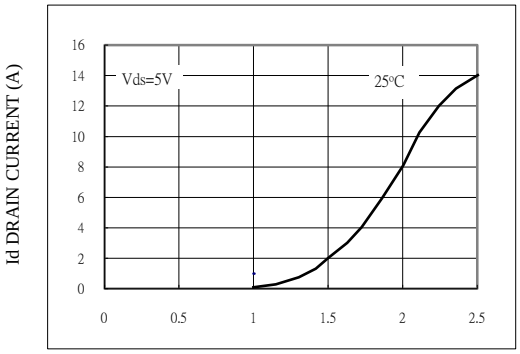


Fig.1-TRANSFER CHARACTERISTICS

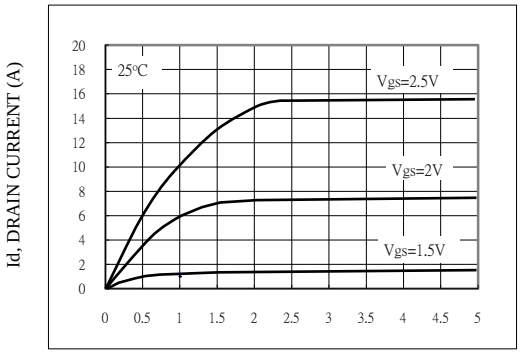


Fig.2-ON-REGION CHARACTERISTICS

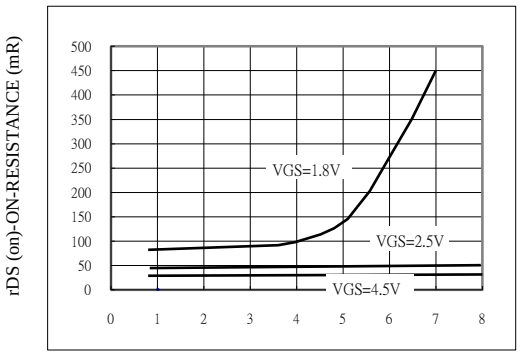


Fig.3- ON-RESISTANCE VERSUS DRAIN CURRENT

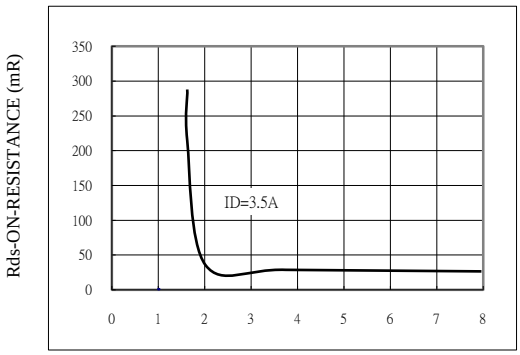


Fig.4-ON-RESISTANCE VS. GATE-TO-SOURCE VOLTAGE

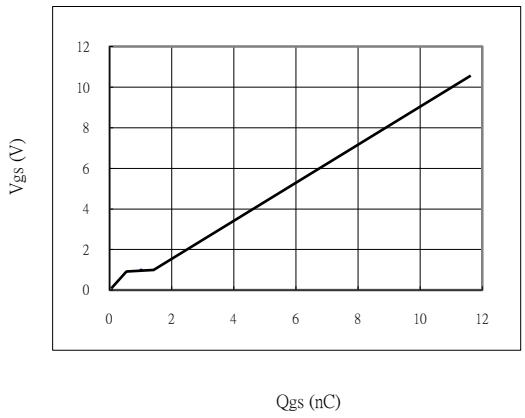


Fig.5-GATE CHARGE

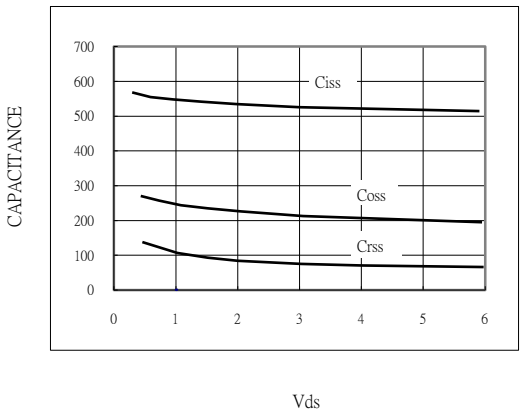


Fig.6-CAPACITANCE

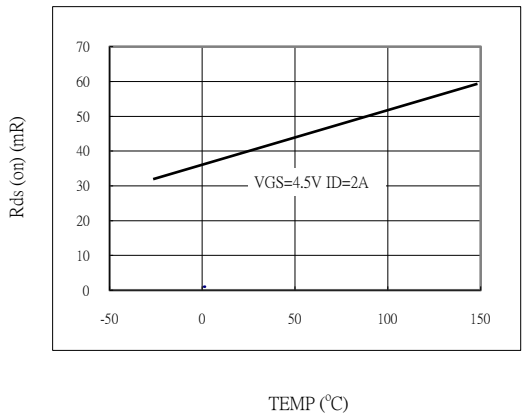


Fig.7-ON-RESISTANCE VS. JUNCTION TEMPERATURE

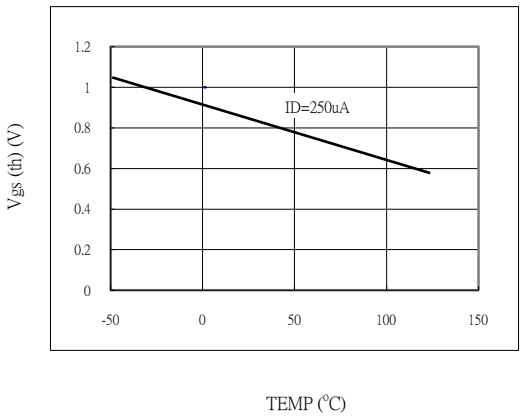


Fig.8-Vth VS.JUNCTION TEMPERATURE