Data Sheet June 2000 File Number 4396.5

10A, 30V, 0.013 Ohm, N-Channel, Logic Level UltraFET Power MOSFET

This N-Channel power MOSFET is manufactured using the innovative UltraFET process. This advanced process technology achieves the lowest possible on-resistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low-voltage bus switches, and power management in portable and battery-operated products.

Formerly developmental type TA76131.

Ordering Information

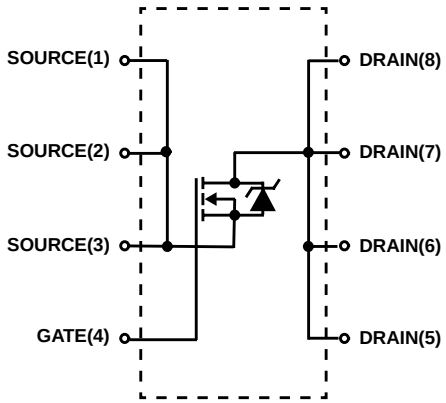
PART NUMBER	PACKAGE	BRAND
HUF76131SK8	MS-012AA	76131SK8

NOTE: When ordering, use the entire part number. Add the suffix T to obtain the variant in tape and reel, e.g., HUF76131SK8T.

Features

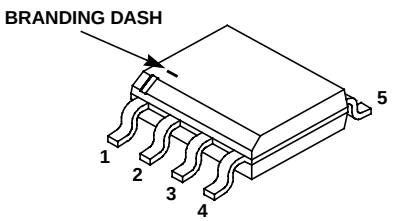
- Logic Level Gate Drive
- 10A, 30V
- Ultra Low On-Resistance, $r_{DS(ON)} = 0.013\Omega$
- Temperature Compensating PSPICE® Model
- Thermal Impedance SPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
  - TB334, “Guidelines for Soldering Surface Mount Components to PC Boards”

Symbol



Packaging

JEDEC MS-012AA



Absolute Maximum Ratings $T_A = 25^oC$, Unless Otherwise Specified

		HUF76131SK8	UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	30	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	30	V
Gate to Source Voltage	V_{GS}	±16	V
Drain Current			
Continuous (Figure 2) (Notes 2, 3)	I_D	10	A
Pulsed Drain Current	I_{DM}	Figure 5	
Pulsed Avalanche Rating	E_{AS}	Figure 6	
Power Dissipation	P_D	2.5	W
Derate Above 25^oC		0.02	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 150^oC.

Electrical Specifications $T_A = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250µA, V_{GS} = 0V (Figure 11)		30	-	-	V
Gate to Source Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250µA (Figure 10)		1	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 25V, V_{GS} = 0V		-	-	1	µA
		V_{DS} = 25V, V_{GS} = 0V, $T_A = 150^oC$		-	-	250	µA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±16V		-	-	±100	nA
Drain to Source On Resistance	$r_{DS(ON)}$	I_D = 10A, V_{GS} = 4.5V (Figures 9,14)		-	0.017	0.018	Ω
		I_D = 10A, V_{GS} = 5V		-	0.015	0.017	Ω
		I_D = 10A, V_{GS} = 10V		-	0.011	0.013	Ω
Turn-On Time	t_{ON}	V_{DD} = 15V, $I_D \cong$ 10A, R_L = 1.5Ω, V_{GS} = 5V, R_{GS} = 6.8Ω (Figure 15)		-	-	115	ns
Turn-On Delay Time	$t_{d(ON)}$			-	15	-	ns
Rise Time	t_r			-	61	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	33	-	ns
Fall Time	t_f			-	36	-	ns
Turn-Off Time	t_{OFF}			-	-	105	ns
Total Gate Charge	$Q_{g(TOT)}$	V_{GS} = 0V to 10V	V_{DD} = 15V, $I_D \cong$ 10A, R_L = 1.5Ω, $I_{g(REF)}$ = 1.0mA (Figure 13)	-	39	47	nC
Gate Charge at 5V	$Q_{g(5)}$	V_{GS} = 0V to 5V		-	22	26	nC
Threshold Gate Charge	$Q_{g(TH)}$	V_{GS} = 0V to 1V		-	1.53	1.85	nC
Gate to Source Gate Charge	Q_{gs}			-	4.00	-	nC
Gate to Drain "Miller" Charge	Q_{gd}			-	9.50	-	nC
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz (Figure 12)		-	1605	-	pF
Output Capacitance	C_{OSS}			-	685	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	115	-	pF
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Pad Area = 0.76 in^2 (Note 2)		-	-	50	$^oC/W$
		Pad Area = 0.054 in^2 (See TB377)		-	-	143.4	$^oC/W$
		Pad Area = 0.0115 in^2 (See TB377)		-	-	177.3	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	I_{SD} = 10A	-	-	1.25	V
		I_{SD} = 2.3A	-	-	1.1	V
Reverse Recovery Time	t_{rr}	I_{SD} = 2.3A, dI_{SD}/dt = 100A/µs	-	-	57	ns
Reverse Recovered Charge	Q_{RR}	I_{SD} = 2.3A, dI_{SD}/dt = 100A/µs	-	-	81	nC

NOTES:

2. $50^oC/W$ measured using FR-4 board with 0.76 in^2 footprint at 10 seconds.
3. $177.3^oC/W$ measured using FR-4 board with 0.0115 in^2 footprint at 1000 seconds.

Typical Performance Curves

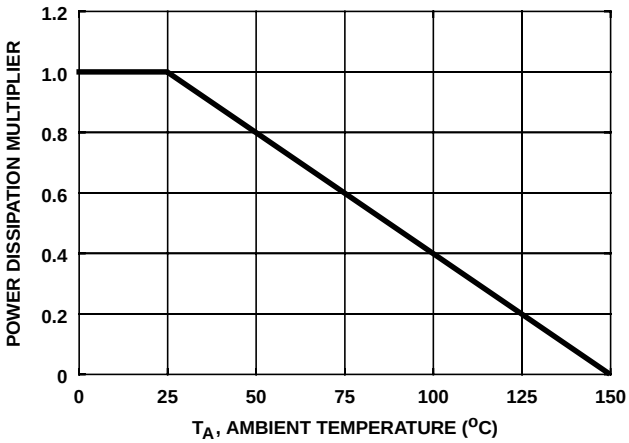


FIGURE 1. NORMALIZED POWER DISSIPATION vs AMBIENT TEMPERATURE

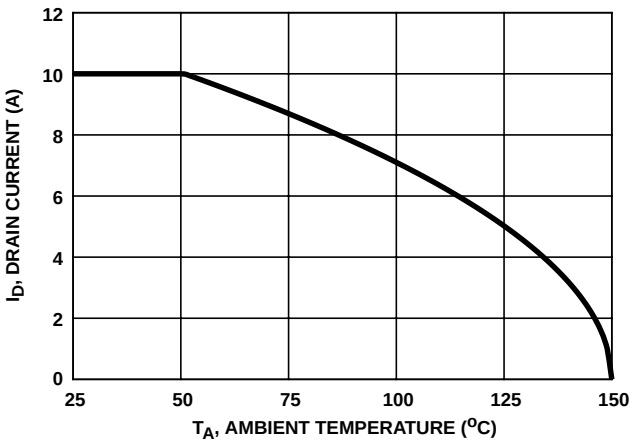


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs AMBIENT TEMPERATURE

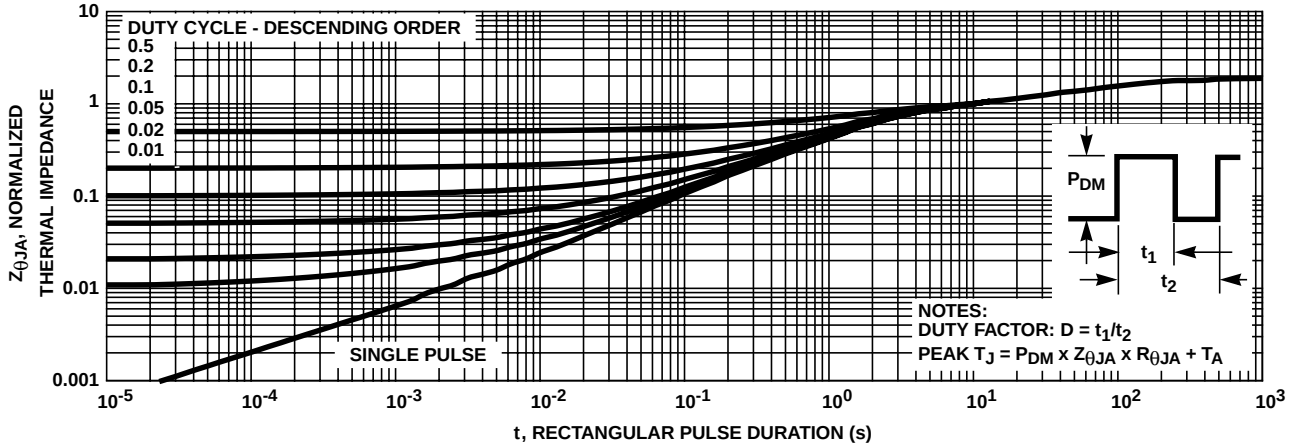


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

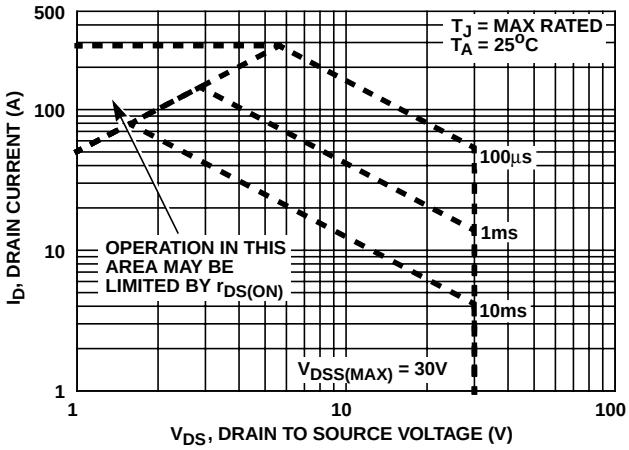


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

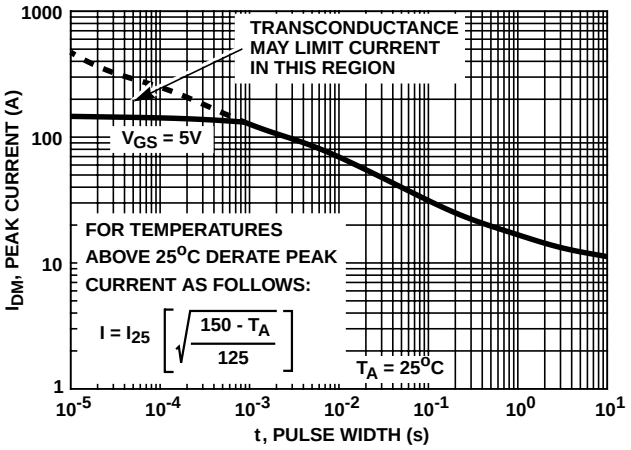
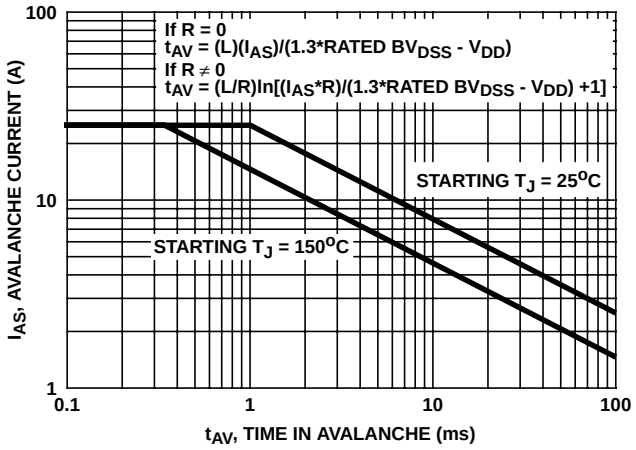


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves (Continued)



NOTE: Refer to Intersil Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

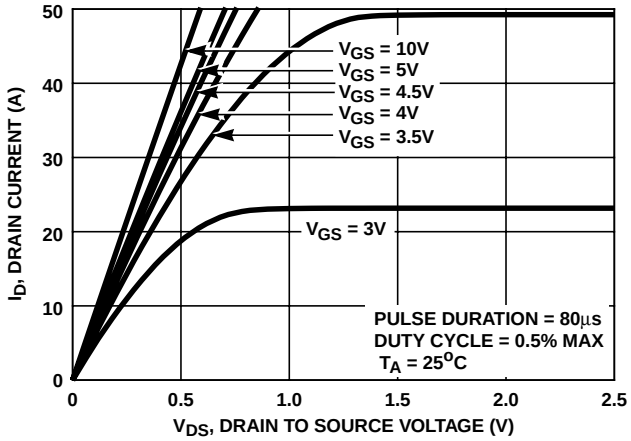


FIGURE 7. SATURATION CHARACTERISTICS

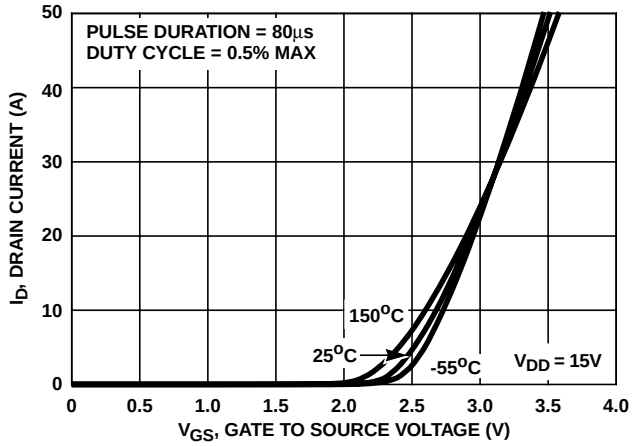


FIGURE 8. TRANSFER CHARACTERISTICS

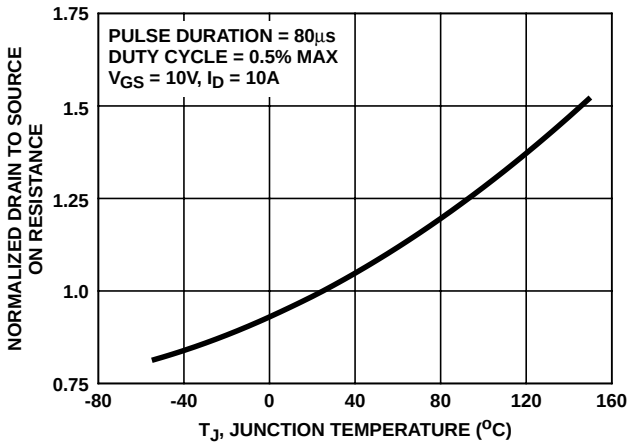


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

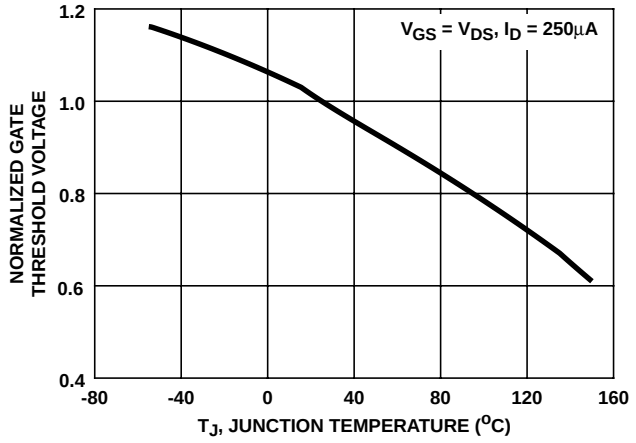


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

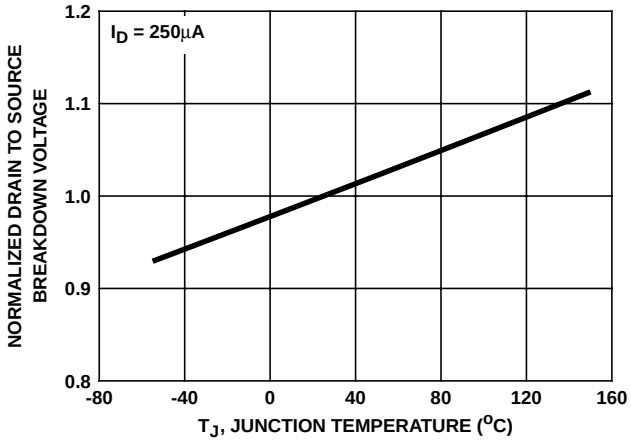


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

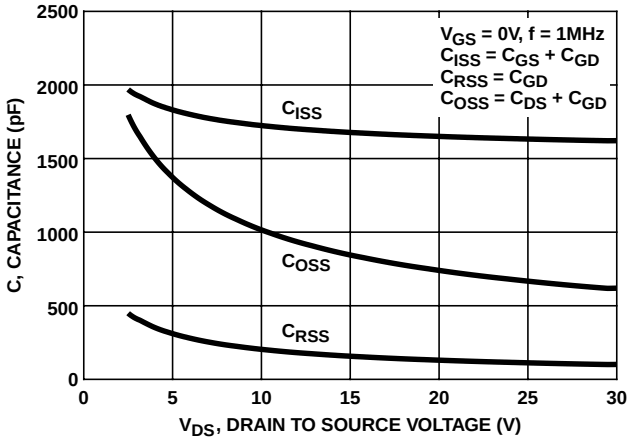
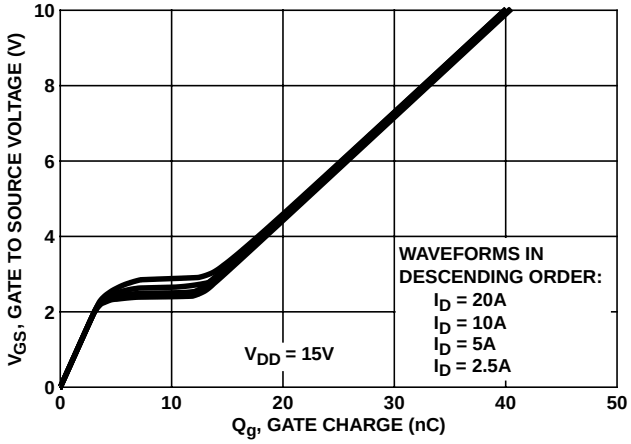


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes 7254 and 7260.

FIGURE 13. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

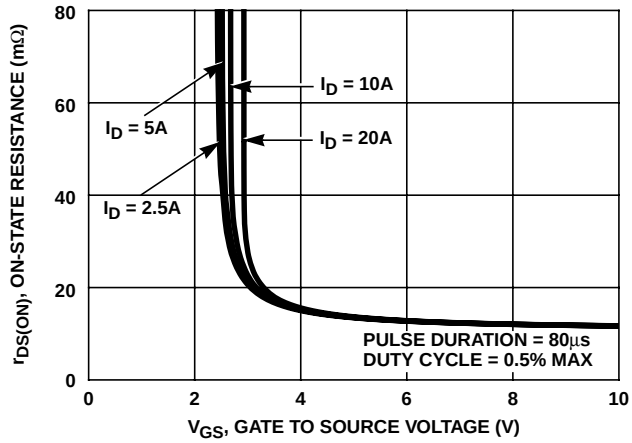


FIGURE 14. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

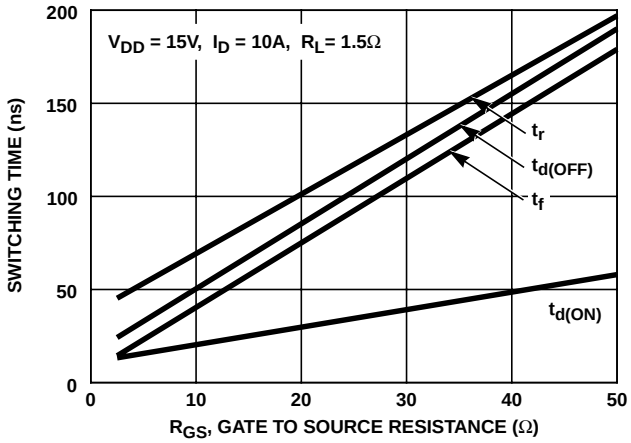


FIGURE 15. SWITCHING TIME vs GATE RESISTANCE

Test Circuits and Waveforms

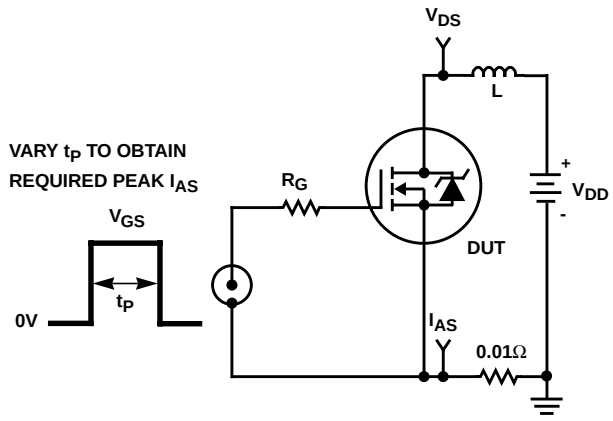


FIGURE 16. UNCLAMPED ENERGY TEST CIRCUIT

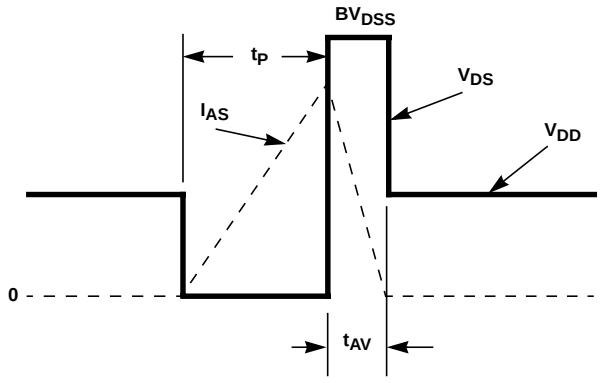


FIGURE 17. UNCLAMPED ENERGY WAVEFORMS

Test Circuits and Waveforms (Continued)

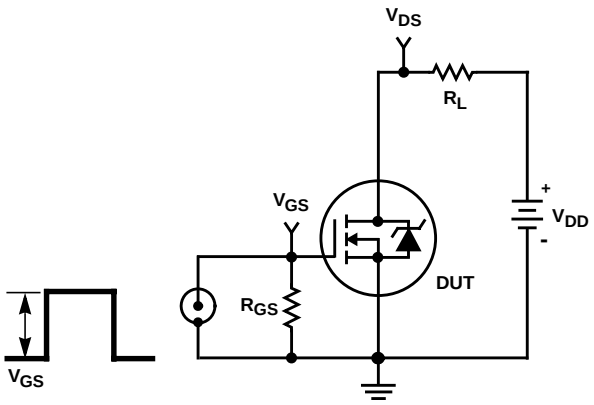


FIGURE 18. SWITCHING TIME TEST CIRCUIT

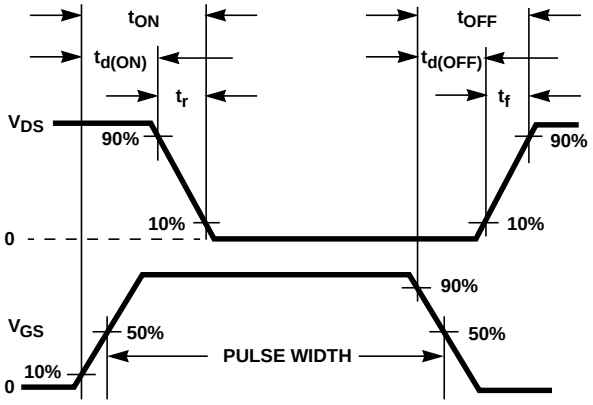


FIGURE 19. SWITCHING TIME WAVEFORM

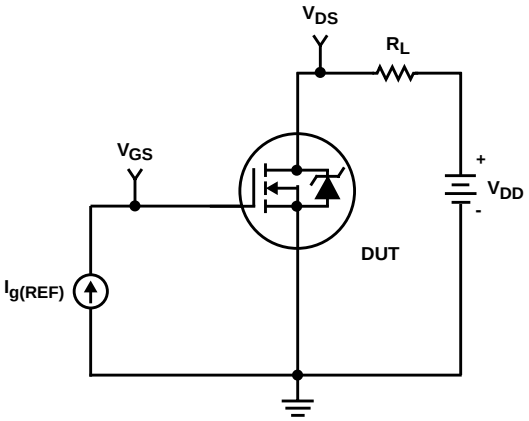


FIGURE 20. GATE CHARGE TEST CIRCUIT

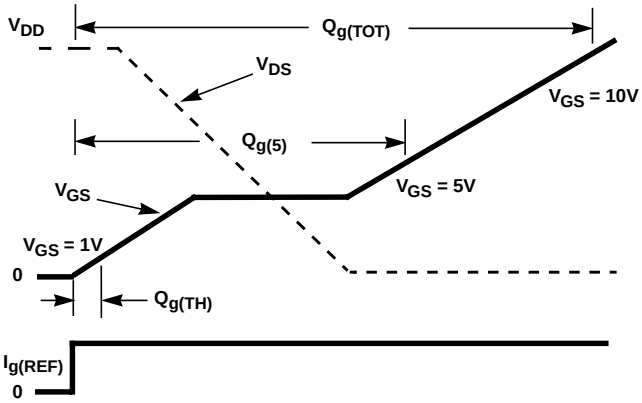


FIGURE 21. GATE CHARGE WAVEFORMS

Thermal Resistance vs Mounting Pad Area

The maximum rated junction temperature T_{JMAX} constrains the maximum allowable device power dissipation P_{Dmax} in an application. The application ambient temperature T_A (^oC) and thermal impedance $Z_{\theta JA}$ ($^oC/W$) must be reviewed to ensure that T_{JMAX} (^oC) is never exceeded. Equation 1 mathematically represents the relationship.

$$P_{DMAX} = \frac{(T_{JMAX} - T_A)}{Z_{\theta JA}} \quad \text{(EQ. 1)}$$

Intersil provides thermal information to assist the designer's preliminary application evaluation. Precise determination of P_{DMAX} is complex and influenced by many factors:

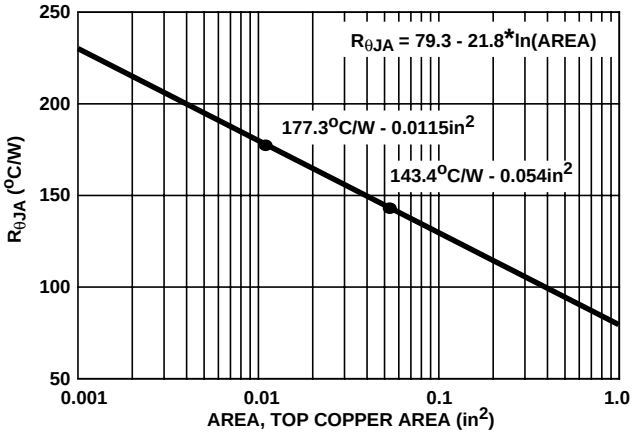
1. PC heat sink area and location (top and bottom), copper leads and mounting pad area.
2. Air Flow, board orientation and type.
3. Power pulse width and duty factor.

Figure 22 addresses these points by depicting $R_{\theta JA}$ values vs. top copper (component side) heat sink area. The measurements were performed in still air using a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power.

Figure 22 also displays the two $R_{\theta JA}$ values listed in the Electrical Specifications table. The two points were chosen to graphically depict the compromise between copper board area, thermal resistance and ultimately power dissipation.

Thermal resistance values corresponding to other component side copper areas can be obtained from Figure 22 or by calculation using Equation 2. Area in Equation 2 is the top copper area including the gate and source pads.

$$R_{\theta JA} = 79.3 - 21.8 \times \ln(Area) \quad \text{(EQ. 2)}$$



IGURE 22. THERMAL RESISTANCE vs MOUNTING PAD AREA

Figure 22 provides the necessary information for steady state junction temperature or power dissipation calculations. Transient pulse applications are best studied using the Intersil device SPICE thermal model.

PSPICE Electrical Model

SUBCKT HUF76131 2 1 3 ; rev 12/31/97

CA 12 8 2.22-9
CB 15 14 2.13e-9
CIN 6 8 1.52e-9

DBODY 7 5 DBODYMOD
DBREAK 5 11 DBREAKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 37.4
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTHRES 6 21 19 8 1
EVTEMP 20 6 18 22 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 1.04e-9
LSOURCE 3 7 1.29e-10

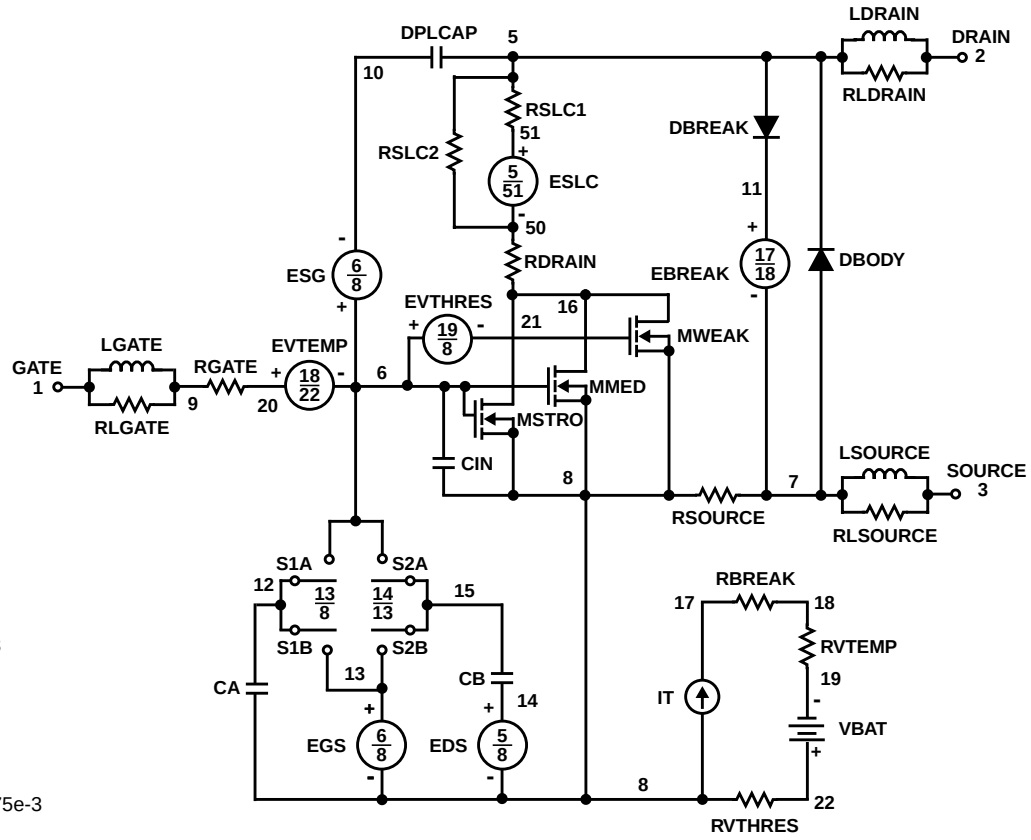
MMED 16 6 8 8 MMEDMOD
MSTRO 16 6 8 8 MSTROMOD
MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1
RDRAIN 50 16 RDRAINMOD 1.94e-3
RGATE 9 20 2.20
RLDRAIN 2 5 10
RLGATE 1 9 10.4
RLSOURCE 3 7 1.29
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
RSOURCE 8 7 RSOURCEMOD 8.75e-3
RVTHRES 22 8 RVTHRESMOD 1
RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*275),3))}



.MODEL DBODYMOD D (IS = 2.25e-12 RS = 6.05e-3 IKF=16.00 TRS1 = 1.14e-4 TRS2 = 1.23e-6 CJO = 2.35e-9 TT = 2.71e-8 M = 0.44)
.MODEL DBREAKMOD D (RS = 1.05e-1 TRS1 = 1.01e-4 TRS2 = 1.11e-7)
.MODEL DPLCAPMOD D (CJO = 1.08e-9 IS = 1e-30 N = 10 M = 0.69)
.MODEL MMEDMOD NMOS (VTO = 1.89 KP = 5.05 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 2.20)
.MODEL MSTROMOD NMOS (VTO = 2.22 KP = 125.00 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL MWEAKMOD NMOS (VTO = 1.62 KP = 0.10 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 22.0 RS = 0.1)
.MODEL RBREAKMOD RES (TC1 = 9.54e-4 TC2 = 1.07e-7)
.MODEL RDRAINMOD RES (TC1 = 1.61e-2 TC2 = 5.17e-5)
.MODEL RSLCMOD RES (TC1 = 1.03e-5 TC2 = 7.67e-7)
.MODEL RSOURCEMOD RES (TC1 = 0 TC2 = 0)
.MODEL RVTHRESMOD RES (TC = -2.81e-3 TC2 = -8.75e-6)
.MODEL RVTEMPMOD RES (TC1 = -6.68e-4 TC2 = 8.80e-7)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -5.80 VOFF= -1.50)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -1.50 VOFF= -5.80)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -0.50 VOFF= -0.00)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.00 VOFF= -0.50)

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

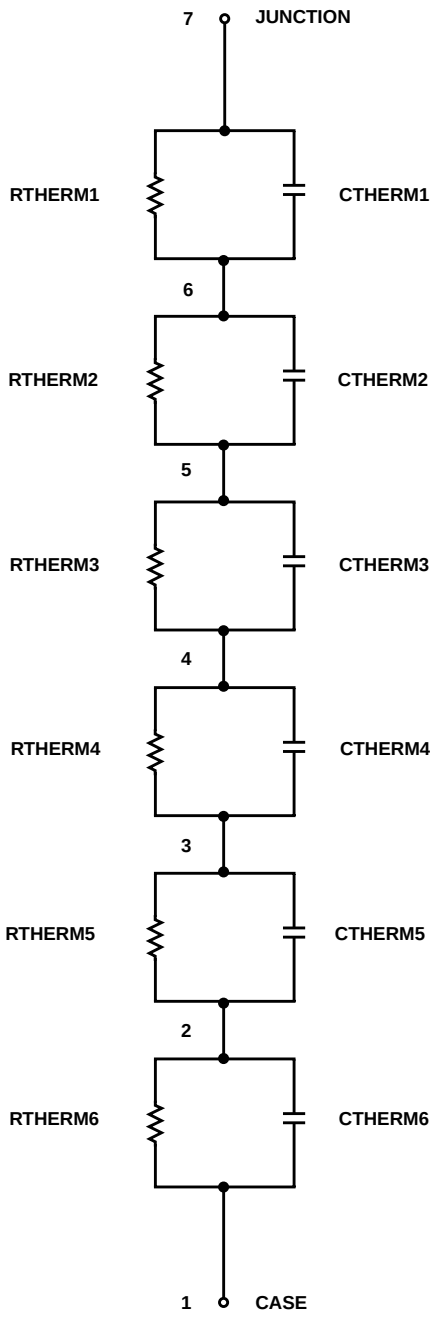
SPICE Thermal Model

REV 20 Feb 98

HUF76131

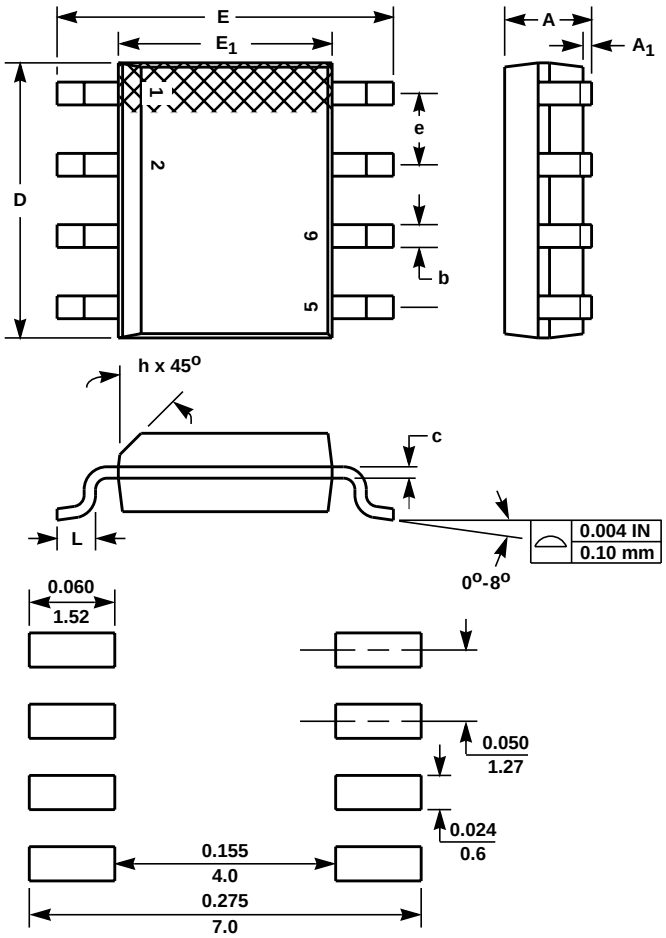
CTHERM1 7 6 3.75e-4
CTHERM2 6 5 3.05e-3
CTHERM3 5 4 3.70e-2
CTHERM4 4 3 2.52e-2
CTHERM5 3 2 8.50e-2
CTHERM6 2 1 7.95e-1

RTHERM1 7 6 3.95e-2
RTHERM2 6 5 2.50e-1
RTHERM3 5 4 4.00e-1
RTHERM4 4 3 6.35
RTHERM5 3 2 2.02e1
RTHERM6 2 1 4.80e1



MS-012AA

8 LEAD JEDEC MS-012AA SMALL OUTLINE PLASTIC PACKAGE



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A_1	0.004	0.0098	0.10	0.25	-
b	0.013	0.020	0.33	0.51	-
c	0.0075	0.0098	0.19	0.25	-
D	0.189	0.1968	4.80	5.00	2
E	0.2284	0.244	5.80	6.20	-
E_1	0.1497	0.1574	3.80	4.00	3
e	0.050 BSC		1.27 BSC		-
H	0.0099	0.0196	0.25	0.50	-
L	0.016	0.050	0.40	1.27	4

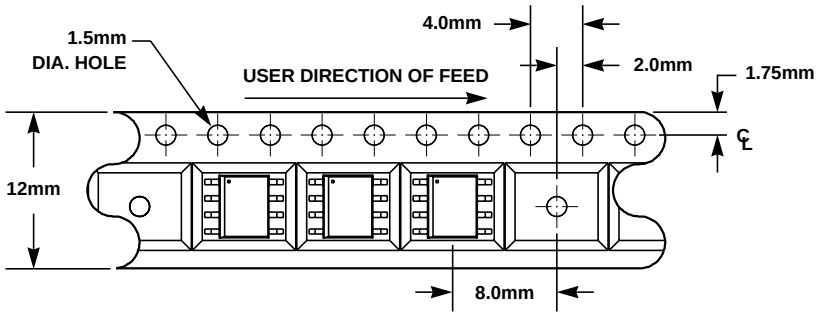
NOTES:

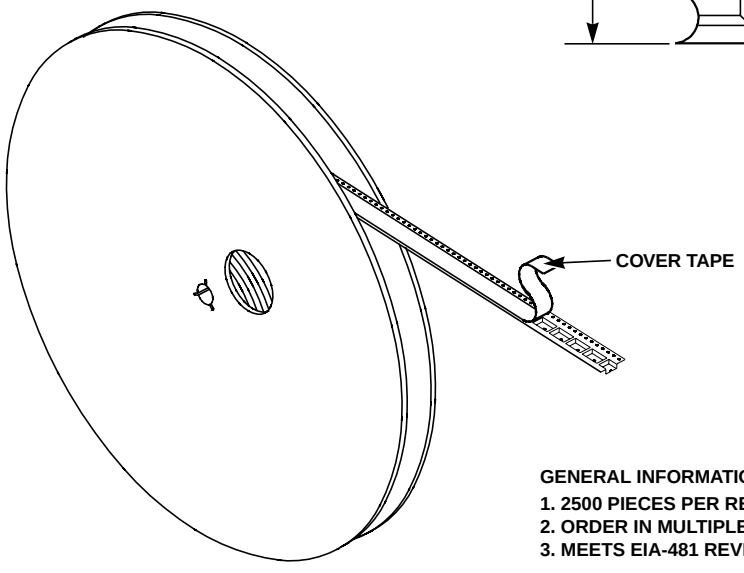
1. All dimensions are within allowable dimensions of Rev. C of JEDEC MS-012AA outline dated 5-90.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.006 inches (0.15mm) per side.
3. Dimension “E_1” does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 0.010 inches (0.25mm) per side.
4. “L” is the length of terminal for soldering.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. Controlling dimension: Millimeter.
7. Revision 8 dated 5-99.

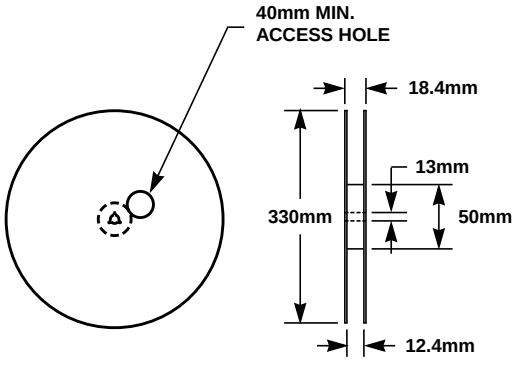
MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE-MOUNTED APPLICATIONS

MS-012AA

12mm TAPE AND REEL







GENERAL INFORMATION

1. 2500 PIECES PER REEL.
2. ORDER IN MULTIPLES OF FULL REELS ONLY.
3. MEETS EIA-481 REVISION “A” SPECIFICATIONS.