

# FCD7N60

## N-Channel SuperFET® MOSFET 600 V, 7 A, 600 mΩ

### Features

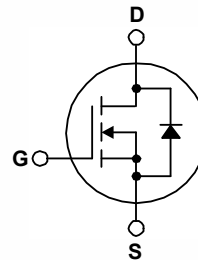
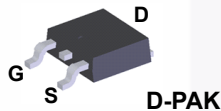
- 650 V @  $T_J = 150^\circ\text{C}$
- Typ.  $R_{DS(on)} = 530\text{ m}\Omega$
- Ultra Low Gate Charge (Typ.  $Q_g = 23\text{ nC}$ )
- Low Effective Output Capacitance (Typ.  $C_{oss(eff.)} = 60\text{ pF}$ )
- 100% Avalanche Tested
- RoHS Compliant

### Application

- LCD / LED TV and Monitor
- Lighting
- Solar Inverter
- AC-DC Power Supply

### Description

SuperFET® MOSFET is Fairchild Semiconductor's first generation of high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance,  $dv/dt$  rate and higher avalanche energy. Consequently, SuperFET MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications.



### MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FCD7N60TM / FCD7N60TM_WS	Unit
$V_{DSS}$	Drain to Source Voltage	600	V
$I_D$	Drain Current	- Continuous ( $T_C = 25^\circ\text{C}$ )	7
		- Continuous ( $T_C = 100^\circ\text{C}$ )	4.4
$I_{DM}$	Drain Current	- Pulsed (Note 1)	21
$V_{GSS}$	Gate to Source Voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	230	mJ
$I_{AR}$	Avalanche Current (Note 1)	7	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	8.3	mJ
$dv/dt$	Peak Diode Recovery $dv/dt$ (Note 3)	20	V/ns
$P_D$	Power Dissipation	( $T_C = 25^\circ\text{C}$ )	83
		- Derate Above $25^\circ\text{C}$	0.67
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	FCD7N60TM / FCD7N60TM_WS	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	1.5	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	83	

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCD7N60TM	FCD7N60	D-PAK	Tape and Reel	330 mm	16 mm	2500 units
FCD7N60TM_WS	FCD7N60	D-PAK	Tape and Reel	330 mm	16 mm	2500 units

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}, T_C = 25^\circ\text{C}$	600	-	-	V
		$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}, T_C = 150^\circ\text{C}$	-	650	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	-	0.6	-	$\text{V}/^\circ\text{C}$
$BV_{DS}$	Drain to Source Avalanche Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 7.0\text{ A}$	-	700	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 480\text{ V}, T_C = 125^\circ\text{C}$	-	-	10	$\mu\text{A}$
$I_{GSS}$	Gate to Body Leakage Current	$V_{GS} = \pm 30\text{ V}, V_{DS} = 0\text{ V}$	-	-	$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 3.5\text{ A}$	-	0.53	0.6	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 3.5\text{ A}$	-	6	-	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	710	920	pF
$C_{oss}$	Output Capacitance		-	380	500	pF
$C_{rss}$	Reverse Transfer Capacitance		-	34	-	pF
$C_{oss}$	Output Capacitance	$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	22	29	pF
$C_{oss(eff.)}$	Effective Output Capacitance	$V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$	-	60	-	pF

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 300\text{ V}, I_D = 7.0\text{ A}, V_{GS} = 10\text{ V}, R_G = 25\ \Omega$	-	35	80	ns
$t_r$	Turn-On Rise Time		-	55	120	ns
$t_{d(off)}$	Turn-Off Delay Time		-	75	160	ns
$t_f$	Turn-Off Fall Time		(Note 4)	-	32	75
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 480\text{ V}, I_D = 7.0\text{ A}, V_{GS} = 10\text{ V}$	-	23	30	nC
$Q_{gs}$	Gate to Source Gate Charge		-	4.2	5.5	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		(Note 4)	-	11.5	-

### Drain-Source Diode Characteristics

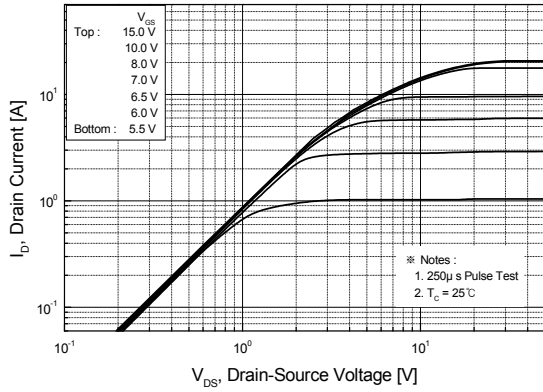
$I_S$	Maximum Continuous Drain to Source Diode Forward Current	-	-	7	A	
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current	-	-	21	A	
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_{SD} = 7.0\text{ A}$	-	-	1.4	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_{SD} = 7.0\text{ A}, di_F/dt = 100\text{ A}/\mu\text{s}$	-	360	-	ns
$Q_{rr}$	Reverse Recovery Charge		-	4.5	-	$\mu\text{C}$

#### Notes:

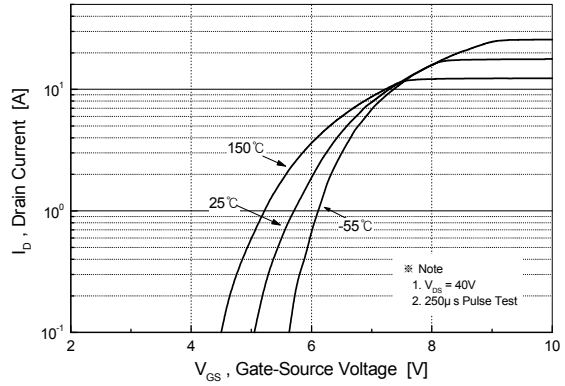
1. Repetitive rating: pulse-width limited by maximum junction temperature.
2.  $I_{AS} = 3.5\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\ \Omega$ , starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq 7\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , starting  $T_J = 25^\circ\text{C}$ .
4. Essentially independent of operating temperature typical characteristics.

## Typical Performance Characteristics

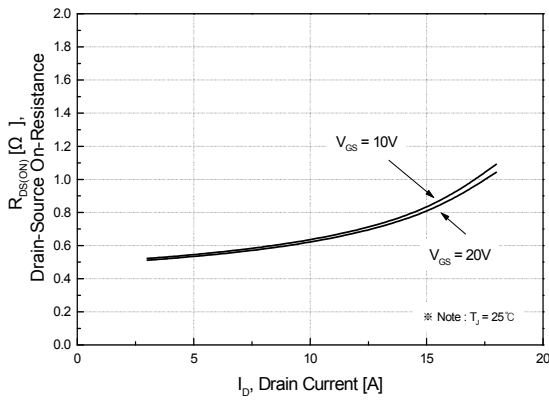
**Figure 1. On-Region Characteristics**



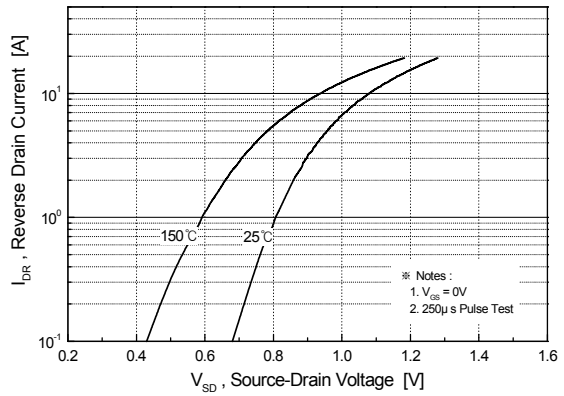
**Figure 2. Transfer Characteristics**



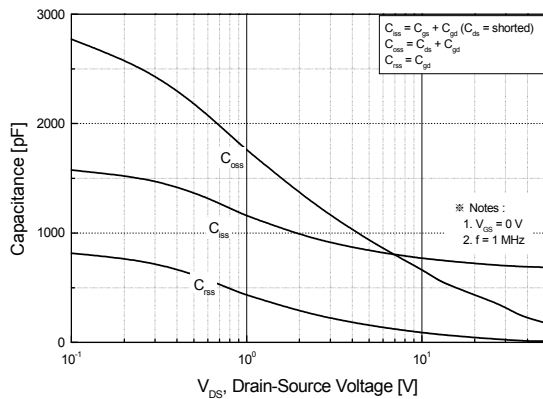
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



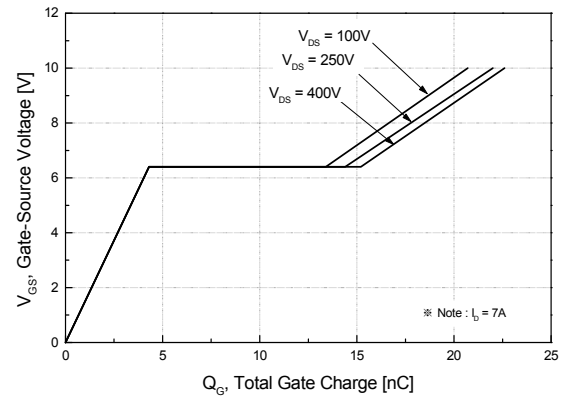
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**

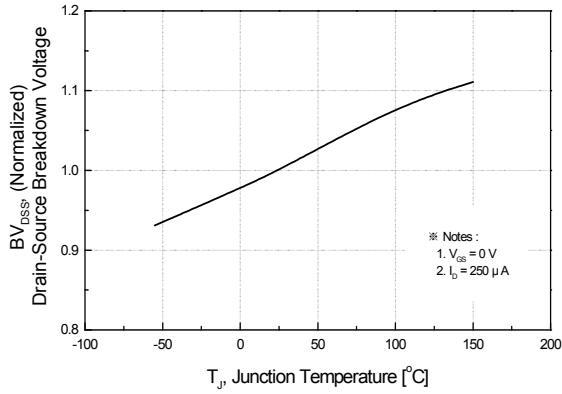


**Figure 6. Gate Charge Characteristics**

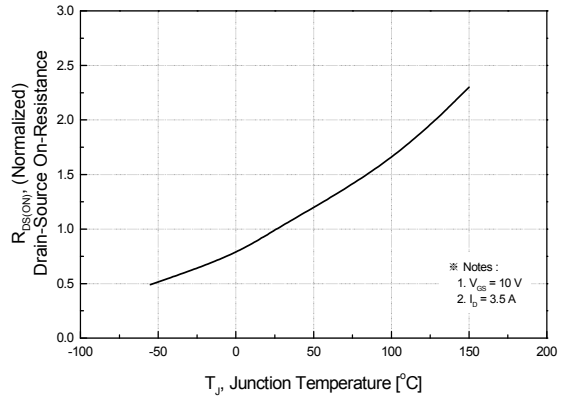


## Typical Performance Characteristics (Continued)

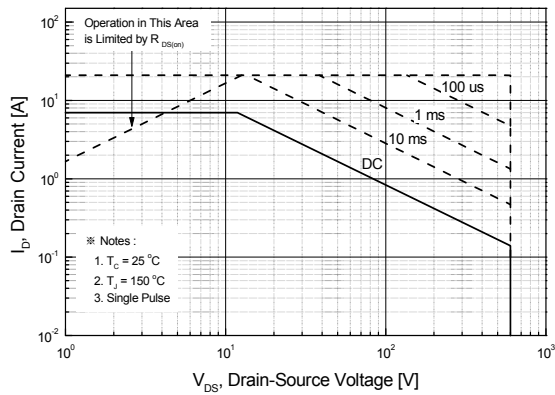
**Figure 7. Breakdown Voltage Variation vs. Temperature**



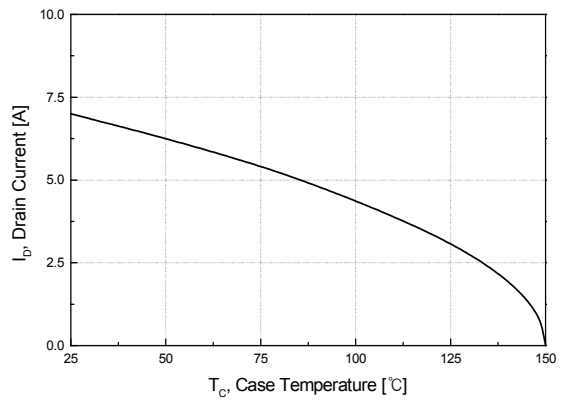
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs. Case Temperature**



**Figure 11. Transient Thermal Response Curve**

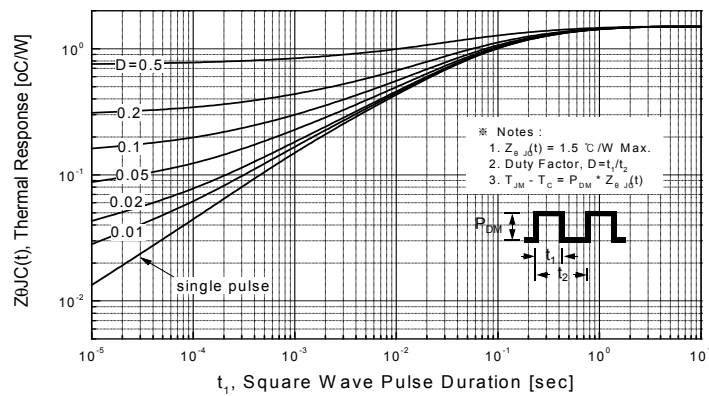




Figure 12. Gate Charge Test Circuit & Waveform



Figure 13. Resistive Switching Test Circuit & Waveforms

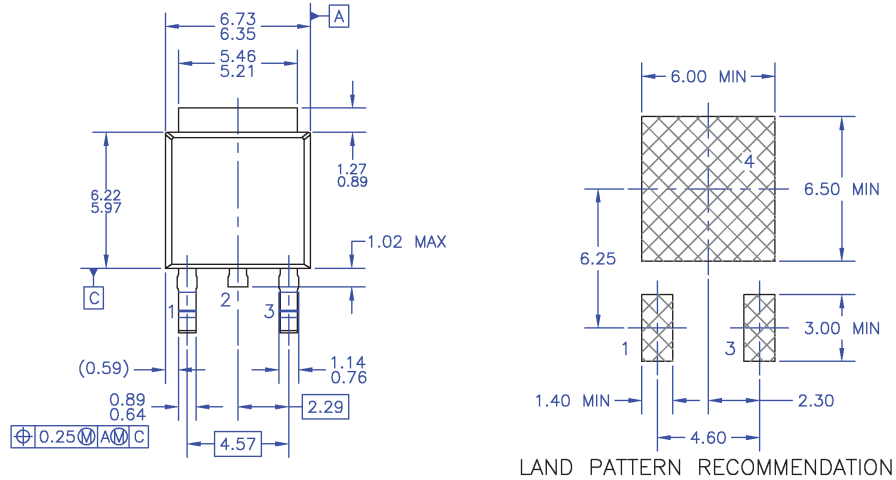


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

## Mechanical Dimensions



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
  - B) ALL DIMENSIONS ARE IN MILLIMETERS.
  - C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
  - D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
  - E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.
  - F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
  - G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO220P1003X238-3N.
  - H) DRAWING NUMBER AND REVISION: MKT-T0252A03REV8

**Figure 16. TO252 (D-PAK), Molded, 3-Lead, Option AA&AB**

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| AX-CAP®*   | FRFET®  | PowerXS™  | <b>SYSTEM GENERAL</b> ®*  |
| BitSiC™  | Global Power Resource <sup>SM</sup>             | Programmable Active Droop™  | TinyBoost®  |
| Build it Now™  | GreenBridge™                                    | QFET®   | TinyBuck®   |
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| FastvCore™   | OptoHiT™  | SupreMOS®   | VisualMax™  |
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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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